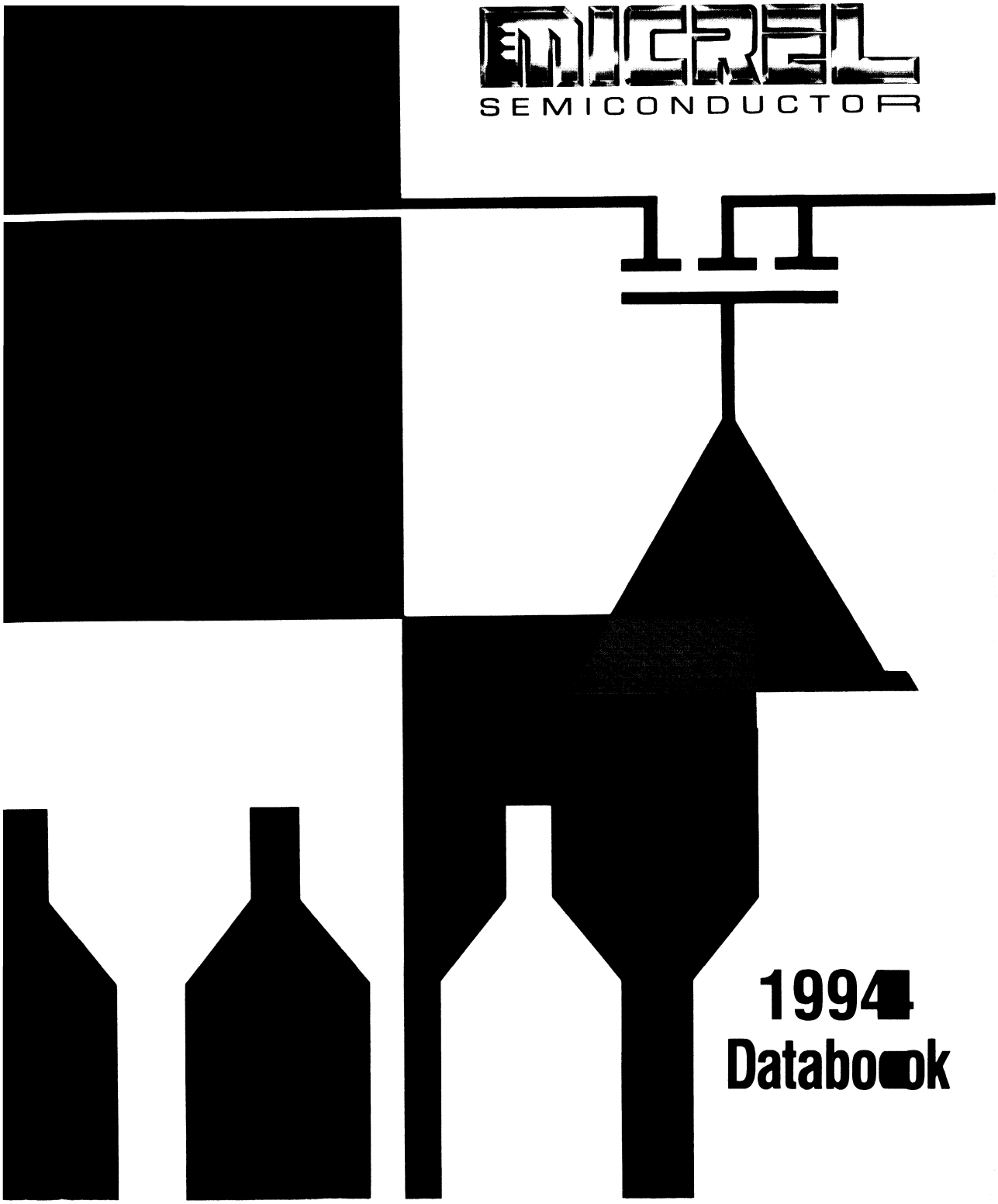
MICREL
SEMICONDUCTOR



1994 Databook

A CORPORATE COMMITMENT TO EXCELLENCE IN SUPPLYING HIGH PERFORMANCE ANALOG POWER ICs:

Micrel Semiconductor was founded in 1978 in the heart of "Silicon Valley". We are a profitable, self-funded, full service semiconductor company. All growth, product development, and acquisitions have been funded through retained earnings. Micrel is emerging as the new leader in power IC products. Our line of power MOSFET drivers, low drop out voltage regulators, and protected latched drivers is the most extensive in the industry.

Micrel's objective is to be a major supplier of high performance analog power ICs to the personal computer, telecommunications, industrial controls, automotive, medical equipment, office automation, avionics, and military markets. Our rapidly expanding standard product line complements our long standing semiconductor foundry and testing services business. This third edition of Micrel's Databook has expanded to almost three times the size of the first edition, including many new high performance analog power ICs such as power MOSFET drivers, protected power latched drivers, low drop-out linear and switching regulators, logic controlled power switches, and PCMCIA memory card support circuits. In addition to significant product line expansion, Micrel has received Standard Military Drawing (SMD) approval on several devices.

Micrel's TinyFET™ is an example of Micrel's leadership in technology: TinyFETs have the industry's lowest $R_{DS(ON)} \times$ die area product for any power P-channel MOSFET. Micrel's superb technology provides the *Micrel Advantage* to its products. Our class 10 wafer fabrication facility is second to none in the markets we serve.

"High Performance Analog Power" is the combining of low voltage linear and digital functions with high voltage, high current output devices. This allows for the further integration of functions heretofore handled primarily by modules and hybrids. By combining these low voltage and high voltage functions in a single monolithic IC, we have dramatically improved both reliability and packaging density. Micrel is dedicated to support this new and exciting high performance analog power semiconductor market. Whether your application is personal computers, telecommunications, industrial controls, automotive, medical equipment, office automation, avionics, or military, Micrel has the solution. We extensively test our products to insure they meet the highest standards of quality and reliability.

Micrel is proud of our success and have established a standard of business performance envied by others in the industry. We are dedicated to service and you have my personal commitment that Micrel will meet or exceed your strictest standard of excellence.

Ray Zinn

President and Chief Executive Officer

Micrel, Inc.

Micrel Semiconductor–your source for *High Performance Analog Power ICs*™

The information furnished by Micrel, Incorporated, in this publication is believed to be accurate and reliable. However, no responsibility is assumed by Micrel for its use, nor any infringements of patents or other rights of third parties resulting from its use. No license is granted by implication or otherwise under any patent or patent rights of Micrel, Inc. Micrel reserves the right to change circuitry and specifications at any time without prior notice.

PATENTS

Some products in this book are protected by one or more of the following patents: 4,914,546; 4,951,101; 4,979,001; 5,034,346; 5,045,966; 5,047,820; 5,254,486.

LIFE SUPPORT APPLICATIONS POLICY

Micrel products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of Micrel, Incorporated.

As used herein:

(I) Life support devices or systems are devices or systems which, (A) are intended for surgical implant into the body, or (B) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

(II) A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

Micrel Semiconductor
1994 Databook

Table of Contents

SECTION 1: GENERAL INFORMATION

SECTION 2: MOSFET DRIVERS

SECTION 3: LATCHED DRIVERS

Table of Contents

SECTION 4: DISPLAY DRIVERS

SECTION 5: HIGH VOLTAGE SEMICUSTOM POWER ARRAY

(continued)

* Summary information. For full details, contact Micrel.

Table of Contents

SECTION 6: LOW DROP-OUT LINEAR VOLTAGE REGULATORS

SECTION 7: SWITCH-MODE VOLTAGE REGULATORS

SECTION 8: OPEN DRAIN POWER SWITCHES

* Summary information. For full details, contact Micrel.

Table of Contents

* Summary information. For full details, contact Micrel.

TinyFET is a trademark of Micrel Inc.

SECTION 1: GENERAL INFORMATION

Introduction

Introduction

For years, the Micrel name was one of the best kept secrets in Silicon Valley. Working closely with several of the industries giants, Micrel quietly helped to develop specialized process and test techniques that have now become industry standards. Now the secret is out and Micrel is a name that is quickly becoming recognized around the world as the emerging leader in the field of high performance analog power ICs.

Micrel History

Since its founding in 1978 as an independent test facility of integrated circuits, Micrel has maintained a reputation for excellence, quality and customer responsiveness that is second to none.

In 1981 Micrel acquired its first independent semiconductor processing facility. Initially focusing on custom and specialty fabrication for other IC manufacturers, Micrel eventually expanded to develop its own line of semicustom and standard product Intelligent Power integrated circuits. In 1993, with the continued success of these ventures, a new 57,000 sq. ft. facility was acquired. This new Class 10 facility has allowed Micrel to extend its process and foundry capabilities with a full complement of CMOS/DMOS/Bipolar/NMOS/PMOS processes. Incorporating metal gate, silicon gate, dual metal, dual poly and features sizes down to 1.5 micron, Micrel is able to offer its customers unique design and fabrication tools.

The ability to combine high speed/high density digital, precision high performance analog and high voltage/high power devices all on the same monolithic circuit opened new frontiers in semiconductor design. One early example of this capability was the MPD8020 ASIS™ (Applications Specific Integrated System). This semicustom Intelligent Power Array allows users to economically design a proprietary IC by specifying the final interconnect pattern of an array of low voltage analog and logic CMOS along with customized high voltage PMOS and high voltage DMOS power drivers.

As Micrel moved forward towards its goal of becoming an independent supplier of integrated circuits, it expanded its base by entering into agreements to second source discontinued or follow-on products for several major manufacturers. This program has continued with Micrel currently producing circuits that can be found in a number of critical commercial and military applications. This includes the F-16, Hellfire missile, Standard Missile I, SINCGARS and many others. Many of these require radiation hardened products. Since 1987, Micrel has been the sole provider for both the CD4000 and MM54Cxx family of Radhard ICs.

Micrel Today and Beyond

Building on its strength as an innovator in process and test technology, Micrel has expanded and diversified its business by becoming the:

High Performance Analog Power I.C. Company

of the industry. The niche Micrel has carved for itself involves:

- **High Performance.....**precision voltages, high technology (Super ßeta PNP™ , patented circuit techniques, etc.) combined with the new safety features of over -current, over-voltage, and over-temperature protection
- **Analog.....**we control continuously varying outputs of voltage or current as opposed to digital ones and zeros (although we often throw in "mixed signal" i.e. analog with digital controls to bring out the best of both worlds)
- **Power I.C.s.....**our products involve high voltage, high current, or both

We use this expertise to address the following markets:

1. Power supplies
2. Battery powered computer, cellular phone, and handheld instruments
3. Industrial & display systems
4. Desktop computers
5. Aftermarket automotive
6. Avionics
7. Plus many others

The best kept secret in the Silicon Valley is a secret no longer.

Super ßeta PNP is a trademark of Micrel, Inc.

Alphanumeric Index

Alphanumeric Index

Alphanumeric Index

Alphanumeric Index

Ordering Information

Packaged Devices

MIC XXXX -01 A E B Q

Micrel
or Standard Prefix

Part Number

Speed /Bonding Option
only used when required

Temperature
A = –55°C to +125°C
B = –40°C to +85°C
C = 0°C to +70°C

Package
E = Ceramic Quad
F = Flat-Pack
J = Ceramic DIP
L = Leadless Chip Carrier
M = 150 mil body SOIC
M3 = SOT-23
M4 = SOT-143
N = Plastic DIP
Q = QFP
S = SOT-223
T = TO-220
U = TO-263
V = PLCC
WM = Wide 300 mil SOIC
Y = Dice
Z = TO-92

Screening Option
(None) = Industrial
B = Class B **S** = Class S

Qualification Option
H6 = Rad Hard, $1x10^6$ rad (Si)
Q = Class B or S

Die

MIC XXXX A Y P X

Micrel
or Industry Standard Prefix

Part Number

Quality
C: Commercial Visual
(0°C/+70°C design temperature)
A: Class B Visual, per Mil-Std-883/2010
(–55°C/+125°C design temperature)
Wafer Lot Traceability C of C, requires element evaluation, 883/5008, Class B
S: Class S visual per Mil-Std-883/2010
(–55°C/+125°C temperature)
Wafter Lot Traceability C of C, requires element evaluation, 883/5008, Class S and Wafer Lot Acceptance 883/5007

Package
Y: Die are 100% tested at 25°C

Element Evaluation
Die Form
W: Wafer Form
T: Sticky Tape
P: Waffle Pack

Special Processing
H: Radiation Wafer Lot Qualification
L: Backlapped
G: Backlapped and Gold Backed
HG: Rad Hard and Gold Backed

Micrel Semiconductor
1849 Fortune Drive
San Jose, CA 95131
Tel: (408) 944-0800 FAX: (408) 944-0970

Part Number Cross Reference

Part Number	*Micrel Replacement*
Allegro	
UCN4807A	*MIC4807BN*
UCN5800A	**MIC5800CN**
UCN5800L	**MIC5800BM**
UCN5800R	**MIC5800BJ**
UCN5801A	**MIC5801CN, MIC58P01,** *MIC59P50*
UCN5801EP	**MIC5801BV**
UCN5801R	**MIC5801BJ**
UCN5821A	**MIC5821CN**
UCN5822A	**MIC5822CN**
UCN5841A	**MIC5841CN, MIC58P42,** *MIC59P60*
UCN5841EP	**MIC5841BV**
UCN5841EPTR	**MIC5841BWM T&R**
UCN5841LW	**MIC5841BWM**
UCN5841LWTR	**MIC5841BWM T&R**
UCN5842A	**MIC5842CN, MIC58P42,** *MIC59P60*
UCN5842EP	**MIC5842BV**
UCN5842LW	**MIC5842BWM**
UCN5890A	**MIC5890BN**
UCN5891A	**MIC5891BN**
UCQ5800A	**MIC5800BN**
UCQ5801A	**MIC5801BN**
UCQ5801ABU	**MIC5801AJB**
UCQ5801R	**MIC5801BJ**
UCQ5821A	**MIC5821BN**
UCQ5821ABU	**MIC5821AJB**
UCQ5821R	**MIC5821BJ**
UCS5800H883	**MIC5800AJBQ (SMD 5962-8764002CX)**
UCS5801H883	**MIC5801AJBQ (SMD 5962-8764001WX)**
UCS5822H883	**MIC5822AJBQ (SMD 5962-8764101EX†)**
UCS5841H883	**MIC5841AJBQ**
Cherry Semiconductor	
CS2843AN8	**MIC38C43BN, MIC38HC43BN***
CS2843AD8	**MIC38C43BM, MIC38HC43BM***
CS2843AD14	**MIC38C43-1BM, MIC38HC43-1BM***
CS3842AN8	**MIC38C42N, MIC38HC42BN***
CS3842AD8	**MIC38C42BM, MIC38HC42BM***
CS3842AD14	**MIC38C42-1BM, MIC38HC42-1BM***
CS3843AN8	**MIC38C43BN, MIC38HC43BN***
CS3843AD8	**MIC38C43BM, MIC38HC43BM***
CS3843AD14	**MIC38C43-1BM, MIC38HC43-1BM***
Gould AMI	
S4520	**MIC8010** *MIC8030, MIC8031*
Holt	
HI-8010	**MIC8010** *MIC8030, MIC8031*
Intersil	
ICL7667	**MIC426, MIC1426, MIC4423, MIC4426**
Lansdale	
ML4350	**MIC4350**

† DESC approval pending

Part Number	*Micrel Replacement*
Linear Technology Corp.	
LT1241CJ8	**MIC38C45BJ, MIC38HC45BJ***
LT1241MJ8	**MIC18C45AJ, MIC18HC45AJ***
LT1241CN8	**MIC38C45BN, MIC38HC45BN***
LT1241CS8	**MIC38C45BM, MIC38HC45BM***
LT1242CJ8	**MIC38C42BJ, MIC38HC42BJ***
LT1242MJ8	**MIC18C42AJ, MIC18HC42AJ***
LT1242CN8	**MIC38C42BN, MIC38HC42BN***
LT1242CS8	**MIC38C42BM, MIC38HC42BM***
LT1243CJ8	**MIC38C43BJ, MIC38HC43BJ***
LT1243MJ8	**MIC18C43AJ, MIC18HC43AJ***
LT1243CN8	**MIC38C43BN, MIC38HC43BN***
LT1243CS8	**MIC38C43BM, MIC38HC43BM***
LT1244CJ8	**MIC38C44BJ, MIC38HC44BJ***
LT1244MJ8	**MIC18C44AJ, MIC18HC44AJ***
LT1244CN8	**MIC38C44BN, MIC38HC44BN***
LT1244CS8	**MIC38C44BM, MIC38HC44BM***
LT1245CJ8	**MIC38C45BJ, MIC38HC45BJ***
LT1245MJ8	**MIC18C45AJ, MIC18HC45AJ***
LT1245CN8	**MIC38C45BN, MIC38HC45BN***
LT1245CS8	**MIC38C45BM, MIC38HC45BM***
Maxim	
ICL7667	**MIC426, MIC1426, MIC4423, MIC4426**
MAX631ACPA	**MIC631BN***
MAX631BCPA	**MIC631BN***
MAX631ACSA	**MIC631BM***
MAX631BCSA	**MIC631BM***
MAX631AEPA	**MIC631BN****
MAX631BEPA	**MIC631BN***
MAX631AESA	**MIC631BM***
MAX631BESA	**MIC631BM***
MAX631AMJA	**MIC631AJ***
MAX631BMJA	**MIC631AJ***
MAX632ACPA	**MIC632BN***
MAX632BCPA	**MIC632BN***
MAX632ACSA	**MIC632BM***
MAX632BCSA	**MIC632BM***
MAX632AEPA	**MIC632BN***
MAX632BEPA	**MIC632BN***
MAX632AESA	**MIC632BM***
MAX632BESA	**MIC632BM***
MAX632AMJA	**MIC632AJ***
MAX632BMJA	**MIC632AJ***
MAX633ACPA	**MIC633BN***
MAX633BCPA	**MIC633BN***
MAX633ACSA	**MIC633BM***
MAX633BCSA	**MIC633BM***
MAX633AEPA	**MIC633BN***
MAX633BEPA	**MIC633BN***
MAX633AESA	**MIC633BM***
MAX633BESA	**MIC633BM***

Micrel **Equivalent** devices are shown in **boldface**.
Micrel *Similar Replacement* devices are shown in *italic*.
* Indicates Micrel Improved Version devices.

Part Number	*Micrel Replacement*
MAX633AMJA	**MIC633AJ***
MAX633BMJA	**MIC633AJ***
MAX641ACPA	**MIC641BN***
MAX641BCPA	**MIC641BN***
MAX641ACSA	**MIC641BM***
MAX641BCSA	**MIC641BM***
MAX641AEPA	**MIC641BN***
MAX641BEPA	**MIC641BN***
MAX641AESA	**MIC641BM***
MAX641BESA	**MIC641BM***
MAX641AMJA	**MIC641AJ***
MAX641BMJA	**MIC641AJ***
MAX642ACPA	**MIC642BN***
MAX642BCPA	**MIC642BN***
MAX642ACSA	**MIC642BM***
MAX642BCSA	**MIC642BM***
MAX642AEPA	**MIC642BN***
MAX642BEPA	**MIC642BN***
MAX642AESA	**MIC642BM***
MAX642BESA	**MIC642BM***
MAX642AMJA	**MIC642AJ***
MAX642BMJA	**MIC642AJ***
MAX643ACPA	**MIC643BN***
MAX643BCPA	**MIC643BN***
MAX643ACSA	**MIC643BM***
MAX643BCSA	**MIC643BM***
MAX643AEPA	**MIC643BN***
MAX643BEPA	**MIC643BN***
MAX643AESA	**MIC643BM***
MAX643BESA	**MIC643BM***
MAX643AMJA	**MIC643AJ***
MAX643BMJA	**MIC643AJ***
TSC426	**MIC426, MIC1426, MIC4423, MIC4426**
Motorola	
MC4350	**MIC4350**
MH0026	**MIC426, MIC1426, MIC4423, MIC4426**
UC2842AN	**MIC38C42BN, MIC38HC42BN***
UC2842AJ	**MIC38C42BJ, MIC38HC42BJ***
UC2842AD	**MIC38C42-1BM, MIC38HC42-1BM***
UC2843AN	**MIC38C43BN, MIC38HC43BN***
UC2843AJ	**MIC38C43BJ, MIC38HC43BJ***
UC2843AD	**MIC38C43-1BM, MIC38HC43-1BM***
UC3842AN	**MIC38C42BN, MIC38HC42BN***
UC3842AD	**MIC38C42-1BM, MIC38HC42-1BM***
UC3843AN	**MIC38C43BN, MIC38HC43BN***
UC3843AD	**MIC38C43-1BM, MIC38HC43-1BM***
National Semiconductor	
DS0026	**MIC426, MIC1426, MIC4423, MIC4426**
LM1575K-ADJ	**LM1575AK**
LM1575K-5.0	**LM1575-5.0AK**
LM1576	**LM1576**
LM2574M-5.0	**LM2574-5.0BWM**
LM2574M-12	**LM2574-12BWM**
LM2574M-15	**LM2574-15BWM**
LM2574M-ADJ	**LM2574BWM**
LM2574N-5.0	**LM2574-5.0BN**
LM2574N-12	**LM2574-12BN**
LM2574N-15	**LM2574-15BN**
LM2574N-ADJ	**LM2574BN**
LM2575M-ADJ	**LM2575BWM**
LM2575M-5.0	**LM2575-5.0BWM**
LM2575M-12	**LM2575-12BWM**
LM2575M-15	**LM2575-15BWM**

Part Number	*Micrel Replacement*
LM2575N-ADJ	**LM2575BN**
LM2575N-5.0	**LM2575-5.0BN**
LM2575N-12	**LM2575-12BN**
LM2575N-15	**LM2575-15BN**
LM2575T-ADJ	**LM2575BT**
LM2575T-5.0	**LM2575-5.0BT**
LM2575T-12	**LM2575-12BT**
LM2575T-15	**LM2575-15BT**
LM2576T-ADJ	**LM2576BT**
LM2576T-5.0	**LM2576-5.0BT**
LM2576T-12	**LM2576-12BT**
LM2576T-15	**LM2576-15BT**
LM2930T-5.0	**MIC2954-03BT***
LM2931AT-5.0	**MIC2954-03BT***
LM2931AZ-5.0	**MIC2950-06BZ***
LM2931T-5.0	**MIC2954-03BT***
LM2931Z-5.0	**MIC2950-06BT***
LM2937ET-5.0	**MIC2937A-5.0BT***
LM2937ET-12	**MIC2937A-12BT***
LM2937ET-15	**MIC2937A-15BT***
LM2940CT-5.0	**MIC2940A-5.0BT***
LM2940CT-12	**MIC2940A-12BT***
LM2940T-5.0	**MIC2940A-5.0BT***
LM2940T-12	**MIC2940A-12BT***
LM2941CT-5.0	**MIC2941ABT***
LM2941T-5.0	**MIC2941ABT***
LM4040...	**LM4040...**
LM4041...	**LM4041...**
LP2950ACZ-5.0	**LP2950-02BZ, MIC2950-05BZ***
LP2950CZ-5.0	**LP2950-03BZ, MIC2950-06BZ***
LP2951ACJ	**LP2951-02BJ, MIC2951-02BJ***
LP2951ACN	**LP2951-02BN, MIC2951-02BN***
LP2951AIT	**LP2954-02BT, MIC2954-05BT***
LP2951CJ	**LP2951-03BJ, MIC2951-03BJ***
LP2951CN	**LP2951-03BN, MIC2951-03BN***
LP2951IT	**LP2954-03BT, MIC2954-03BT***
LP2951J	**LP2951-01AJ, MIC2951-01AJ***
LP2954AIT	**MIC2954-02BT***
LP2954IT	**MIC2954-03BT***
MM5450	**MM5450**
MM5451	**MM5451**
NHM0026	**MIC426, MIC1426, MIC4423, MIC4426**
Semtech	
LM1576K-ADJ	**LM1576AK**
LM1576K-3.3	**LM1576-3.3AK**
LM1576K-5.0	**LM1576-5.0AK**
LM1576K-12	**LM1576-12AK**
LM1576K-15	**LM1576-15AK**
LM2575T-ADJ	**LM2575BT**
LM2575T-3.3	**LM2575-3.3BT**
LM2575T-5.0	**LM2575-5.0BT**
LM2575T-12	**LM2575-12BT**
LM2575T-15	**LM2575-15BT**
LM2575N-ADJ	**LM2575BN**
LM2575N-3.3	**LM2575-3.3BN**
LM2575N-5.0	**LM2575-5.0BN**
LM2575N-12	**LM2575-12BN**
LM2575N-15	**LM2575-15BN**
LM2575M-ADJ	**LM2575BWM**
LM2575M-3.3	**LM2575-3.3BWM**

Micrel **Equivalent** devices are shown in **boldface**.
Micrel *Similar Replacement* devices are shown in *italic*.
* Indicates Micrel Improved Version devices.

Part Number	*Micrel Replacement*
LM2575M-5.0	**LM2575-5.0BWM**
LM2575M-12	**LM2575-12BWM**
LM2575M-15	**LM2575-15BWM**
LM2576K-ADJ	**LM2576AK**
LM2576K-3.3	**LM2576-3.3AK**
LM2576K-5.0	**LM2576-5.0AK**
LM2576K-12	**LM2576-12AK**
LM2576K-15	**LM2576-15AK**
LM2576T-ADJ	**LM2576BT**
LM2576T-3.3	**LM2576-3.3BT**
LM2576T-5.0	**LM2576-5.0BT**
LM2576T-12	**LM2576-12BT**
LM2576T-15	**LM2576-15BT**
SGS	
M5450	**MM5450**
M5451	**MM5451**
SGS1626/2626/3626	**MIC426, MIC1426, MIC4423, MIC4426**
Silicon General	
SG1626/2626/3626	**MIC426, MIC1426, MIC4423, MIC4426**
SG1644/2644/3644	**MIC426, MIC1426, MIC4423, MIC4426**
Siliconix	
SG1626/2626/3626	**MIC426, MIC1426, MIC4423, MIC4426**
Teledyne	
TSC426	**MIC426**
TSC427	**MIC427**
TSC428	**MIC428**
TSC1426	**MIC1426**
TSC1427	**MIC1427**
TSC1428	**MIC1428**
TSC18C42MJA883	**MIC18C42AJB, MIC18HC42AJB***
TSC18C43MJA883	**MIC18C43AJB, MIC18HC43AJB***
TSC18C44MJA883	**MIC18C44AJB, MIC18HC44AJB***
TSC18C45MJA883	**MIC18C45AJB, MIC18HC45AJB***
TSC18C42MJA	**MIC18C42AJ, MIC18HC42AJ***
TSC18C43MJA	**MIC18C43AJ, MIC18HC43AJ***
TSC18C44MJA	**MIC18C44AJ, MIC18HC44AJ***
TSC18C45MJA	**MIC18C45AJ, MIC18HC45AJ***
TSC18HC42MJA883	**MIC18HC42AJB***
TSC18HC43MJA883	**MIC18HC43AJB***
TSC18HC44MJA883	**MIC18HC44AJB***
TSC18HC45MJA883	**MIC18HC45AJB***
TSC18HC42MJA	**MIC18HC42AJ***
TSC18HC43MJA	**MIC18HC43AJ***
TSC18HC44MJA	**MIC18HC44AJ***
TSC18HC45MJA	**MIC18HC45AJ***
TSC28C42EJA	**MIC38C42BJ, MIC38HC42BJ***
TSC28C43EJA	**MIC38C43BJ, MIC38HC43BJ***
TSC28C44EJA	**MIC38C44BJ, MIC38HC44BJ***
TSC28C45EJA	**MIC38C45BJ, MIC38HC45BJ***
TSC28C42EPA	**MIC38C42BN, MIC38HC42BN***
TSC28C43PA	**MIC38C43BN, MIC38HC43BN***
TSC28C44EPA	**MIC38C44BN, MIC38HC44BN***
TSC28C45EPA	**MIC38C45BN, MIC38HC45BN***
TSC28HC42EJA	**MIC38HC42BJ***
TSC28HC43EJA	**MIC38HC43BJ***
TSC28HC44EJA	**MIC38HC44BJ***
TSC28HC45EJA	**MIC38HC45BJ***
TSC28HC42EPA	**MIC38HC42BN***
TSC28HC43PA	**MIC38HC43BN***
TSC28HC44EPA	**MIC38HC44BN***
TSC28HC45EPA	**MIC38HC45BN***
TSC38C42CPA	**MIC38C42BN, MIC38HC42BN***
TSC38C43CPA	**MIC38C43BN, MIC38HC43BN***
TSC38C44CPA	**MIC38C44BN, MIC38HC44BN***
TSC38C45CPA	**MIC38C45BN, MIC38HC45BN***
TSC38HC42CPA	**MIC38HC42BN***
TSC38HC43CPA	**MIC38HC43BN***
TSC38HC44CPA	**MIC38HC44BN***
TSC38HC45CPA	**MIC38HC45BN***
TSC4401	**MIC4401**
TSC4403	**MIC4403**
TSC4404	*MIC4604*
TSC4405	*MIC4605*
TSC4406	*MIC4606*
TSC4407	*MIC4607*
TSC4408	*MIC4608*
TSC4409	*MIC4609*
TSC4420	**MIC4420**
TSC4421	**MIC4421**
TSC4422	**MIC4422**
TSC4423	**MIC4423**
TSC4424	**MIC4424**
TSC4425	**MIC4425**
TSC4426	**MIC4426**
TSC4427	**MIC4427**
TSC4428	**MIC4428**
TSC4429	**MIC4429**
TSC4467	**MIC4467**
TSC4468	**MIC4468**
TSC4469	**MIC4469**
Toshiba	
TC5002B	**MIC5002**
Unitrode	
UC1576K-ADJ	**LM1576AK**
UC1576K-5.0	**LM1576-5.0AK**
UC1576K-12	**LM1576-12AK**
UC1576K-15	**LM1576-15AK**
UC1842AJ	**MIC18C42BJ, MIC18HC42BJ***
UC1843AJ	**MIC18C43BJ, MIC18HC43BJ***
UC1844AJ	**MIC18C44BJ, MIC18HC44BJ***
UC1845AJ	**MIC18C45BJ, MIC18HC45BJ***
UC2575T	**LM2575-5.0BT**
UC2576T-ADJ	**LM2576BT**
UC2576T-5.0	**LM2576-5.0BT**
UC2576T-12	**LM2576-12BT**
UC2576T-15	**LM2576-15BT**
UC2842AN	**MIC38C42BN, MIC38HC42BN***
UC2843AN	**MIC38HC43BN, MIC38HC43BN***
UC2844AN	**MIC38C44BN, MIC38HC44BN***
UC2845AN	**MIC38C45BN, MIC38HC45BN***
UC3842AN	**MIC38C42BN, MIC38HC42BN***
UC3843AN	**MIC38C43BN, MIC38HC43BN***
UC3844AN	**MIC38C44BN, MIC38HC44BN***
UC3845AN	**MIC38C45BN, MIC38HC45BN***

Micrel **Equivalent** devices are shown in **boldface**.
Micrel *Similar Replacement* devices are shown in *italic*.
* Indicates Micrel Improved Version devices.

Quality/Reliability Program

Our Philosophy

Product quality and reliability are two of the most critical elements for achieving success in today's semiconductor industry. Micrel has attained success as a semiconductor supplier by designing and processing parts that meet the most strenuous applications and most adverse environments. Micrel has accomplished this by never wavering from the philosophy that quality must be built into each and every device and process.

Micrel considers product reliability to be an expression of the quality philosophy extended over the expected life of each product. Micrel's philosophy begins in the design stage and continues, under strict monitoring and control, throughout the development, production, testing and packaging of each product.

Micrel's specific goal is to produce devices that are without defect from their given specifications for performance and product life. Product testing and comparative studies are ongoing activities at Micrel as we continue our search for new and more effective methods for manufacturing products with built-in quality. The Micrel quality program is in full compliance with MIL-I-45208, MIL-STD-883 paragraph 1.2.1 compliant non-JAN devices, and equipment calibration meets all requirements of MIL-STD-45662.

Quality Program Elements

Quality and reliability in Micrel products are obtained through a number of quality assurance program elements, most of which contain multiple levels of requirements and procedures. These program elements comprise the Micrel Quality Assurance Program.

I. Supplier requirements

Vendor certification of compliance to published specifications is required for process materials, gasses, substrates, masks, etc., as well as for components, parts and materials used in assembly.

II. Fabrication QA is based on a Statistical Process Control (SPC) Program including:

1. Test procedures
2. Document control
   - Specifications/recipes
   - Process change notice (PCN)
   - Engineering change notice (ECN)
3. Critical process-step monitoring
   - Particulates
   - Critical dimensions
   - Electrical performance
4. Extended SPC programs
   - Process Limit Control (PLC)
   - Process on Exception (POE)
5. Outgoing QA
   - Visual Inspection
   - To Micrel Standards
   - To Mil-883 Class B or Class S Requirements

III. Vendor Requirements

Certification of compliance to published Micrel or customer specifications is required for processes, materials, and services from third-party vendors.

IV. Assembly QA Program

1. Test procedures
2. Document control
   - Specifications
   - Control systems
   - Engineering change notices (ECN)
3. Critical-step monitoring
   - Assembly processes
   - Critical dimensions
   - Environmental processes
4. Acceptance Test Procedure
   - Electrical performance
   - Component marking
5. Outgoing QA
   - Visual Inspection
   - To Micrel Standards
   - To Mil-883 Class B or Class S Requirements

Organization

At Micrel, quality assurance management reports directly to the President of the corporation. All quality and reliability issues are independent of the production organizations.

The QA Manager's responsibilities are to establish and maintain effective controls for monitoring Micrel manufacturing and test services, equipment and processes (as well as our suppliers and contractors), to report the findings to the President, and to initiate statistically valid techniques to further improve Micrel quality and reliability levels.

The QA Manager is responsible for implementation and administration of multiple quality-related programs and systems for both commercial and military grade processes and products. Activities under the QA Manager's control include: incoming inspection, in-process quality control, qualification testing, conformance testing, document control, specification review, failure analysis, internal audit, quality procedures training, and ongoing vendor qualification and performance appraisal.

Statistical Process Control

Foremost of the Micrel quality assurance programs is their Statistical Process Control (SPC) methodology. Because of the company's unique mix of proprietary, custom and foundry products, SPC at Micrel is approached on two levels.

Level 1 Traditional SPC utilizing process capability studies, design of experiments, Paretto analysis, histograms and X-bar R charting of critical process steps.

Level 2 Extended SPC methodology adds Process Limit Control (PLC) and Process on Exception (POE) programs as sub-sets to the standard SPC programs.

Micrel's Process Limit Control (PLC) program provides absolute control of wafer runs during processing. Parameters are measured and recorded at every process steps against established limits. When any measurement value is found to exceed a specification limit, the run is immediately stopped and process engineering is notified. Before the run can proceed, engineering must evaluate the data and determine the run disposition during that production shift.

The Process on Exception (POE) program monitors and controls wafers during electrical testing. Wafer probe results are compared against specifications. Any exceptions to either absolute, preferred, or target specifications are noted and detailed reports are generated. Engineering may then exercise some influence over yield issues by determining which electrical performance criteria are critical.

The results of SPC, PLC and POE performance monitoring are reviewed on a monthly basis. Trends are charted, corrective actions are evaluated and process improvements are implemented as a result of the data.

Document Control

Document control is an integral part of the Micrel quality assurance program. It is designed to assure that operating procedures and customer requirements are translated into regulatory written instructions. Document control is responsible for initiating, approving, distributing, revising, recalling, and archiving internal control systems in the form of product run sheets (recipes), process and test specifications, etc.

Micrel's two main specification control methodologies utilize engineering change notice (ECN) and process change notice (PCN) systems.

ECN The engineering change notice system follows standard industry procedures for process and test specifications, travelers, forms, and drawings.

PCN The process change notice system is an extension of Micrel's unique, highly-detailed product run sheet (recipe) control system. PCN mechanisms meet the extreme demands for accuracy required in wafer processing.

Packaged product quality is controlled by a detailed set of instructions that are issued and controlled as part of the ECN system. These instructions cover all assembly and back-end processing steps and include the build-diagram, burn-in drawing, test set-up specification, test traveler, etc.

Inspection and Test Points

The flow charts accompanying this section describe the sequential steps of semiconductor processing and fabrication, and the associated test or inspection procedures and documentation.

Equipment Calibration

Micrel maintains a calibration system that conforms to MIL-STD-45662 and ensures measurement accuracy of equipment used to determine product workmanship and acceptability. Major provisions of the program include:

- Qualification of external calibration services,
- References traceable to National Institute of Standards and Technology (NIST). Identification of measurement and test equipment for type (electrical, mechanical, and optical) and frequency of calibration
- Certification history of equipment calibration and recall
- Recall status report history
- Audit history (calibration date stickers and recall designation)

Quality Control

The quality control program includes multiple inspections of material in-process, as well as final acceptance inspection of outgoing finished products. The QC system comprises product integrity characterizations of dimensional, structural, electrical and visual parameters. It also includes environmental and procedural monitoring checks.

The program elements include, but are not necessarily limited to:

- Particulate monitoring
- Temperature and relative humidity monitoring
- Electrostatic discharge monitoring and control
- Specification compliance reviews
- Random monitoring of wafers in-process
- Critical dimension qualification of product lot samples
- Wafer/die electrical sort
- Performance/trend data analysis
- Storage, handling, packaging and identification of raw materials, work-in-progress, and finished goods
- Returned material analysis

Finished product is inspected and tested prior to its shipment to the customer. Random sampling methodology is used to check deliverable wafer, die or part quality against published Micrel workmanship standards and customer specifications.

This final-product quality control program includes systems and procedures that assure the following:

- Correlation and qualification of test equipment to internal and customer specifications
- Manufacturing test operations are proper and complete
- Product lots conform to detailed test requirements for visual, mechanical and electrical performance criteria
- Documentation for each product/lot is proper and complete

New Products and Processes

New products or major process changes must undergo complete evaluation before they are certified at Micrel. Quality Assurance participation and approval is required in new product design reviews, product characterization and reliability studies, and documentation preparation.

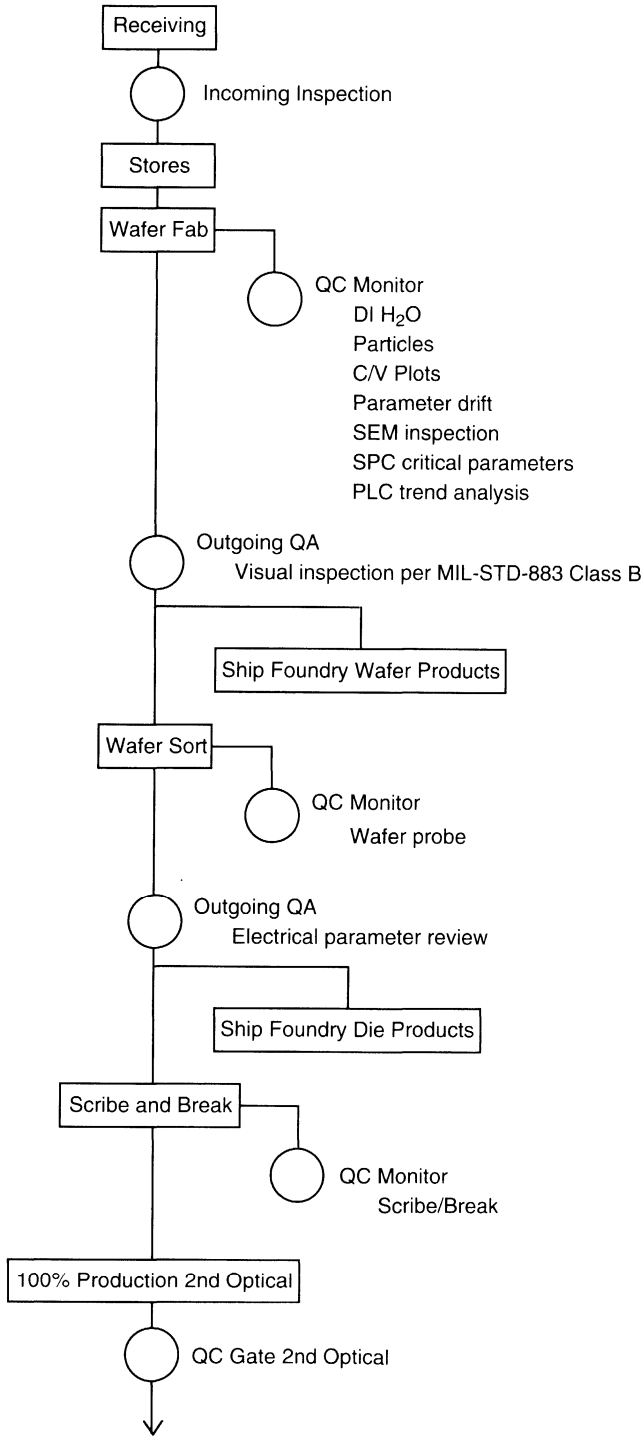
Certification is granted to new products or processes only after rigorous stress-testing, thorough monitoring of critical dimensions, careful failure analysis, and full process/trend data review. New packages are qualified and released for production only after Quality Assurance has determined that all environmental, mechanical and electrical tests are satisfactorily completed.

Complete and proper documentation of all material, process, procedure or packaging changes is required for final Quality Assurance certification.

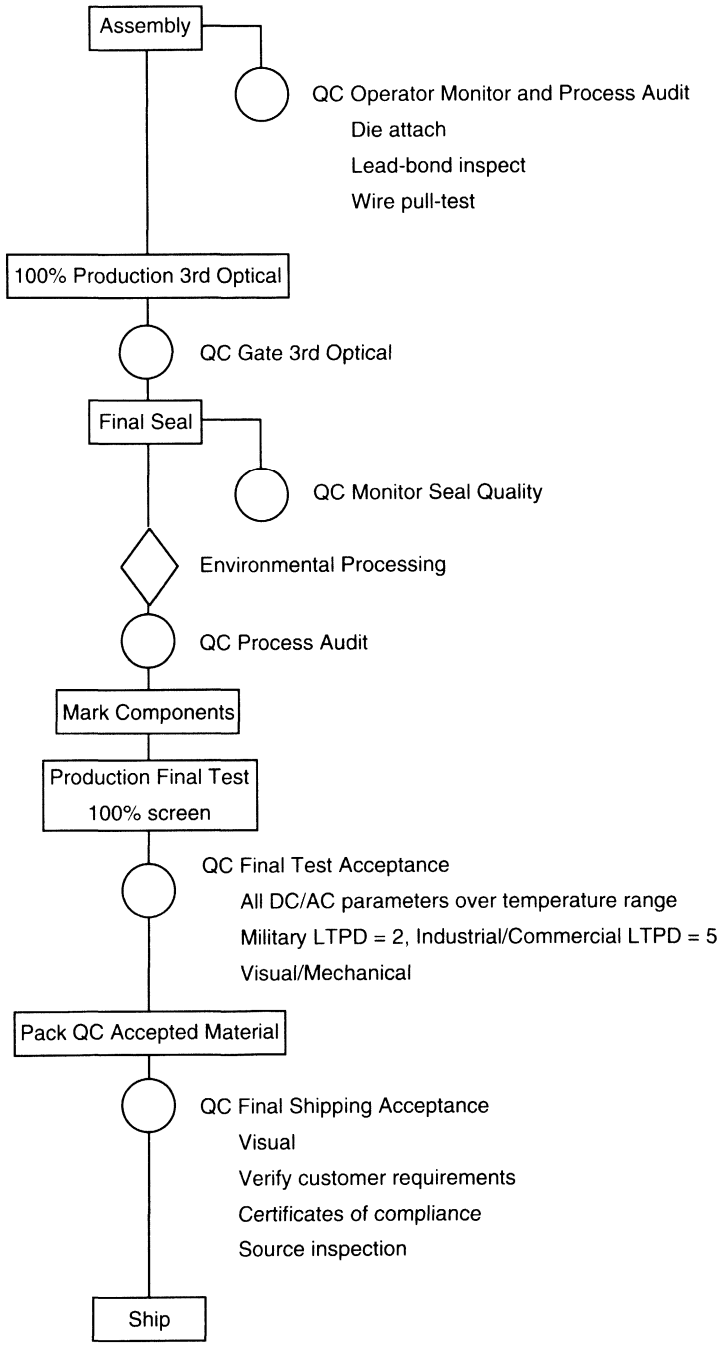
Summary

The Micrel Quality Assurance philosophy — that quality must be built into every process and product — is realized by the company's thorough implementation of the policies, procedures and processes required to ensure that our products and services meet the highest standards for material and workmanship.

Micrel Quality Flow for Semiconductor Circuit Manufacturing



Micrel Quality Flow for Semiconductor Assembly



Customer Returns

Perform analysis, answer and/or generate corrective action request, make disposition of return.

Specification Review

Review internal specifications, verify agreement to customer requirements, issue specification to production.

Reliability Assurance

Qualification — Test each device family in accordance with MIL-STD-883, Method 5004 and 5005, Class B reequirements.

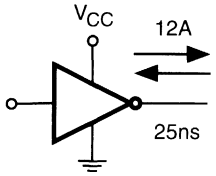
Certification — New products and major process changes subjected to accelerated test and process analysis.

Failure Analysis — Performed on all Qualification and Process Monitor failures and customer returns as needed.

Document Control — Maintains files of all latest drawings and specifications, controls and issues wafer run-sheets, specifications, drawings and ECN numbers, distributes copies to specification control books and user groups.

SECTION 2: MOSFET DRIVERS

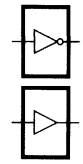
MOSFET Driver Selection Guide



1500pF to 62,000pF

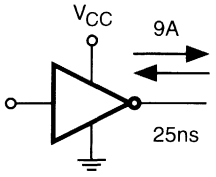
MIC4451/4452

- 12A Peak Output
- 0.8Ω Output Impedance
- 25ns into 15,000pF
- 4.5V to 18V Supply
- Latch-up Protected
- Withstands 5V Negative Swing
- Surface Mount and High Power Package Available



MIC4451

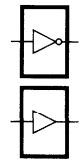
MIC4452



1500pF to 47,000pF

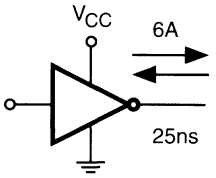
MIC4421/4422

- 9A Peak Output
- 1.0Ω Output Impedance
- 25ns into 10,000pF
- 4.5V to 18V Supply
- Latch-up Protected
- Withstands 5V Negative Swing
- Surface Mount and High Power Package Available



MIC4421

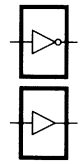
MIC4422



Drives a hex 6—hex 7 size
MOSFET: 1500pF to 16,000pF

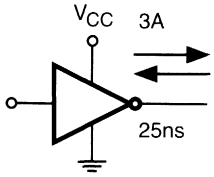
MIC4420/4429

- 6A Peak Output
- 2.5Ω Output Impedance
- 4.5V to 18V Supply
- 25ns into 2500pF
- Latch-up Protected
- Withstands 5V Negative Swing
- Surface Mount and High Power Package Available



MIC4429

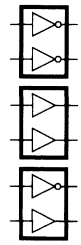
MIC4420



Drives a hex 4—hex 5 size
MOSFET: 6000pF to 12,000pF

MIC4423/4424/4425

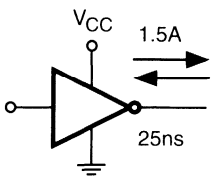
- 3A Peak Output
- 3.5Ω Output Impedance
- 25ns into 1800pF
- 4.5V to 18V Supply
- Latch-up Protected
- Withstands 5V Negative Swing
- Surface Mount Available



MIC4423

MIC4424

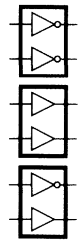
MIC4425



Drives a hex 0—hex 3 size
MOSFET: 400pF to 3000pF

MIC4426/4427/4428

- 1.5A Peak Output
- 7Ω Output Impedance
- 25ns into 1000pF
- 4.5V to 18V Supply
- Latch-up Protected
- Withstands 5V Negative Swing
- Surface Mount Available

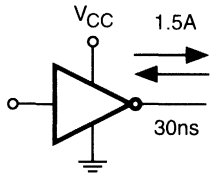


MIC4426

MIC4427

MIC4428

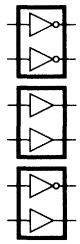
MOSFET Driver Selection Guide



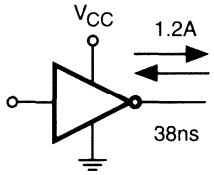
Drives a hex 0—hex 3 size
MOSFET: 400pF to 3000pF

MIC426/427/428

- 1.5A Peak Output
- 6Ω Output Impedance
- 30ns into 1000pF
- 4.5V to 18V Supply
- Surface Mount Available



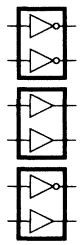
MIC426
MIC427
MIC428



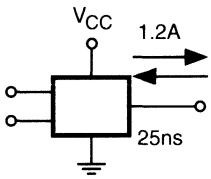
Drives a hex 0—hex 3 size
MOSFET: 400pF to 3000pF

MIC1426/1427/1428

- 1.2A Peak Output
- 8Ω Output Impedance
- 38ns into 1000pF
- 4.75V to 16V Supply
- Low Cost Predriver
- Surface Mount Available



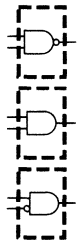
MIC1426
MIC1427
MIC1428



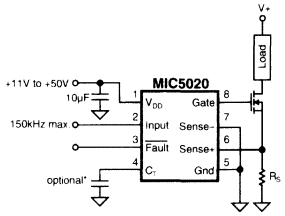
Drives a hex 0—hex 3 size
MOSFET: 400pF to 3000pF

MIC4467/4468/4469

- 1.2A Peak Output
- 10Ω Output Impedance
- 25ns into 470pF
- 4.5V to 18V Supply
- Latch-up Protected
- Withstands 5V Negative Swing
- Surface Mount Available
- Three Logic Choices



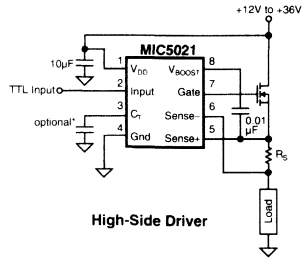
MIC4467
MIC4468
MIC4469



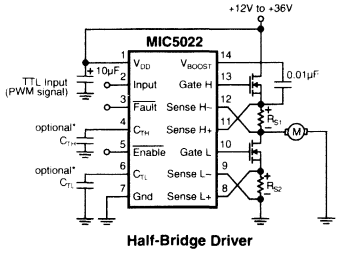
Low-Side Driver

MIC5020/5021

- 11V to 50V Supply (MIC5020)
- 12V to 36V Supply (MIC5021)
- 175ns into 2000pF (MIC5020)
- 550ns into 2000pF (MIC5021)
- Programmable Overcurrent Shutdown
- Internal Charge Pump
- Surface Mount Available



High-Side Driver

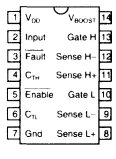


Half-Bridge Driver

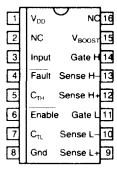
MIC5022

- 12V to 36V Supply
- 500ns into 1000pF
- Programmable Overcurrent Shutdown
- Internal Charge Pump
- Surface Mount Available

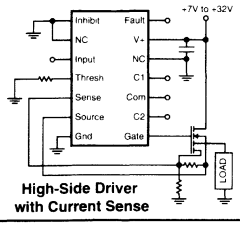
14-pin DIP



16-pin SOIC



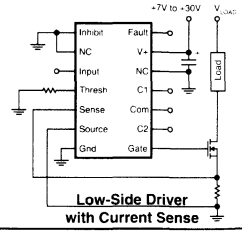
MOSFET Driver Selection Guide



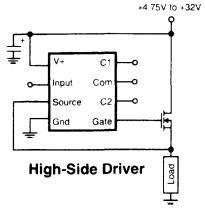
High-Side Driver with Current Sense

MIC5010

- 60µs into 1nF
- 7 to 32V Supply
- Full-featured Predriver
- Optional Speed-up Capacitors
- Internal Charge Pump
- Dynamic Sensing Threshold
- Surface Mount Available



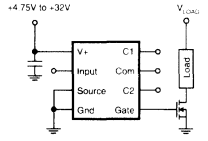
Low-Side Driver with Current Sense



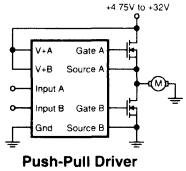
High-Side Driver

MIC5011

- 60µs into 1nF
- 4.5 to 32V Supply
- Minimum Parts Count
- Optional Speed-up Capacitors
- Internal Charge Pump
- Surface Mount Available



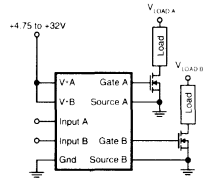
Low-Side Driver



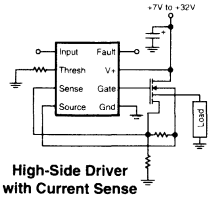
Push-Pull Driver

MIC5012

- 60µs into 1nF
- 4.75 to 32V Supply
- Dual Predriver
- Provides High and Low Side drive for H-bridge
- Internal Charge Pump
- Surface Mount Available



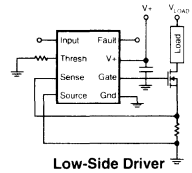
Dual Low-Side Driver



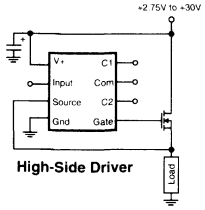
High-Side Driver with Current Sense

MIC5013

- 60µs into 1nF
- 7 to 32V Supply
- Overcurrent Sensing
- Internal Charge Pump
- Dynamic Sensing Threshold
- Surface Mount Available



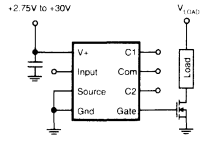
Low-Side Driver with Current Sense



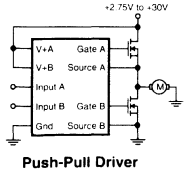
High-Side Driver

MIC5014/5015

- 2.75 to 30V Supply
- Minimum Parts Count
- "Load Dump" Protected
- Reverse Battery Protected to –20V
- Internal Charge Pump
- Surface Mount Available
- * Low Cost



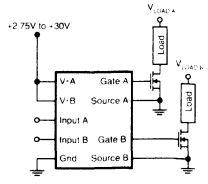
Low-Side Driver



Push-Pull Driver

MIC5016/5017

- 2.75 to 30V Supply
- Minimum Parts Count
- "Load Dump" Protected
- Reverse Battery Protected to –20V
- Internal Charge Pump
- Surface Mount Available
- Low Cost



Dual Low-Side Driver

MIC426/427/428

Dual Power MOSFET Driver

Bipolar/CMOS/DMOS Process

General Description

The MIC426/427/428 are dual high speed drivers. A TTL/CMOS input voltage level is translated into an output voltage level swing equalling the supply. The DMOS output will be within 25mV of ground or positive supply. Bipolar designs are capable of swinging only within 1 volt of the supply.

The low impedance high current driver outputs will swing a 1000pF load 18V in 30ns. The unique current and voltage drive qualities make the MIC426/427/428 ideal power MOSFET drivers, line drivers and DC to DC converter building blocks.

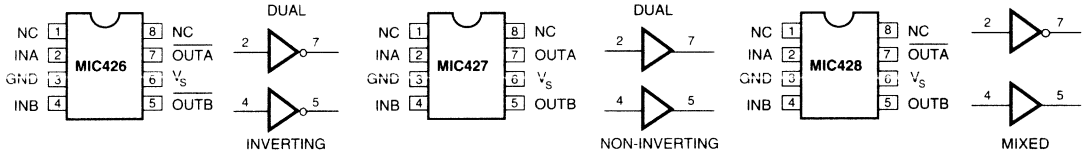
Input logic signals may equal the power supply voltage. Input current is a low 1µA making direct interface to CMOS/BIPOLAR switch mode power supply control integrated circuits possible as well as open collector analog comparators.

Features

- High Speed Switching (C_L = 1000pF) 30ns
- High Peak Output Current 1.5A
- High Output Voltage Swing ..... V_S – 25mV
  GND + 25mV
- Low Input Current (Logic "0" or "1") 1µA
- Low Equivalent Input Capacitance (typ) 6pF
- TTL/CMOS Input Compatible
- Available in Inverting & Non-Inverting Configurations
- Wide Operating Supply Voltage ..... 4.5V to 18V
- Low Power Consumption
  (Inputs Low) 0.4mA
  (Inputs High) 8mA
- Single Supply Operation
- Low Output Impedance (typ) 6Ω
- Pin Out Equivalent to DS0026 & MMH0026

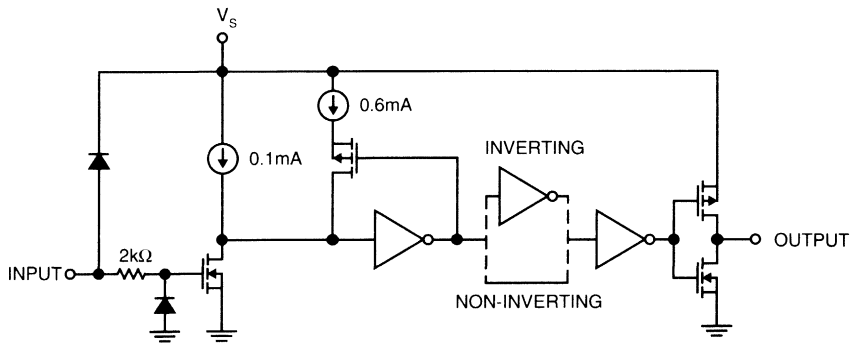
2

Pin Configuration



Functional Diagram

Integrated Component Count:
4 Resistors
4 Capacitors
52 Transistors



Functional Diagram for One Driver (Two Drivers per Package—Ground Unused Drivers)

Quiescent power supply current is 8mA maximum. The MIC426 requires 1/5 the current of the pin compatible bipolar DS0026 device. This is important in DC to DC converter applications with power efficiency constraints and high frequency switch mode power supply applications. Quiescent current is typically 6mA when driving a 1000pF load 18V at 100kHz.

The inverting MIC426 driver is pin compatible with the bipolar DS0026 and MMH0026 devices. The MIC427 is non-inverting; the MIC428 contains an inverting and non-inverting driver.

Ordering Information

Part Number	Temperature Range	Package	Configuration
MIC426CM MIC426BM	0°C to +70°C –40°C to +85°C	8-pin SOIC	Dual Inverting
MIC426CN MIC426BN	0°C to +70°C –40°C to +85°C	8-pin plastic DIP	Dual Inverting
MIC426AJ MIC426AJBQ*	–55°C to +125°C –55°C to +125°C	8-pin CerDIP	Dual Inverting SMD#5962-8850301PX
MIC426CY	—	CHIP	Dual Inverting
MIC427CM MIC427BM	0°C to +70°C –40°C to +85°C	8-pin SOIC	Dual Non-Inverting
MIC427CN MIC427BN	0°C to +70°C –40°C to +85°C	8-pin plastic DIP	Dual Non-Inverting
MIC427AJ MIC427AJBQ*	–55°C to +125°C –55°C to +125°C	8-pin CerDIP	Dual Non-Inverting SMD#5962-8850302PX
MIC427CY	—	CHIP	Dual Non-Inverting
MIC428CM MIC428BM	0°C to +70°C –40°C to +85°C	8-pin SOIC	Non-Inv. & Inverting
MIC428CN MIC428BN	0°C to +70°C –40°C to +85°C	8-pin plastic DIP	Non-Inv. & Inverting
MIC428AJ MIC428AJBQ*	–55°C to +125°C –55°C to +125°C	8-pin CerDIP	Non-Inv. & Inverting SMD#5962-8850303PX
MIC428CY	—	CHIP	Non-Inv. & Inverting

* AJB indicates units screen to MIL-STD 883, Method 5004, condition B, and burned-in for 1 week. Use SMD (Standard Military Drawing) number for ordering.

Absolute Maximum Ratings (Notes 1, 2, and 3)

If Military/Aerospace specified devices are required, contact Micrel for availability and specifications.

Supply Voltage	20V
Input Voltage Any Terminal	V_S + 0.3V to GND – 0.3V
Maximum Chip Temperature	150°C
Storage Temperature	–65°C to 150°C
Lead Temperature (10 sec)	300°C
Package Thermal Resistance	
CerDIP $R_{\theta J-A}$ (°C/W)	100
CerDIP $R_{\theta J-C}$ (°C/W)	50
PDIP $R_{\theta J-A}$ (°C/W)	130
PDIP $R_{\theta J-C}$ (°C/W)	42
SOIC $R_{\theta J-A}$ (°C/W)	120
SOIC $R_{\theta J-C}$ (°C/W)	75
Operating Temperature Range	
C Version	0°C to +70°C
B Version	–40°C to +85°C
A Version	–55°C to +125°C

MIC426/427/428 Electrical Characteristics: T_A = 25°C with 4.5V ≤ V_S ≤ 18V unless otherwise specified.

No.	Symbol	Parameter	Conditions	Min	Typ	Max	Units
INPUT							
1	V_{IH}	Logic 1 Input Voltage		2.4	1.4		V
2	V_{IL}	Logic 0 Input Voltage			1.1	0.8	V
3	I_{IN}	Input Current	$0 \le V_{IN} \le V_S$	–1		1	µA
OUTPUT							
4	V_{OH}	High Output Voltage		V_S–0.025			V
5	V_{OL}	Low Output Voltage				0.025	V
6	R_O	Output Resistance	V_{IN} = 0.8V I_{OUT} = 10mA, V_S = 18V		6	15	Ω
7	R_O	Output Resistance	V_{IN} = 2.4V I_{OUT} = 10mA, V_S = 18V		6	10	Ω
8	I_{PK}	Peak Output Current			1.5		A
SWITCHING TIME							
9	T_R	Rise Time	Test Figures 1, 2		18	30	ns
10	T_F	Fall Time	Test Figures 1, 2		15	20	ns
11	T_{D1}	Delay TIme	Test Figures 1, 2		17	40	ns
12	T_{D2}	Delay Time	Test Figures 1, 2		23	75	ns
POWER SUPPLY							
13	I_S	Power Supply Current	V_{IN} = 3.0V (Both Inputs)		1.4	8.0	mA
14	I_S	Power Supply Current	V_{IN} = 0.0V (Both Inputs)		0.18	0.4	mA

MIC426/427/428 Electrical Characteristics:

Over operating temperature range with 4.5V ≤ V_S ≤ 18V unless otherwise specified.

No.	Symbol	Parameter	Conditions	Min	Typ	Max	Units
INPUT							
1	V_{IH}	Logic 1 Input Voltage		2.4	1.5		V
2	V_{IL}	Logic 0 Input Voltage			1.0	0.8	V
3	I_{IN}	Input Current	$0 \le V_{IN} \le V_S$	–10		10	µA

MIC426/427/428 Electrical Characteristics:

Over operating temperature range with 4.5V ≤ V_S ≤ 18V unless otherwise specified (Continued).

No.	Symbol	Parameter	Conditions	Min	Typ	Max	Units
OUTPUT							
4	V_{OH}	High Output Voltage		V_S–0.025			V
5	V_{OL}	Low Output Voltage				0.025	V
6	R_O	Output Resistance	V_{IN} = 0.8V I_{OUT} = 10mA, V_S = 18V		8	20	Ω
7	R_O	Output Resistance	V_{IN} = 2.4V I_{OUT} = 10mA, V_S = 18V		10	15	Ω
SWITCHING TIME							
8	T_R	Rise Time	Test Figures 1, 2		20	60	ns
9	T_F	Fall Time	Test Figures 1, 2		29	40	ns
10	T_{D1}	Delay TIme	Test Figures 1, 2		19	60	ns
11	T_{D2}	Delay Time	Test Figures 1, 2		27	120	ns
POWER SUPPLY							
12	I_S	Power Supply Current	V_{IN} = 3.0V (Both Inputs)		1.5	12.0	mA
13	I_S	Power Supply Current	V_{IN} = 0.0V (Both Inputs)		0.19	0.6	mA

Note 1: Functional operation above the absolute maximum stress ratings is not implied.

Note 2: Static Sensitive device (above 2kV). Unused devices must be stored in conductive material to protect devices from static discharge and static fields.

Note 3: Switching times guaranteed by design.

Switching Time Test Circuits

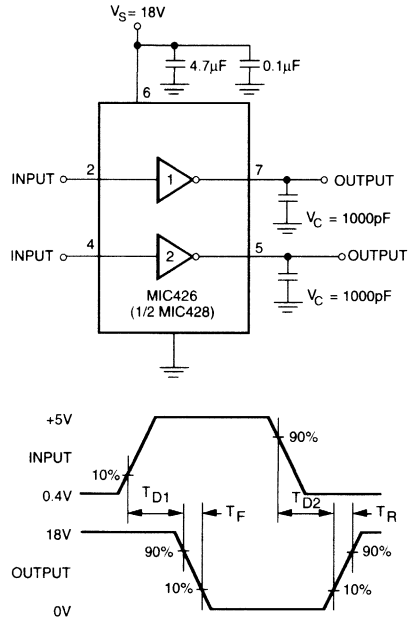


Figure 1. Inverting Driver Switching Time

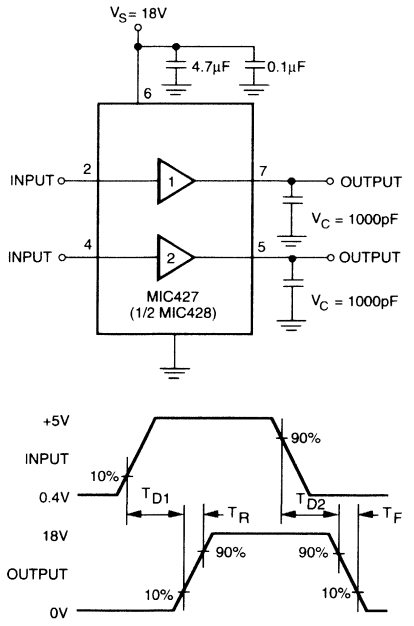
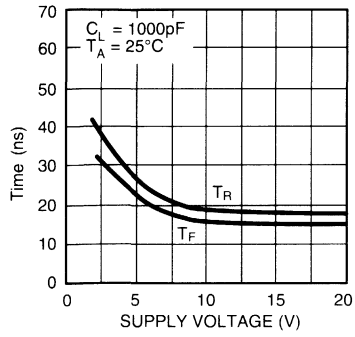


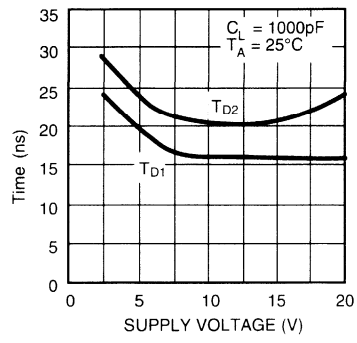
Figure 2. Non-Inverting Driver Switching Time

Typical Characteristic Curves

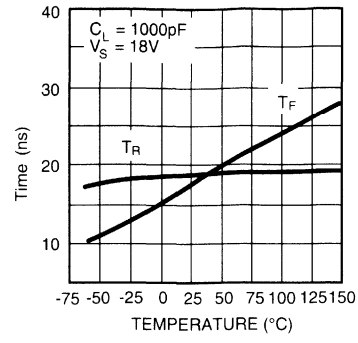
Rise and Fall Time vs. Supply Voltage



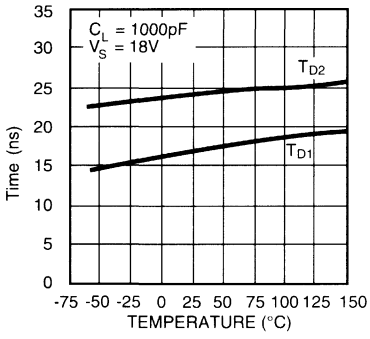
Delay Time vs. Supply Voltage



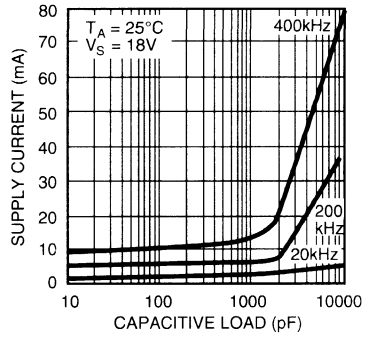
Rise and Fall Time vs. Temperature



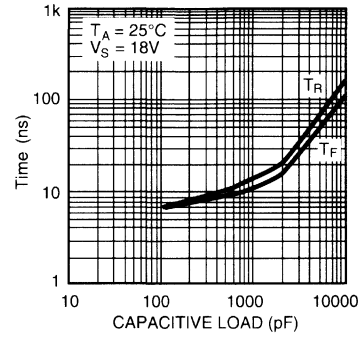
Delay Time vs. Temperature



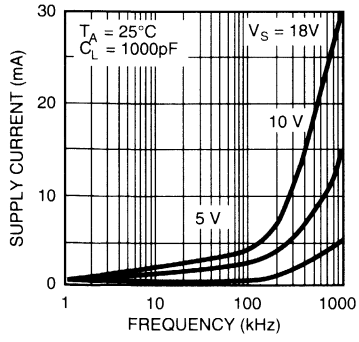
Supply Current vs. Capacitive Load



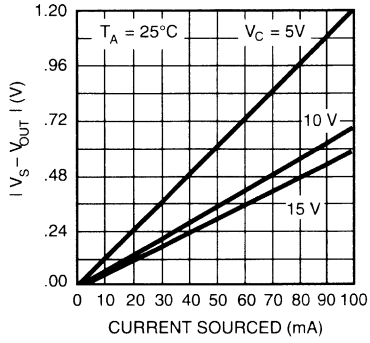
Rise and Fall Time vs. Capacitive Load



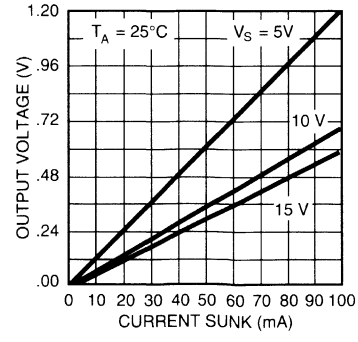
Supply Current vs. Frequency



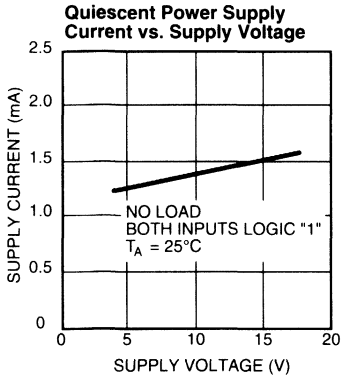
High Output vs. Current

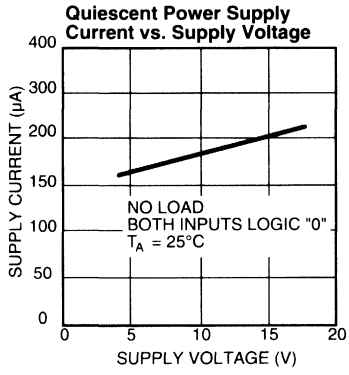


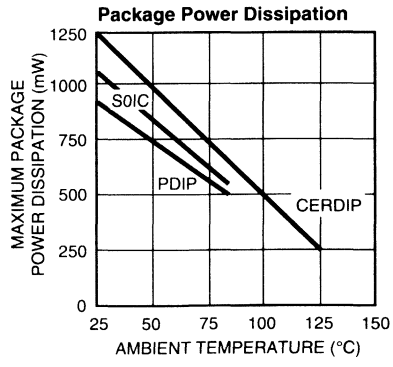
Low Output vs. Current



Typical Characteristic Curves (Continued)







Supply Bypassing

Charging and discharging large capacitive loads quickly requires large currents. For example, changing a 1000pF load 18 volts in 25ns requires a 0.8A current from the device power supply.

To guarantee low supply impedance over a wide frequency range, a parallel capacitor combination is recommended for supply bypassing. Low inductance ceramic disk capacitors with short lead lengths (< 0.5 inch) should be used. A 4.7µF solid tantalum capacitor in parallel with one or two 0.1µF ceramic disk capacitors normally provides adequate bypassing.

Grounding

The MIC426 and MIC428 contain inverting drivers. Ground potential drops developed in common ground impedances from input to output will appear as negative feedback and degrade switching speed characteristics.

Individual ground returns for the input and output circuits or a ground plane should be used.

Input Stage

The input voltage level changes the no load or quiescent supply current. The N channel MOSFET input stage transistor drives a 2.5mA current source load. With a logic "1" input, the maximum quiescent supply current is 8mA. Logic "0" input level signals reduce quiescent current to 400µA maximum. Minimum power dissipation occurs for logic "0" inputs for the MIC426/427/428; unused driver inputs **must be grounded or tied to the positive supply.**

The drivers are designed with 100mV of hysteresis. This provides clean transitions and minimizes output stage current spiking when changing states. Input voltage thresholds are approximately 1.5V making the device TTL compatible over the 4.5V to 18V operating supply range. Input current is less than 1µA over this range.

The MIC426/427/428 may be directly driven by the TL494, SG1526/1527, SG1524, SE5560 and similar switch mode power supply integrated circuits.

Power Dissipation

The supply current vs. frequency and supply current vs. capacitive load characteristic curves will aid in performing power dissipation calculations.

The MIC426/427/428 CMOS drivers have greatly reduced quiescent DC power consumption. Maximum quiescent current is 8mA compared to the DS0026 40mA specification. For a 15V supply, power dissipation is typically 40mW.

Two other power dissipation components are:

- Output stage AC and DC load power.
- Transition state power.

Output stage power is:

$$P_O = P_{DC} + P_{AC}$$
$$= V_O (I_{DC}) + f C_L V_S^2$$

Where: V_O = DC output voltage
I_{DC} = DC output load current
f = Switching frequency
V_S = Supply voltage

In power MOSFET drive applications, the P_{DC} term is negligible. MOSFET power transistors are high impedance, capacitive input devices. In applications where resistive loads or relays are driven, the P_{DC} component will normally dominate.

The magnitude of P_{AC} is readily estimated for several cases:

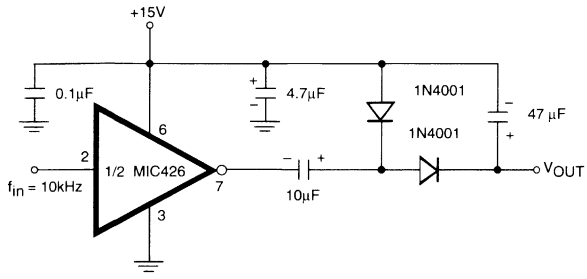
A. 1. f = 200kHz
2. C_L = 1000pF
3. V_S = 18V
4. P_{AC} = 65mW

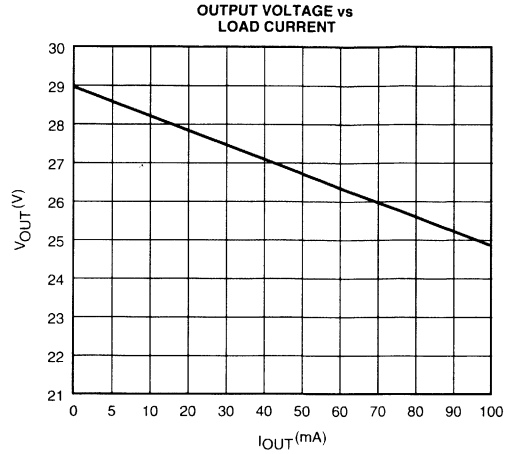
B. 1. f = 200kHz
2. C_L = 1000pF
3. V_S = 15V
4. P_{AC} = 45mW

During output level state changes, a current surge will flow through the series connected N and P channel output

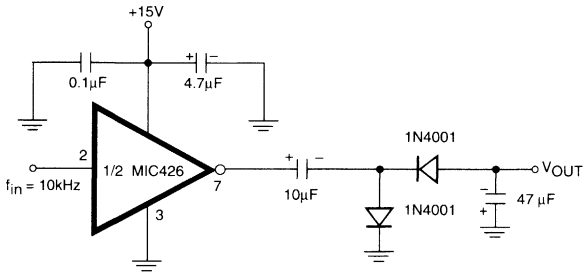
MOSFETs as one device is turning "ON" while the other is turning "OFF." The current spike flows only during output transitions. The input levels should not be maintained between the logic "0" and logic "1" levels. **Unused driver inputs must be tied to ground and not be allowed to float.** Average power dissipation will be reduced by minimizing input rise times. As shown in the characteristic curves, average supply current is frequency dependent.

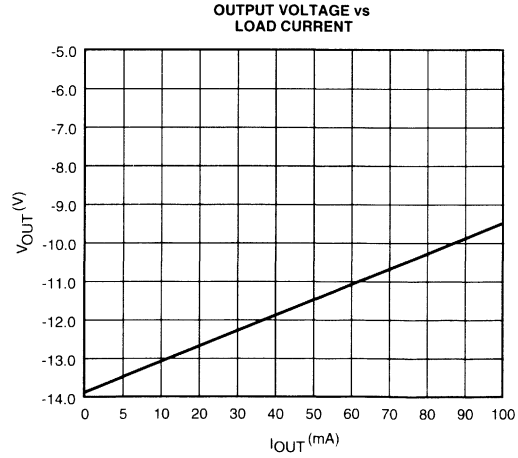
Voltage Doubler





Voltage Inverter





MIC1426/1427/1428

1.2A Dual High-Speed MOSFET Drivers

Bipolar/CMOS/DMOS Process

General Description

The MIC1426/27/28 are a family of 1.2A dual high-speed drivers. They are ideal for high-volume OEM manufacturers, with latch-up protection, and ESD protection. BiCMOS/DMOS fabrication is used for low power consumption and high efficiency.

These devices are fabricated using an epitaxial layer to effectively short out the intrinsic parasitic transistor responsible for CMOS latch-up. They incorporate a number of other design and process refinements to increase their long-term reliability.

The MIC1426 is compatible with the bipolar DS0026, but only draws 1/5 of the quiescent current. The MIC1426/27/28 are also compatible with the MIC426/27/28, but with 1.2A peak output current rather than the 1.5A of the MIC426/27/28 devices.

The high-input impedance MIC1426/27/28 drivers are CMOS/TTL input-compatible, do not require the speed-up needed by the bipolar devices, and can be directly driven by most PWM ICs.

This family of devices is available in inverting and non-inverting versions. Specifications have been optimized to achieve low-cost and high-performance devices, well-suited for the high-volume manufacturer.

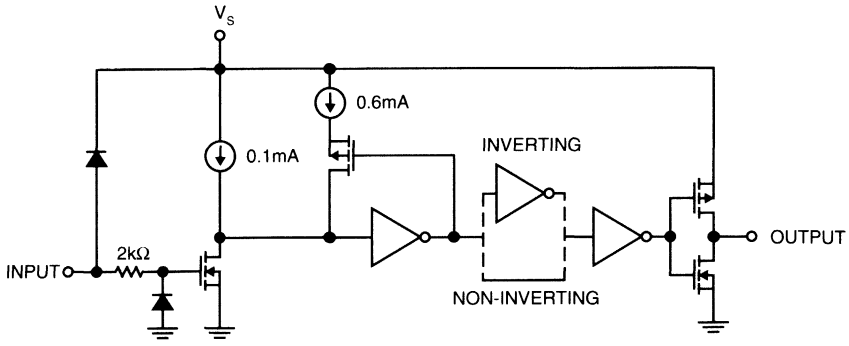
Features

- Low Cost
- Latch-Up Protected: Will Withstand 500mA Reverse Output Current
- ESD Protected ..... ±2kV
- High Peak Output Current ..... 1.2A Peak
- High Capacitive Load Drive Capability ..... 1000pF in 38ns
- Wide Operating Range ..... 4.75V to 16V
- Low Delay Time ..... 75ns Max
- Low Equivalent Input Capacitance (typ) 6pF
- Logic Input Threshold Independent of Supply Voltage
- Output Voltage Swing to Within 25mV of Ground or V_S
- Low Output Impedance 8Ω

Applications

- Power MOSFET Drivers
- Switched Mode Power Supplies
- Pulse Transformer Drive
- Small Motor Controls
- Print Head Drive

Functional Diagram

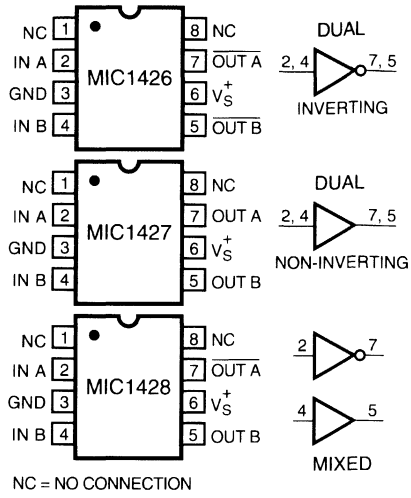


Functional Diagram for One Driver (Two Drivers per Package—Ground Unused Drivers)

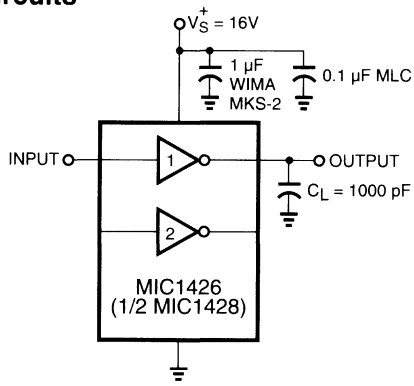
Ordering Information

Part No.	Temperature Range	Package	Configuration
MIC1426CM	0°C to 70°C	8-Pin SO	Dual-Inverting
MIC1426CN	0°C to 70°C	8-Pin Plastic DIP	Dual-Inverting
MIC1427CM	0°C to 70°C	8-Pin SO	Dual Non-Inverting
MIC1427CN	0°C to 70°C	8-Pin Plastic DIP	Dual Non-Inverting
MIC1428CM	0°C to 70°C	8-Pin SO	Inverting and Non-Inverting
MIC1428CN	0°C to 70°C	8-Pin Plastic DIP	Inverting and Non-Inverting

Pin Configurations



Test Circuits



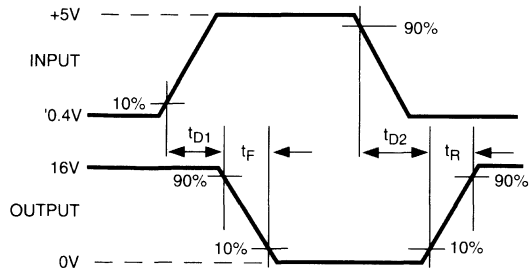
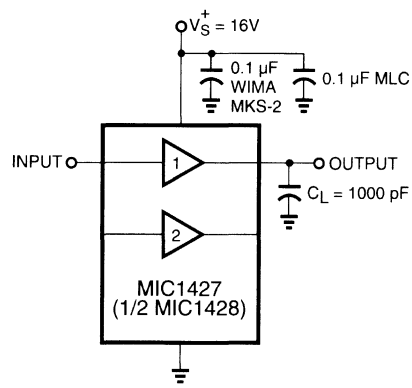


Figure 1. Inverting Driver Switching Time



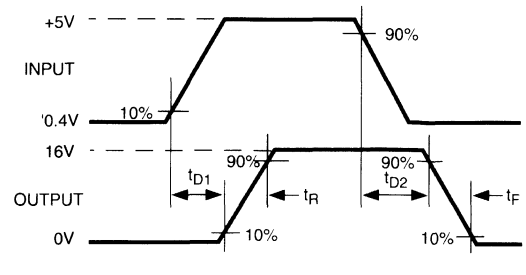


Figure 2. Non-Inverting Driver Switching Time

Absolute Maximum Ratings (Notes 1, 2 and 3)

Power Dissipation
- Plastic DIP 750mW
- SOIC 830mW

Derating Factor
- Plastic DIP 7.7mW/°C
- SOIC 8.3mW/°C

Supply Voltage 18V

Input Voltage, Any Terminal V_S + 0.3V to GND – 0.3V

Operating Temperature: C Version 0°C to +70°C

Maximum Chip Temperature +150°C

Storage Temperature –55°C to +150°C

Lead Temperature (10 sec) +300°C

NOTES: 1. Functional operation above the absolute maximum stress ratings is not implied.
2. Static-sensitive device (above 2kV). Unused devices must be stored in conductive material to protect devices from static discharge.
3. Switching times guaranteed by design.

Electrical Characteristics: T_A = 25°C with 4.75V < V_S < 16V unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
INPUT						
V_{IH}	Logic 1, Input Voltage		3	1.4		V
V_{IL}	Logic 0, Input Voltage			1.1	0.8	V
I_{IN}	Input Current	0V < V_{IN} < V_S	–1		1	µA
OUTPUT						
V_{OH}	High Output Voltage	Test Figures 1 and 2	V_S–0.025			V
V_{OL}	Low Output Voltage	Test Figures 1 and 2			0.025	V
R_O	Output Resistance	V_{IN} = 0.8V I_{OUT} = 10 mA, V_S = 16V		6	18	Ω
R_O	Output Resistance	V_{IN} = 3V I_{OUT} = 10 mA, V_S = 16V		6	12	Ω
I_{PK}	Peak Output Current			1.5		A
I	Latch-Up Current	Withstand Reverse Current	>500			mA
SWITCHING TIME						
t_R	Rise Time	Test Figures 1 and 2		18	35	ns
t_F	Fall Time	Test Figures 1 and 2		15	25	ns
t_{D1}	Delay Time	Test Figures 1 and 2		17	75	ns
t_{D2}	Delay Time	Test Figures 1 and 2		23	75	ns
POWER SUPPLY						
I_S	Power Supply Current	V_{IN} = 3V (Both Inputs) V_{IN} = 0V (Both Inputs)		1.4 0.18	9 0.5	mA mA

Electrical Characteristics:

Over operating temperature range with 4.75V < V_S < 16V unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
INPUT						
V_{IH}	Logic 1, Input Voltage		3	1.5		V
V_{IL}	Logic 0, Input Voltage			1.0	0.8	V
I_{IN}	Input Current	0V < V_{IN} < V_S	–10		10	µA
OUTPUT						
V_{OH}	High Output Voltage	Test Figures 1 and 2	V_S–0.025			V
V_{OL}	Low Output Voltage	Test Figures 1 and 2			0.025	V
R_O	Output Resistance	V_{IN} = 0.8V I_{OUT} = 10 mA, V_S = 16V		8	23	Ω
R_O	Output Resistance	V_{IN} = 3V I_{OUT} = 10 mA, V_S = 16V		10	18	Ω
I	Latch-Up Current	Withstand Reverse Current	>500	1.5		mA
SWITCHING TIME						
t_R	Rise Time	Test Figures 1 and 2		20	60	ns
t_F	Fall Time	Test Figures 1 and 2		29	40	ns
t_{D1}	Delay Time	Test Figures 1 and 2		19	125	ns
t_{D2}	Delay Time	Test Figures 1 and 2		27	125	ns
POWER SUPPLY						
I_S	Power Supply Current	V_{IN} = 3V (Both Inputs)		1.5	13	mA
I_S	Power Supply Current	V_{IN} = 0V (Both Inputs)		0.19	0.7	mA

Supply Bypassing

Large currents are required to charge and discharge large capacitive loads quickly. For example, changing a 1000pF load 16V in 25ns, requires a 0.8A current from the device power supply.

To guarantee low supply impedance over a wide frequency range, a parallel capacitor combination is recommended for supply bypassing. Low-inductance ceramic MLC capacitors with short lead lengths (<0.5in.) should be used. A 1.0µF film capacitor in parallel with one or two 0.1µF ceramic MLC capacitors normally provides adequate bypassing.

Grounding

The MIC1426 and MIC1428 contain inverting drivers. Ground potential drops developed in common ground impedances from input to output will appear as negative feedback and degrade switching speed characteristics.

Individual ground returns for the input and output circuits or a ground plane should be used.

Input Stage

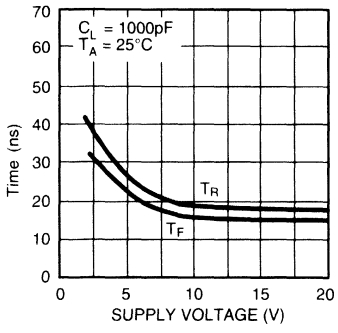
The input voltage level changes the no-load or quiescent supply current. The N-channel MOSFET input stage transistor drives a 2.5mA current source load. With a logic "1" input, the maximum quiescent supply current is 9mA. Logic "0" input level signals reduce quiescent current to 500µA maximum. **Unused driver inputs must be connected to V_S or GND**. Minimum power dissipation occurs for logic "0" inputs for the MIC1426/27/28.

The drivers are designed with 100mV of hysteresis. This provides clean transitions and minimizes output stage current spiking when changing states. Input voltage thresholds are approximately 1.5V, making logic "1" input any voltage greater than 1.5V up to V_S. Input current is less than 1µA over this range.

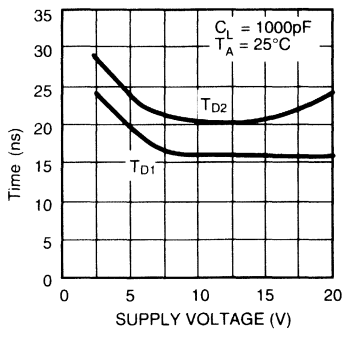
The MIC1426/27/28 may be directly driven by the TL494, SG1526/27, MIC38C42, TSC170 and similar switch-mode power supply integrated circuits.

MIC1426/7/8 Typical Characteristic Curves

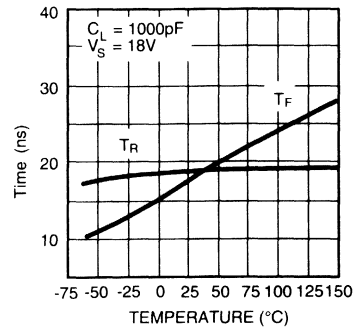
Rise and Fall Time vs. Supply Voltage



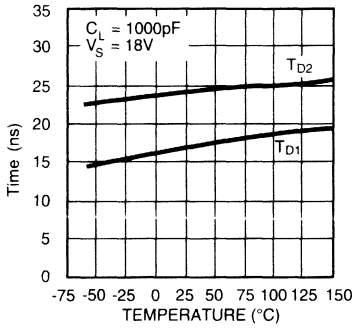
Delay Time vs. Supply Voltage



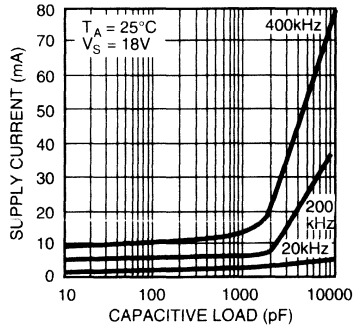
Rise and Fall Time vs. Temperature



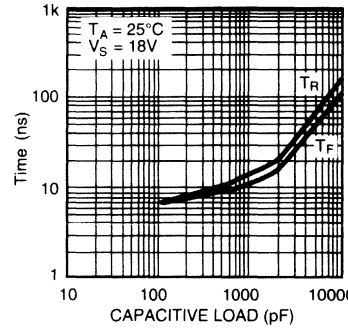
Delay Time vs. Temperature



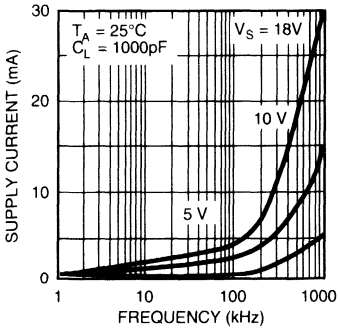
Supply Current vs. Capacitive Load



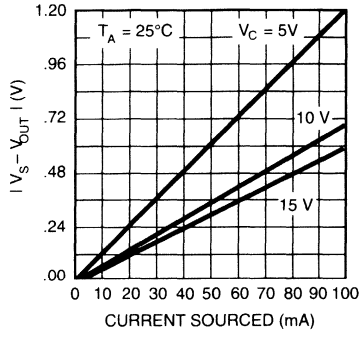
Rise and Fall Time vs. Capacitive Load



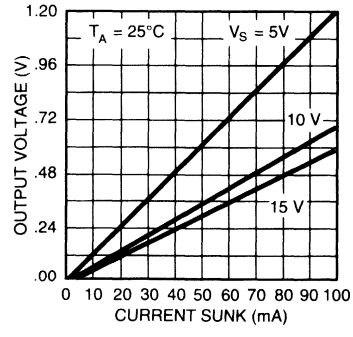
Supply Current vs. Frequency



High Output vs. Current

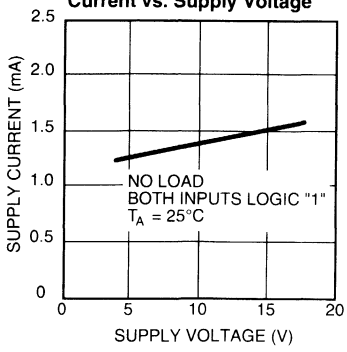


Low Output vs. Current

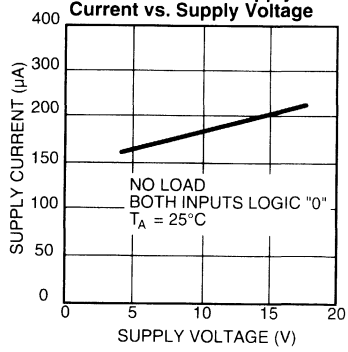


MIC1426/7/8 Typical Characteristic Curves (Cont.)

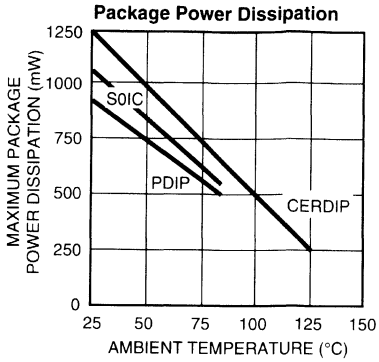
Quiescent Power Supply Current vs. Supply Voltage



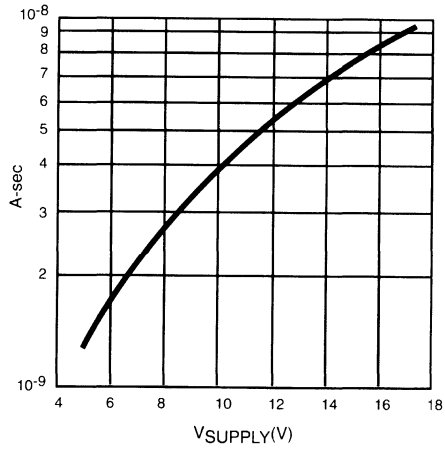
Quiescent Power Supply Current vs. Supply Voltage



Package Power Dissipation



Crossover Energy Loss



Note: The values on this graph represent the loss seen by a single transition of a single driver. For a complete cycle of a single driver multiply the stated value by 2.

MIC4420/4429

6A High-Speed High-Current MOSFET Driver

Bipolar/CMOS/DMOS Process

General Description

MIC4420 and MIC4429 MOSFET drivers are tough, efficient, and easy to use. The MIC4429 is an inverting driver, while the MIC4420 is a non-inverting driver.

Both versions are capable of 6A (peak) output and can drive the largest MOSFETs with an improved safe operating margin. The MIC4420/4429 accepts any logic input from 2.4V to V_S without external speed-up capacitors or resistor networks. Proprietary circuits allow the input to swing negative by as much as 5V without damaging the part. Additional circuits protect against damage from electrostatic discharge.

MIC4420/4429 drivers can replace three or more discrete components, reducing PCB area requirements, simplifying product design, and reducing assembly cost.

Modern BiCMOS/DMOS construction guarantees freedom from latch-up. The rail-to-rail swing capability insures adequate gate voltage to the MOSFET during power up/down sequencing.

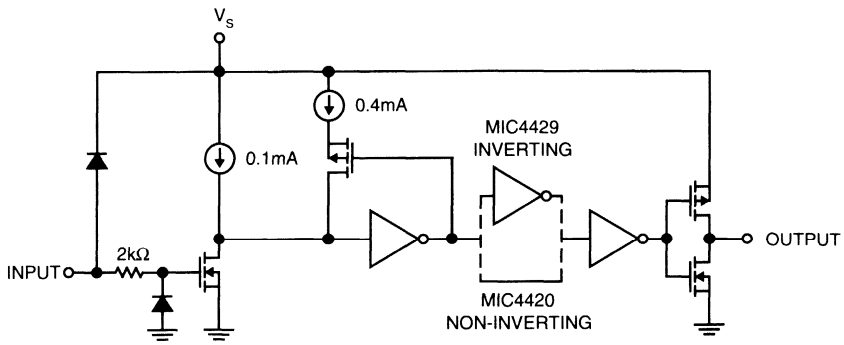
Features

- CMOS Construction
- Latch-Up Protected: Will Withstand >500mA Reverse Output Current
- Logic Input Will Withstand Negative Swing of Up to 5V
- Matched Rise and Fall Times 25ns
- High Peak Output Current ..... 6A Peak
- Wide Operating Range ..... 4.5V to 18V
- High Capacitive Load Drive 10,000pF
- Low Delay Time ..... 55ns Typ
- Logic High Input for Any Voltage From 2.4V to V_S
- Low Equivalent Input Capacitance (typ) 6pF
- Low Supply Current ..... 450µA With Logic 1 Input
- Low Output Impedance 2.5Ω
- Output Voltage Swing to Within 25mV of Ground or V_S
- MIL-STD-883 Method 5004/5005 version available

Applications

- Switch Mode Power Supplies
- Motor Controls
- Pulse Transformer Driver
- Class D Switching Amplifiers

Functional Diagram



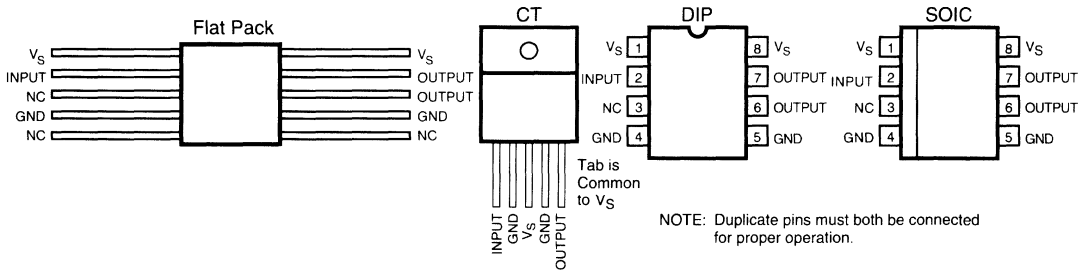
Ordering Information

Part No.	Temperature Range	Package	Configuration
MIC429AJBQ*	–55°C to +125°C	8-Pin CerDIP	Inverting
MIC4420CN	0°C to +70°C	8-Pin PDIP	Non-Inverting
MIC4420BN	–40°C to +85°C	8-Pin PDIP	Non-Inverting
MIC4420CM	0°C to +70°C	8-Pin SOIC	Non-Inverting
MIC4420BM	–40°C to +85°C	8-Pin SOIC	Non-Inverting
MIC4420AJ	–55°C to +125°C	8-Pin CerDIP	Non-Inverting
MIC4420AJB†	–55°C to +125°C	8-Pin CerDIP	Non-Inverting
MIC4420AF	–55°C to +125°C	10-Pin Flat Pack	Non-Inverting
MIC4420CT	0°C to +70°C	5-Pin TO-220	Non-Inverting
MIC4429CN	0°C to +70°C	8-Pin PDIP	Inverting
MIC4429BN	–40°C to +85°C	8-Pin PDIP	Inverting
MIC4429CM	0°C to +70°C	8-Pin SOIC	Inverting
MIC4429BM	–40°C to +85°C	8-Pin SOIC	Inverting
MIC4429AJ	–55°C to +125°C	8-Pin CerDIP	Inverting
MIC4429AJB†	–55°C to +125°C	8-Pin CerDIP	Inverting
MIC4429AF	–55°C to +125°C	10-Pin Flat Pack	Inverting
MIC4429CT	0°C to +70°C	5-Pin TO-220	Inverting

* SMD#5962-8877001PX

† AJB indicates units screened to MIL-STD 883, Method 5004, condition B, and burned-in for 1 week.

Pin Configurations



Absolute Maximum Ratings (Notes 1, 2 and 3)

Power Dissipation, $T_{AMBIENT} \leq 25°C$	
PDIP	960MW
SOIC	1040 mW
CerDIP	1250 mW
5-Pin TO-220	2W
Power Dissipation, $T_{CASE} \leq 25°C$	
5-Pin TO-220	12.5W
Derating Factors (To Ambient)	
PDIP	7.7 mW/°C
SOIC	8.3 mW/°C
CerDIP	10 mW/°C
5-Pin TO-220	17 mW/°C
Thermal Impedances (To Case)	
5-Pin TO-220 $R_{\theta J-C}$	10°C/W
Storage Temperature	–65°C to +150°C
Operating Temperature (Chip)	150°C
Operating Temperature (Ambient)	
C Version	0°C to +70°C
B Version	–40°C to +85°C
A Version	–55°C to +125°C
Lead Temperature (10 sec)	300°C
Supply Voltage	20V
Input Voltage	–5V to V_S
Input Current ($V_{IN} > V_S$)	50 mA

If Military/Aerospace specified devices are required, contact Micrel for availability and specifications.

Electrical Characteristics: (T_A = 25°C with 4.5V ≤ V_S ≤ 18V unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
INPUT						
V_{IH}	Logic 1 Input Voltage		2.4	1.4		V
V_{IL}	Logic 0 Input Voltage			1.1	0.8	V
V_{IN}	Input Voltage Range		–5		V_S + 0.3	V
I_{IN}	Input Current	0 V ≤ V_{IN} ≤ V_S	–10		10	µA
OUTPUT						
V_{OH}	High Output Voltage	See Figure 1	V_S–0.025			V
V_{OL}	Low Output Voltage	See Figure 1			0.025	V
R_O	Output Resistance, Output Low	I_{OUT} = 10 mA, V_S = 18 V		1.7	2.8	Ω
R_O	Output Resistance, Output High	I_{OUT} = 10 mA, V_S = 18 V		1.5	2.5	Ω
I_{PK}	Peak Output Current	V_S = 18 V (See Figure 5)		6		A
I_R	Latch-Up Protection Withstand Reverse Current		>500			mA
SWITCHING TIME (Note 3)						
t_R	Rise Time	Test Figure 1, C_L = 2500 pF		12	35	ns
t_F	Fall Time	Test Figure 1, C_L = 2500 pF		13	35	ns
t_{D1}	Delay Time	Test Figure 1		18	75	ns
t_{D2}	Delay Time	Test Figure 1		48	75	ns
Power Supply						
I_S	Power Supply Current	V_{IN} = 3 V V_{IN} = 0 V		0.45 90	1.5 150	mA µA
V_S	Operating Input Voltage		4.5		18	V

2

Electrical Characteristics: (T_A = −55°C to +125°C with 4.5V ≤ V_S ≤ 18V unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
INPUT						
V_{IH}	Logic 1 Input Voltage		2.4			V
V_{IL}	Logic 0 Input Voltage				0.8	V
V_{IN}	Input Voltage Range		−5		V_S + 0.3	V
I_{IN}	Input Current	0V ≤ V_{IN} ≤ V_S	−10		10	µA
OUTPUT						
V_{OH}	High Output Voltage	Figure 1	V_S−0.025			V
V_{OL}	Low Output Voltage	Figure 1			0.025	V
R_O	Output Resistance, Output Low	I_{OUT} = 10mA, V_S = 18V		3	5	Ω
R_O	Output Resistance, Output High	I_{OUT} = 10mA, V_S = 18V		2.3	5	Ω
SWITCHING TIME (Note 3)						
t_R	Rise Time	Figure 1, C_L = 2500pF		32	60	ns
t_F	Fall Time	Figure 1, C_L = 2500pF		34	60	ns
t_{D1}	Delay Time	Figure 1		50	100	ns
t_{D2}	Delay Time	Figure 1		65	100	ns
POWER SUPPLY						
I_S	Power Supply Current	V_{IN} = 3V V_{IN} = 0V		0.45 0.06	3.0 0.4	mA mA
V_S	Operating Input Voltage		4.5		18	V

NOTE 1: Functional operation above the absolute maximum stress ratings is not implied.
NOTE 2: Static-sensitive device. Store only in conductive containers. Handling personnel and equipment should be grounded to prevent damage from static discharge.
NOTE 3: Switching times guaranteed by design.

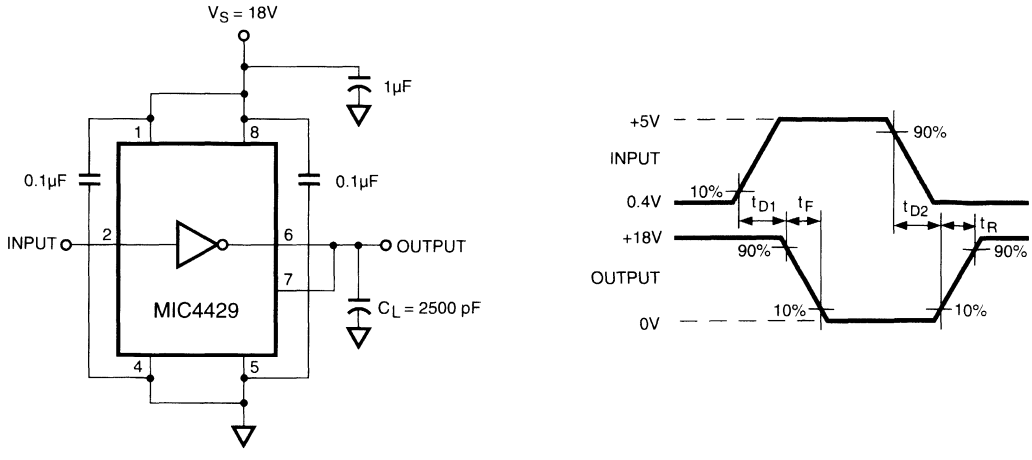
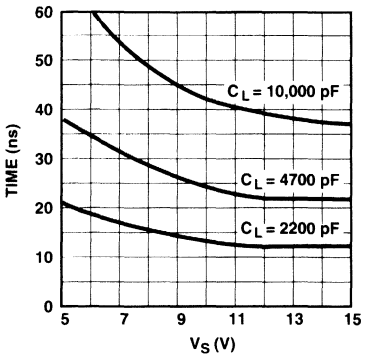


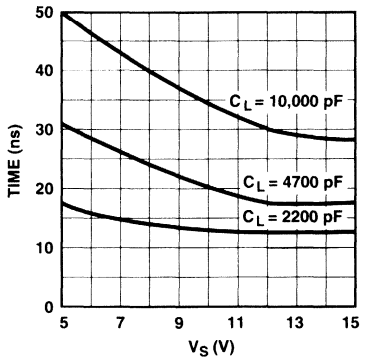
Figure 1. Switching Time Test Circuit

Typical Characteristic Curves

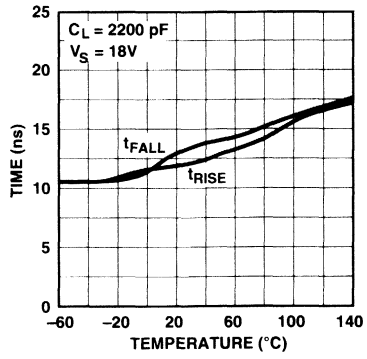
Rise Time vs. Supply Voltage



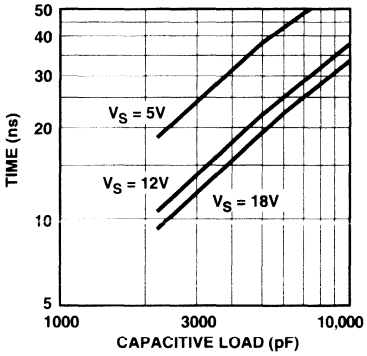
Fall Time vs. Supply Voltage



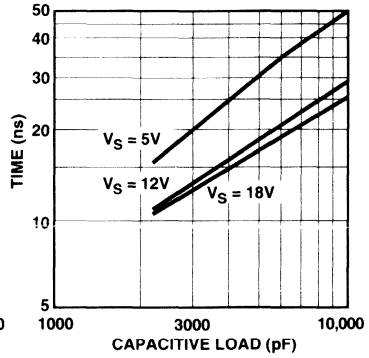
Rise and Fall Times vs. Temperature



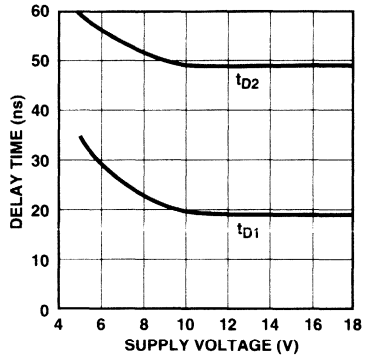
Rise Time vs. Capacitive Load



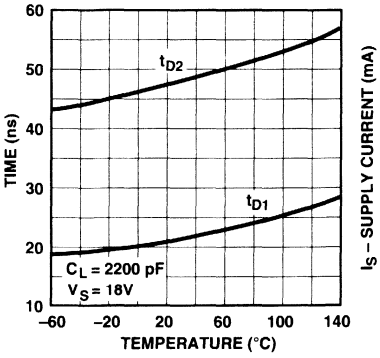
Fall Time vs. Capacitive Load



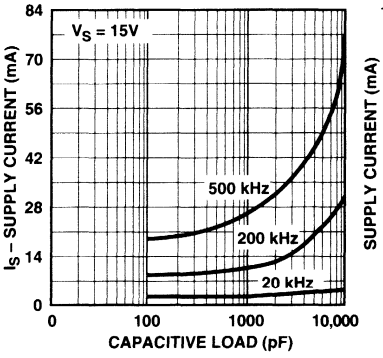
Delay Time vs. Supply Voltage



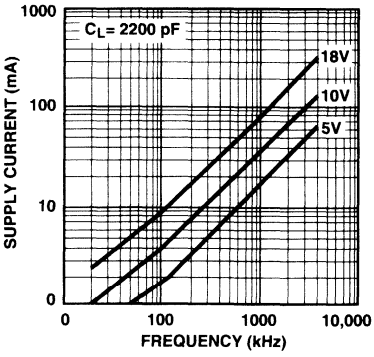
Propagation Delay Time vs. Temperature



Supply Current vs. Capacitive Load

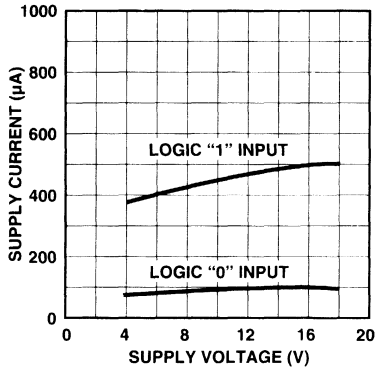


Supply Current vs. Frequency

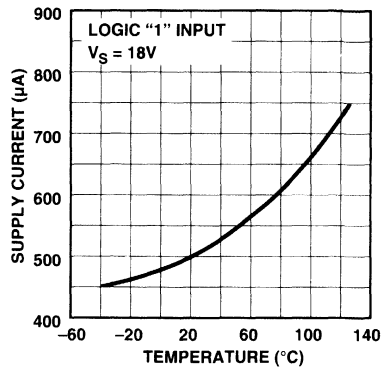


Typical Characteristic Curves (Cont.)

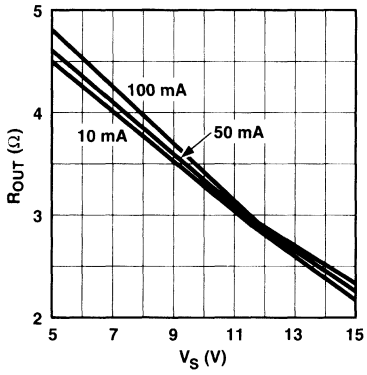
Quiescent Power Supply Voltage vs. Supply Current



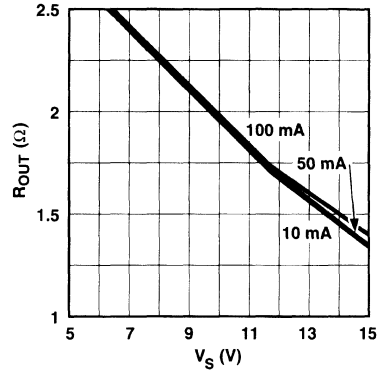
Quiescent Power Supply Current vs. Temperature



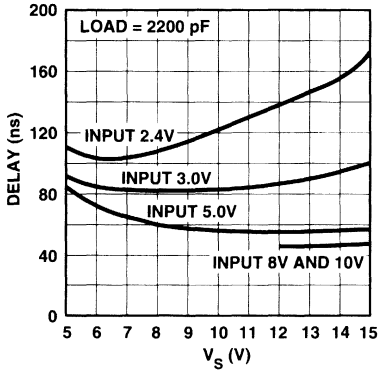
High-State Output Resistance



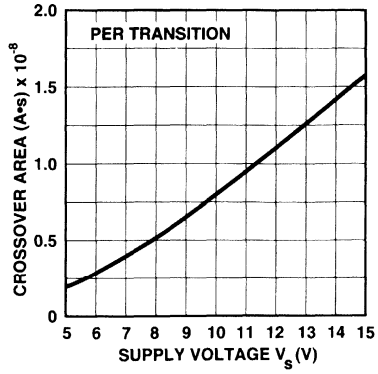
Low-State Output Resistance



Effect of Input Amplitude on Propagation Delay



Crossover Area vs. Supply Voltage



Applications Information

Supply Bypassing

Charging and discharging large capacitive loads quickly requires large currents. For example, charging a 2500pF load to 18V in 25ns requires a 1.8 A current from the device power supply.

The MIC4420/4429 has double bonding on the supply pins, the ground pins and output pins This reduces parasitic lead inductance. Low inductance enables large currents to be switched rapidly. It also reduces internal ringing that can cause voltage breakdown when the driver is operated at or near the maximum rated voltage.

Internal ringing can also cause output oscillation due to feedback. This feedback is added to the input signal since it is referenced to the same ground.

To guarantee low supply impedance over a wide frequency range, a parallel capacitor combination is recommended for supply bypassing. Low inductance ceramic disk capacitors with short lead lengths (< 0.5 inch) should be used. A 1μF low ESR film capacitor in parallel with two 0.1 μF low ESR ceramic capacitors, (such as AVX RAM GUARD®), provides adequate bypassing. Connect one ceramic capacitor directly between pins 1 and 4. Connect the second ceramic capacitor directly between pins 8 and 5.

Grounding

The high current capability of the MIC4420/4429 demands careful PC board layout for best performance Since the MIC4429 is an inverting driver, any ground lead impedance will appear as negative feedback which can degrade switching speed. Feedback is especially noticeable with slow-rise time inputs. The MIC4429 input structure includes 300mV of hysteresis to ensure clean transitions and freedom from oscillation, but attention to layout is still recommended.

Figure 5 shows the feedback effect in detail. As the MIC4429 input begins to go positive, the output goes negative and several amperes of current flow in the ground lead. As little as 0.05Ω of PC trace resistance can produce hundreds of millivolts at the MIC4429 ground pins. If the driving logic is referenced to power ground, the effective logic input level is reduced and oscillation may result.

To insure optimum performance, separate ground traces should be provided for the logic and power connections. Connecting the logic ground directly to the MIC4429 GND pins will ensure full logic drive to the input and ensure fast output switching. Both of the MIC4429 GND pins should, however, still be connected to power ground.

2

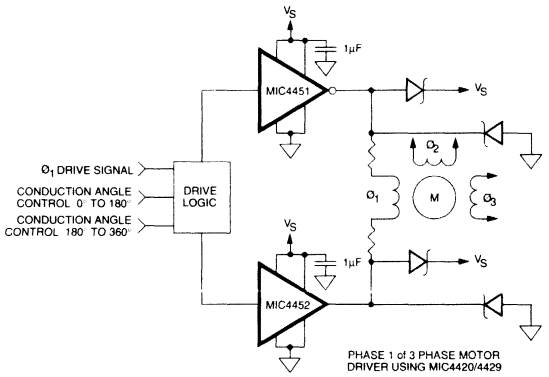
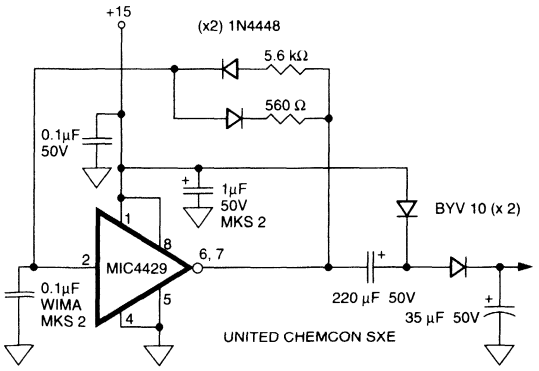


Figure 3. Direct Motor Drive



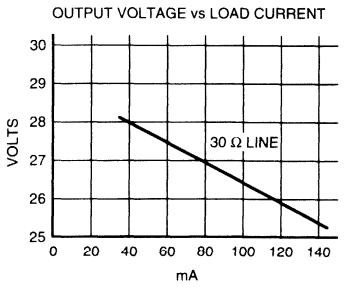


Figure 4. Self Contained Voltage Doubler

Input Stage

The input voltage level of the 4429 changes the quiescent supply current. The N channel MOSFET input stage transistor drives a 450µA current source load. With a logic "1" input, the maximum quiescent supply current is 450µA. Logic "0" input level signals reduce quiescent current to 55µA maximum.

The MIC4420/4429 input is designed to provide 300mV of hysteresis. This provides clean transitions, reduces noise sensitivity, and minimizes output stage current spiking when changing states. Input voltage threshold level is approximately 1.5V, making the device TTL compatible over the 4 .5V to 18V operating supply voltage range. Input current is less than 10µA over this range.

The MIC4429 can be directly driven by the TL494, SG1526/1527, SG1524, TSC170, MIC38HC42 and similar switch mode power supply integrated circuits. By offloading the power-driving duties to the MIC4420/4429, the power supply controller can operate at lower dissipation. This can improve performance and reliability.

The input can be greater than the $^{+}V_S$ supply, however, current will flow into the input lead. The propagation delay for T_{D2} will increase to as much as 400ns at room temperature. The input currents can be as high as 30mA p-p ($6.4mA_{RMS}$) with the input, 6 V greater than the supply voltage. No damage will occur to MIC4420/4429 however, and it will not latch.

The input appears as a 38pF capacitance, and does not change even if the input is driven from an AC source. Care should be taken so that the input does not go more than 5 volts below the negative rail.

Power Dissipation

CMOS circuits usually permit the user to ignore power dissipation. Logic families such as 4000 and 74C have outputs which can only supply a few milliamperes of current, and even shorting outputs to ground will not force enough current to destroy the device. The MIC4420/4429 on the other hand, can source or sink several amperes and drive large capacitive loads at high frequency. The package power dissipation limit can easily be exceeded. Therefore, some attention should be given to power dissipation when driving low impedance loads and/or operating at high frequency.

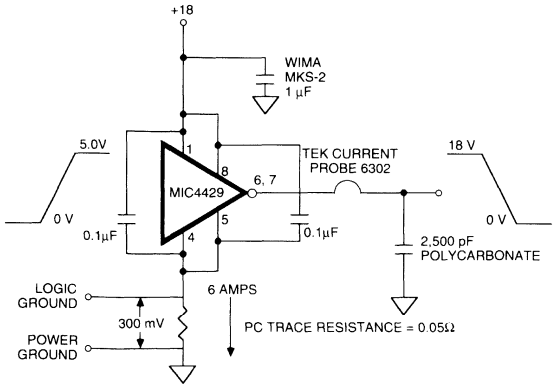


Figure 5. Switching Time Degradation Due to Negative Feedback

The supply current vs frequency and supply current vs capacitive load characteristic curves aid in determining power dissipation calculations. Table 1 lists the maximum safe operating frequency for several power supply voltages when driving a 2500pF load. More accurate power dissipation figures can be obtained by summing the three dissipation sources.

Given the power dissipation in the device, and the thermal resistance of the package, junction operating temperature for any ambient is easy to calculate. For example, the thermal resistance of the 8-pin CerDIP package, from the data sheet, is 150°C/W. In a 25°C ambient, then, using a maximum junction temperature of 150°C, this package will dissipate 800mW.

Accurate power dissipation numbers can be obtained by summing the three sources of power dissipation in the device:

- Load Power Dissipation (P_L)
- Quiescent power dissipation (P_Q)
- Transition power dissipation (P_T)

Calculation of load power dissipation differs depending on whether the load is capacitive, resistive or inductive.

Resistive Load Power Dissipation

Dissipation caused by a resistive load can be calculated as:

$$P_L = I^2 R_O D$$

where:

I = the current drawn by the load
R_O = the output resistance of the driver when the output is high, at the power supply voltage used. (See data sheet)
D = fraction of time the load is conducting (duty cycle)

Table 1: MIC4429 Maximum Operating Frequency

V_S	Max Frequency
18V	500kHz
15V	700kHz
10V	1.6MHz

Conditions: 1. DIP Package (θ_{JA} = 130°C/W)
2. T_A = 25°C
3. C_L = 2500pF

Capacitive Load Power Dissipation

Dissipation caused by a capacitive load is simply the energy placed in, or removed from, the load capacitance by the driver. The energy stored in a capacitor is described by the equation:

$$E = 1/2\ C\ V^2$$

As this energy is lost in the driver each time the load is charged or discharged, for power dissipation calculations the 1/2 is removed. This equation also shows that it is good practice not to place more voltage on the capacitor than is necessary, as dissipation increases as the square of the voltage applied to the capacitor. For a driver with a capacitive load:

$$P_L = F\ C\ (V_S)^2$$

where:

F = Operating Frequency
C = Load Capacitance
V_S = Driver Supply Voltage

Inductive Load Power Dissipation

For inductive loads the situation is more complicated. For the part of the cycle in which the driver is actively forcing current into the inductor, the situation is the same as it is in the resistive case:

$$P_{L1} = I^2\ R_O\ D$$

However, in this instance the R_O required may be either the on resistance of the driver when its output is in the high state, or its on resistance when the driver is in the low state, depending on how the inductor is connected, and this is still only half the story. For the part of the cycle when the inductor is forcing current through the driver, dissipation is best described as

$$P_{L2} = I\ V_D\ (1\text{-}D)$$

where V_D is the forward drop of the clamp diode in the driver (generally around 0.7V). The two parts of the load dissipation must be summed in to produce P_L

$$P_L = P_{L1} + P_{L2}$$

Quiescent Power Dissipation

Quiescent power dissipation (P_Q, as described in the input section) depends on whether the input is high or low. A low input will result in a maximum current drain (per driver) of ≤0.2mA; a logic high will result in a current drain of ≤2.0mA. Quiescent power can therefore be found from:

$$P_Q = V_S\ [D\ I_H + (1\text{-}D)\ I_L]$$

where:

I_H = quiescent current with input high
I_L = quiescent current with input low
D = fraction of time input is high (duty cycle)
V_S = power supply voltage

Transition Power Dissipation

Transition power is dissipated in the driver each time its output changes state, because during the transition, for a very brief interval, both the N- and P-channel MOSFETs in the output totem-pole are ON simultaneously, and a current is conducted through them from V^+_S to ground. The transition power dissipation is approximately:

$$P_T = 2\ F\ V_S\ (A{\bullet}s)$$

where (A•s) is a time-current factor derived from the typical characteristic curves.

Total power (P_D) then, as previously described is:

$$P_D = P_L + P_Q + P_T$$

Definitions

C_L = Load Capacitance in Farads.

D = Duty Cycle expressed as the fraction of time the input to the driver is high.

F = Operating Frequency of the driver in Hertz

I_H = Power supply current drawn by a driver when both inputs are high and neither output is loaded.

I_L = Power supply current drawn by a driver when both inputs are low and neither output is loaded.

I_D = Output current from a driver in Amps.

P_D = Total power dissipated in a driver in Watts.

P_L = Power dissipated in the driver due to the driver's load in Watts.

P_Q = Power dissipated in a quiescent driver in Watts.

P_T = Power dissipated in a driver when the output changes states ("shoot-through current") in Watts. NOTE: The "shoot-through" current from a dual transition (once up, once down) for both drivers is stated in Figure 7 in ampere-nanoseconds. This figure must be multiplied by the number of repetitions per second (frequency) to find Watts.

R_O = Output resistance of a driver in Ohms.

V_S = Power supply voltage to the IC in Volts.

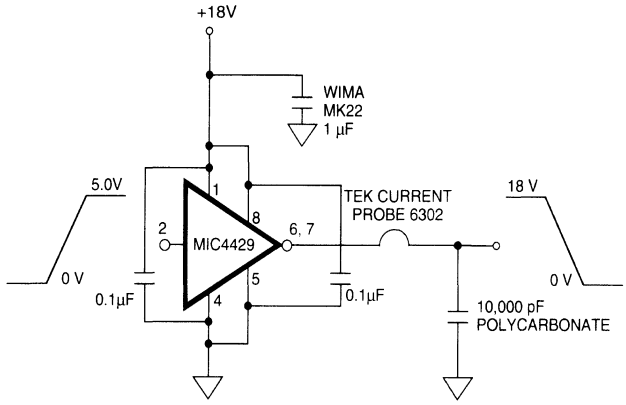


Figure 6. Peak Output Current Test Circuit

MIC4421/4422

9A High-Speed High-Current MOSFET Driver

Bipolar/CMOS/DMOS Process

General Description

MIC4421 and MIC4422 MOSFET drivers are rugged, efficient, and easy to use. The MIC4421 is an inverting driver, while the MIC4422 is a non-inverting driver.

Both versions are capable of 9A (peak) output and can drive the largest MOSFETs with an improved safe operating margin. The MIC4421/4422 accepts any logic input from 2.4V to V_S without external speed-up capacitors or resistor networks. Proprietary circuits allow the input to swing negative by as much as 5V without damaging the part. Additional circuits protect against damage from electrostatic discharge.

MIC4421/4422 drivers can replace three or more discrete components, reducing PCB area requirements, simplifying product design, and reducing assembly cost.

Modern Bipolar/CMOS/DMOS construction guarantees freedom from latch-up. The rail-to-rail swing capability of CMOS/DMOS insures adequate gate voltage to the MOSFET during power up/down sequencing. Since these devices are fabricated on a self-aligned process, they have very low crossover current, run cool, use little power, and are easy to drive.

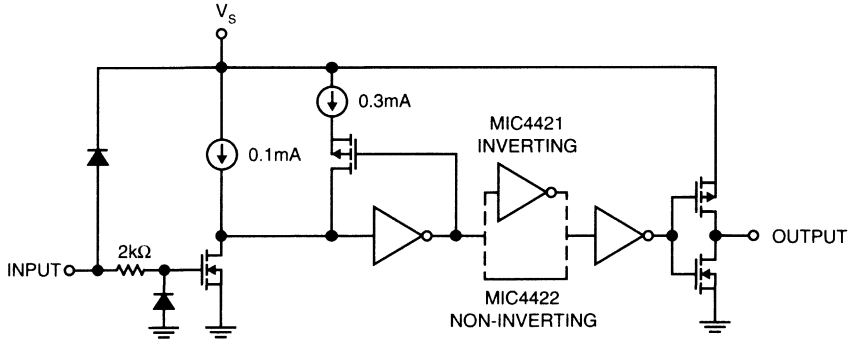
Features

- BiCMOS/DMOS Construction
- Latch-Up Proof: Fully Isolated Process is Inherently Immune to Any Latch-up.
- Input Will Withstand Negative Swing of Up to 5V
- Matched Rise and Fall Times 25ns
- High Peak Output Current ..... 9A Peak
- Wide Operating Range ..... 4.5V to 18V
- High Capacitive Load Drive 47,000pF
- Low Delay Time ..... 30ns Typ.
- Logic High Input for Any Voltage from 2.4V to V_S
- Low Equivalent Input Capacitance (typ) 7pF
- Low Supply Current ..... 450µA With Logic 1 Input
- Low Output Impedance 1.5Ω
- Output Voltage Swing to Within 25mV of GND or V_S
- MIL-STD-883 Method 5004/5005 Version Available

Applications

- Switch Mode Power Supplies
- Motor Controls
- Pulse Transformer Driver
- Class D Switching Amplifiers
- Line Drivers
- Driving MOSFET or IGBT Parallel Chip Modules
- Local Power ON/OFF Switch
- Pulse Generators

Functional Diagram

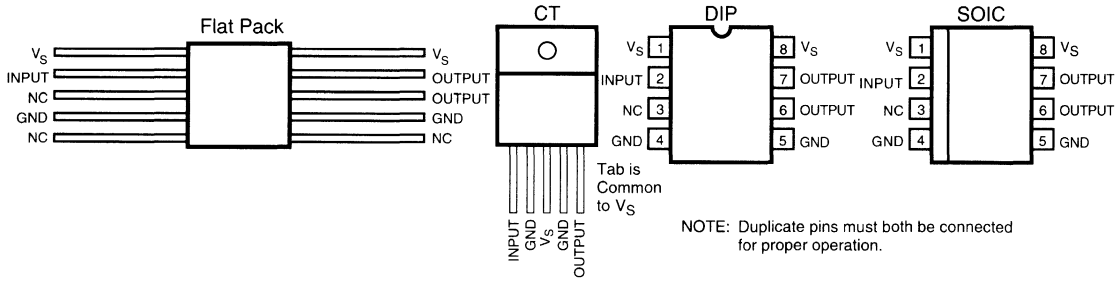


Ordering Information

Part No.	Temperature Range	Package	Configuration
MIC4421CN	0°C to +70°C	8-Pin PDIP	Inverting
MIC4421BN	–40°C to +85°C	8-Pin PDIP	Inverting
MIC4421CM	0°C to +70°C	8-Pin SOIC	Inverting
MIC4421BM	–40°C to +85°C	8-Pin SOIC	Inverting
MIC4421AJ	–55°C to +125°C	8-Pin CerDIP	Inverting
MIC4421AJB*	–55°C to +125°C	8-Pin CerDIP	Inverting
MIC4421AF	–55°C to +125°C	10-Pin Flat Pack	Inverting
MIC4421CT	0°C to +70°C	5-Pin TO-220	Inverting
MIC4422CN	0°C to +70°C	8-Pin PDIP	Non-Inverting
MIC4422BN	–40°C to +85°C	8-Pin PDIP	Non-Inverting
MIC4422CM	0°C to +70°C	8-Pin SOIC	Non-Inverting
MIC4422BM	–40°C to +85°C	8-Pin SOIC	Non-Inverting
MIC4422AJ	–55°C to +125°C	8-Pin CerDIP	Non-Inverting
MIC4422AJB*	–55°C to +125°C	8-Pin CerDIP	Non-Inverting
MIC4422AF	–55°C to +125°C	10-Pin Flat Pack	Non-Inverting
MIC4422CT	0°C to +70°C	5-Pin TO-220	Non-Inverting

* AJB indicates units screened to MIL-STD 883, Method 5004, condition B, and burned-in for 1 week.

Pin Configurations



Absolute Maximum Ratings (Notes 1, 2 and 3)

Power Dissipation, $T_{AMBIENT} \leq 25°C$
- PDIP 960mW
- SOIC 1040mW
- CerDIP 1250mW
- 5-Pin TO-220 2W

Power Dissipation, $T_{CASE} \leq 25°C$
- 5-Pin TO-220 12.5W

Derating Factors (To Ambient)
- PDIP 7.7mW/°C
- SOIC 8.3mW/°C
- CerDIP 10mW/°C
- 5-Pin TO-220 17mW/°C

Thermal Impedances (To Case)
- 5-Pin TO-220 $R_{\theta J-C}$ 10°C/W

Storage Temperature –65°C to +150°C

Operating Temperature (Chip) 150°C

Operating Temperature (Ambient)
- C Version 0°C to +70°C
- B Version –40°C to +85°C
- A Version –55°C to +125°C

Lead Temperature (10 sec) 300°C

Supply Voltage 20V

Input Voltage V_S + 0.3V to GND – 5V

Input Current ($V_{IN} > V_S$) 50 mA

Electrical Characteristics: (T_A = 25°C with 4.5 V ≤ V_S ≤ 18 V unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
INPUT						
V_{IH}	Logic 1 Input Voltage		2.4	1.3		V
V_{IL}	Logic 0 Input Voltage			1.1	0.8	V
V_{IN}	Input Voltage Range		–5		V_S + 0.3	V
I_{IN}	Input Current	0 V ≤ V_{IN} ≤ V_S	–10		10	µA
OUTPUT						
V_{OH}	High Output Voltage	See Figure 1	V_S–0.025			V
V_{OL}	Low Output Voltage	See Figure 1			0.025	V
R_O	Output Resistance, Output High	I_{OUT} = 10 mA, V_S = 18 V		0.6	1.7	Ω
R_O	Output Resistance, Output Low	I_{OUT} = 10 mA, V_S = 18 V		0.8	2.5	Ω
I_{PK}	Peak Output Current	V_S = 18 V (See Figure 5)		9		A
I_{DC}	Continuous Output Current		2			A
I_R	Latch-Up Protection Withstand Reverse Current	Duty Cycle ≤ 2% t ≤ 300 µs	>1500			mA
SWITCHING TIME (Note 3)						
t_R	Rise Time	Test Figure 1, C_L = 10,000 pF		20	75	ns
t_F	Fall Time	Test Figure 1, C_L = 10,000 pF		24	75	ns
t_{D1}	Delay Time	Test Figure 1		15	60	ns
t_{D2}	Delay Time	Test Figure 1		35	60	ns
Power Supply						
I_S	Power Supply Current	V_{IN} = 3 V V_{IN} = 0 V		0.4 80	1.5 150	mA µA
V_S	Operating Input Voltage		4.5		18	V

Electrical Characteristics: (Over operating temperature range with 4.5V ≤ V_S ≤ 18V unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
INPUT						
V_{IH}	Logic 1 Input Voltage		2.4	1.4		V
V_{IL}	Logic 0 Input Voltage			1.0	0.8	V
V_{IN}	Input Voltage Range		–5		V_S + 0.3	V
I_{IN}	Input Current	0V ≤ V_{IN} ≤ V_S	–10		10	µA
OUTPUT						
V_{OH}	High Output Voltage	Figure 1	V_S–0.025			V
V_{OL}	Low Output Voltage	Figure 1			0.025	V
R_O	Output Resistance, Output High	I_{OUT} = 10mA, V_S = 18V		0.8	3.6	Ω
R_O	Output Resistance, Output Low	I_{OUT} = 10mA, V_S = 18V		1.3	2.7	Ω
SWITCHING TIME (Note 3)						
t_R	Rise Time	Figure 1, C_L = 10,000pF		23	120	ns
t_F	Fall Time	Figure 1, C_L = 10,000pF		30	120	ns
t_{D1}	Delay Time	Figure 1		20	80	ns
t_{D2}	Delay Time	Figure 1		40	80	ns
POWER SUPPLY						
I_S	Power Supply Current	V_{IN} = 3V V_{IN} = 0V		0.6 0.1	3 0.2	mA
V_S	Operating Input Voltage		4.5		18	V

NOTE 1: Functional operation above the absolute maximum stress ratings is not implied.
NOTE 2: Static-sensitive device. Store only in conductive containers. Handling personnel and equipment should be grounded to prevent damage from static discharge.
NOTE 3: Switching times guaranteed by design.

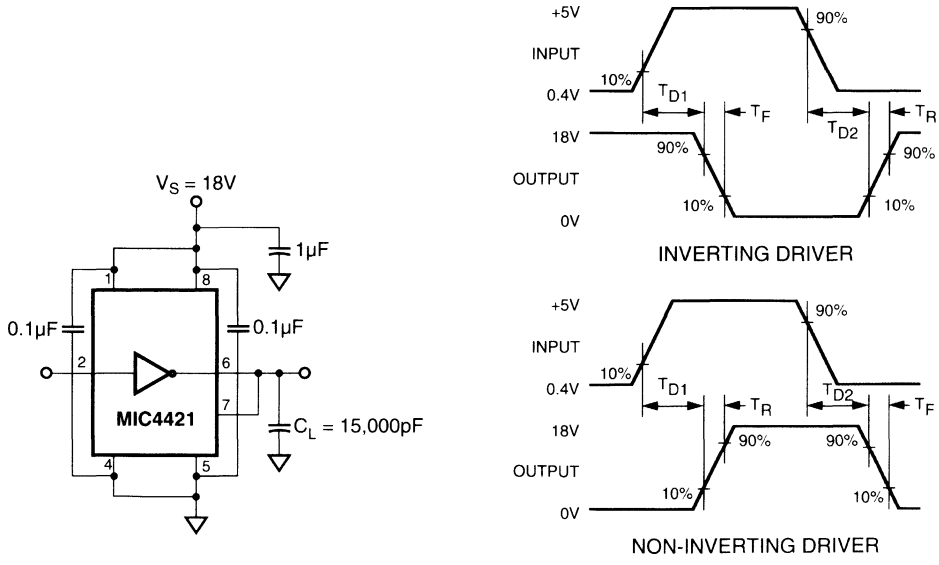
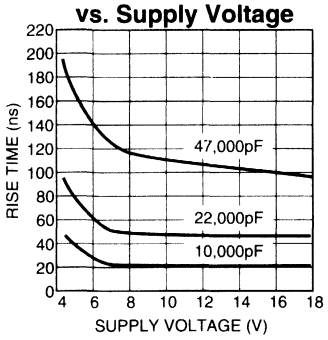


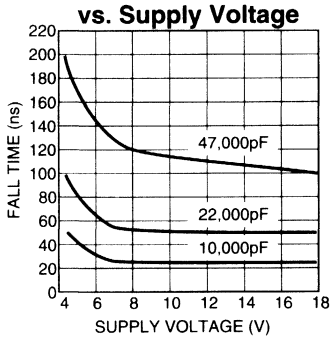
Figure 1. Switching Time Test Circuit

Typical Characteristic Curves

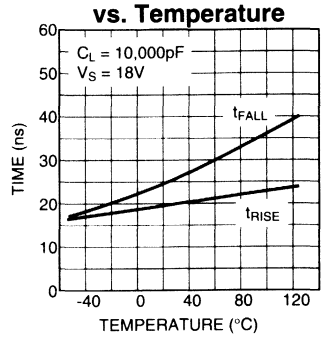
Rise Time vs. Supply Voltage



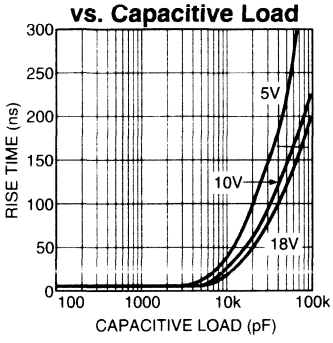
Fall Time vs. Supply Voltage



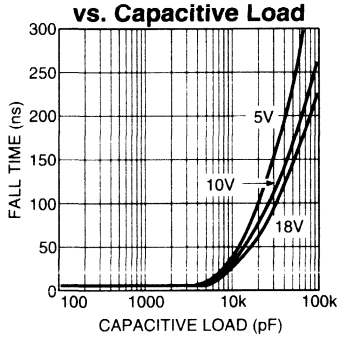
Rise and Fall Times vs. Temperature



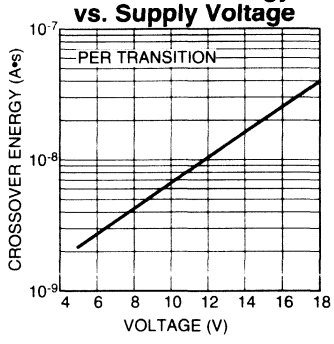
Rise Time vs. Capacitive Load



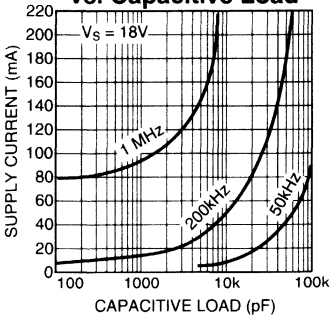
Fall Time vs. Capacitive Load



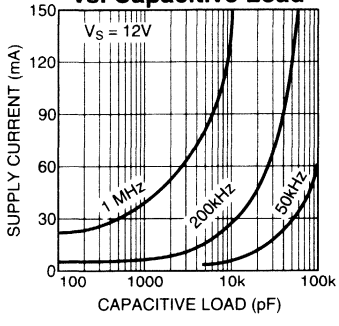
Crossover Energy vs. Supply Voltage



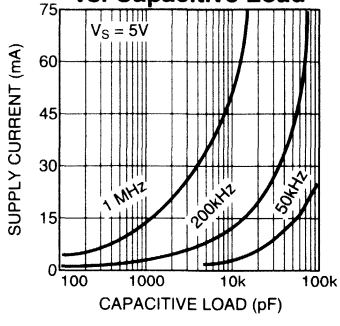
Supply Current vs. Capacitive Load



Supply Current vs. Capacitive Load

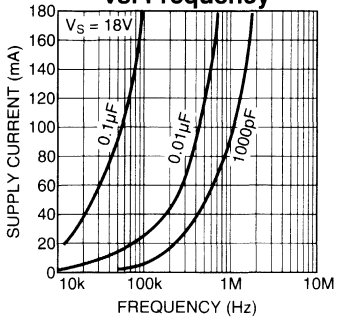


Supply Current vs. Capacitive Load

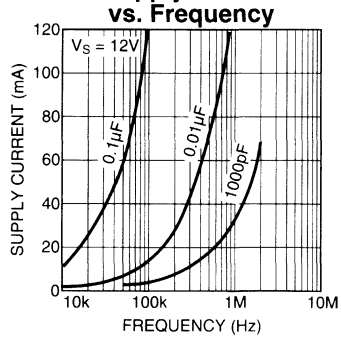


Typical Characteristic Curves (Cont.)

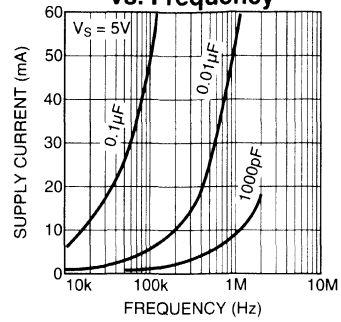
Supply Current vs. Frequency



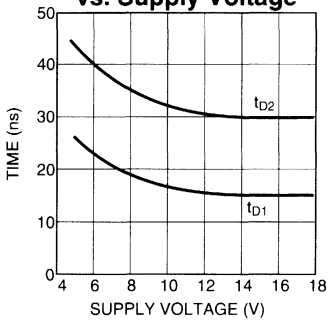
Supply Current vs. Frequency



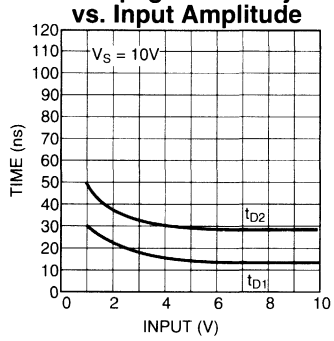
Supply Current vs. Frequency



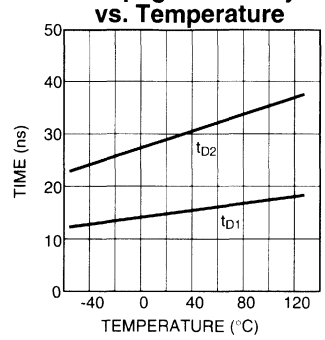
Propagation Delay vs. Supply Voltage



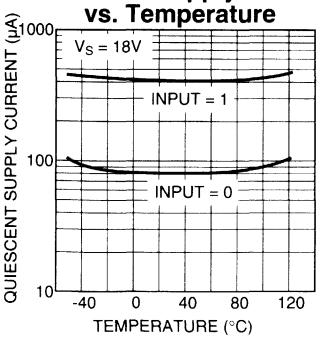
Propagation Delay vs. Input Amplitude



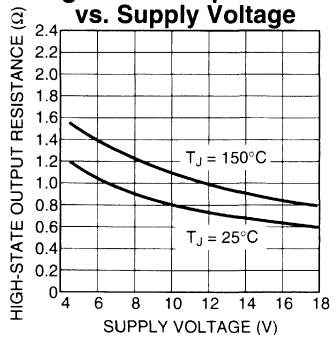
Propagation Delay vs. Temperature



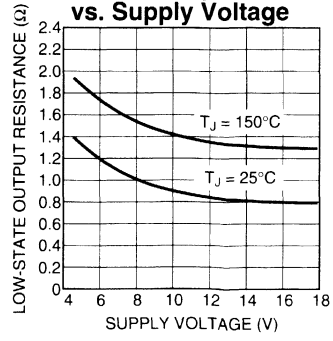
Quiescent Supply Current vs. Temperature



High-State Output Resist. vs. Supply Voltage



Low-State Output Resist. vs. Supply Voltage



Applications Information

Supply Bypassing

Charging and discharging large capacitive loads quickly requires large currents. For example, charging a 10,000pF load to 18V in 50ns requires 3.6A.

The MIC4421/4422 has double bonding on the supply pins, the ground pins and output pins. This reduces parasitic lead inductance. Low inductance enables large currents to be switched rapidly. It also reduces internal ringing that can cause voltage breakdown when the driver is operated at or near the maximum rated voltage.

Internal ringing can also cause output oscillation due to feedback. This feedback is added to the input signal since it is referenced to the same ground.

To guarantee low supply impedance over a wide frequency range, a parallel capacitor combination is recommended for supply bypassing. Low inductance ceramic disk capacitors with short lead lengths (< 0.5 inch) should be used. A 1µF low ESR film capacitor in parallel with two 0.1µF low ESR ceramic capacitors, (such as AVX RAM GUARD®), provides adequate bypassing. Connect one ceramic capacitor directly between pins 1 and 4. Connect the second ceramic capacitor directly between pins 8 and 5.

Grounding

The high current capability of the MIC4421/4422 demands careful PC board layout for best performance. Since the MIC4421 is an inverting driver, any ground lead impedance will appear as negative feedback which can degrade switching speed. Feedback is especially noticeable with slow-rise time inputs. The MIC4421 input structure includes about 200mV of hysteresis to ensure clean transitions and freedom from oscillation, but attention to layout is still recommended.

Figure 5 shows the feedback effect in detail. As the MIC4421 input begins to go positive, the output goes negative and several amperes of current flow in the ground lead. As little as 0.05Ω of PC trace resistance can produce hundreds of millivolts at the MIC4421 ground pins. If the driving logic is referenced to power ground, the effective logic input level is reduced and oscillation may result.

To insure optimum performance, separate ground traces should be provided for the logic and power connections. Connecting the logic ground directly to the MIC4421 GND pins will ensure full logic drive to the input and ensure fast output switching. Both of the MIC4421 GND pins should, however, still be connected to power ground.

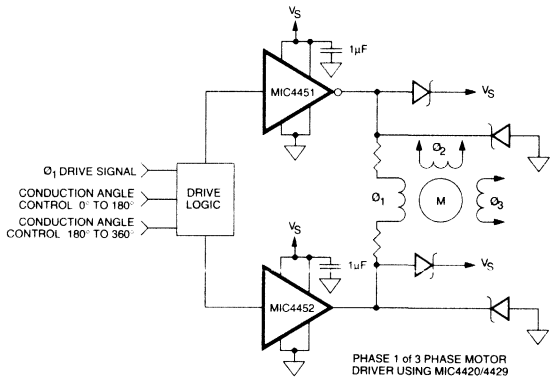
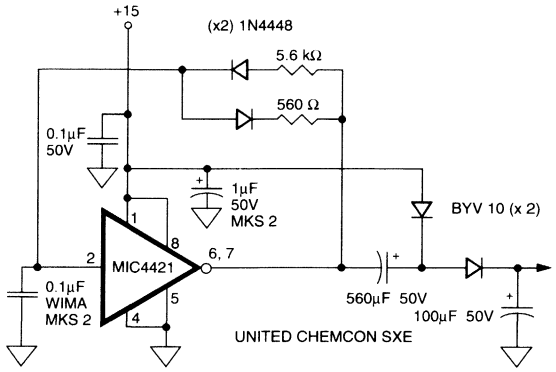


Figure 3. Direct Motor Drive



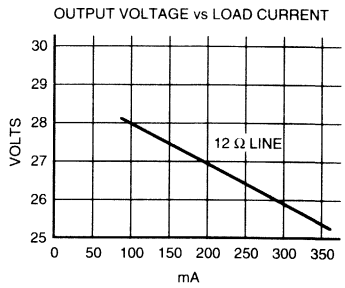


Figure 4. Self Contained Voltage Doubler

Input Stage

The input voltage level of the MIC4421 changes the quiescent supply current. The N channel MOSFET input stage transistor drives a 320µA current source load. With a logic "1" input, the maximum quiescent supply current is 400µA. Logic "0" input level signals reduce quiescent current to 80µA typical.

The MIC4421/4422 input is designed to provide 300mV of hysteresis. This provides clean transitions, reduces noise sensitivity, and minimizes output stage current spiking when changing states. Input voltage threshold level is approximately 1.5V, making the device TTL compatible over the full temperature and operating supply voltage ranges. Input current is less than ±10µA.

The MIC4421 can be directly driven by the TL494, SG1526/1527, SG1524, TSC170, MIC38C42, and similar switch mode power supply integrated circuits. By offloading the power-driving duties to the MIC4421/4422, the power supply controller can operate at lower dissipation. This can improve performance and reliability.

The input can be greater than the V_S supply, however, current will flow into the input lead. The input currents can be as high as 30mA p-p (6.4mA$_{RMS}$) with the input. No damage will occur to MIC4421/4422 however, and it will not latch.

The input appears as a 7pF capacitance and does not change even if the input is driven from an AC source. While the device will operate and no damage will occur up to 25V below the negative rail, input current will increase up to 1mA/V due to the clamping action of the input, ESD diode, and 1kΩ resistor.

Power Dissipation

CMOS circuits usually permit the user to ignore power dissipation. Logic families such as 4000 and 74C have outputs which can only supply a few milliamperes of current, and even shorting outputs to ground will not force enough current to destroy the device. The MIC4421/4422 on the other hand, can source or sink several amperes and drive large capacitive loads at high frequency. The package power dissipation limit can easily be exceeded. Therefore, some attention should be given to power dissipation when driving low impedance loads and/or operating at high frequency.

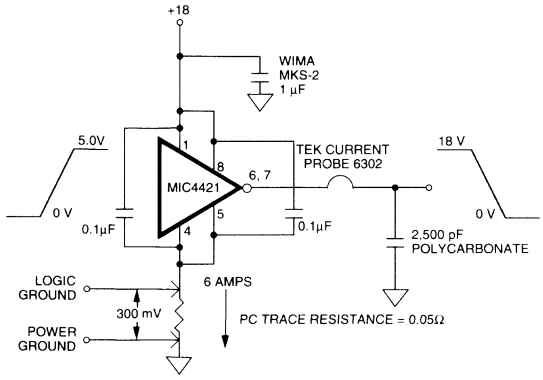


Figure 5. Switching Time Degradation Due to Negative Feedback

The supply current vs. frequency and supply current vs capacitive load characteristic curves aid in determining power dissipation calculations. Table 1 lists the maximum safe operating frequency for several power supply voltages when driving a 10,000pF load. More accurate power dissipation figures can be obtained by summing the three dissipation sources.

Given the power dissipation in the device, and the thermal resistance of the package, junction operating temperature for any ambient is easy to calculate. For example, the thermal resistance of the 8-pin CerDIP package, from the data sheet, is 150°C/W. In a 25°C ambient, then, using a maximum junction temperature of 150°C, this package will dissipate 800mW.

Accurate power dissipation numbers can be obtained by summing the three sources of power dissipation in the device:

- Load Power Dissipation (P_L)
- Quiescent power dissipation (P_Q)
- Transition power dissipation (P_T)

Calculation of load power dissipation differs depending on whether the load is capacitive, resistive or inductive.

Resistive Load Power Dissipation

Dissipation caused by a resistive load can be calculated as:

$$P_L = I^2 R_O D$$

where:

I = the current drawn by the load
R_O = the output resistance of the driver when the output is high, at the power supply voltage used. (See data sheet)
D = fraction of time the load is conducting (duty cycle)

Table 1: MIC4421 Maximum Operating Frequency

V_S	Max Frequency
18V	220kHz
15V	300kHz
10V	640kHz
5V	2MHz

Conditions: 1. CerDIP Package (θ_{JA} = 150°C/W)
2. T_A = 25°C
3. C_L = 10,000pF

Capacitive Load Power Dissipation

Dissipation caused by a capacitive load is simply the energy placed in, or removed from, the load capacitance by the driver. The energy stored in a capacitor is described by the equation:

$$E = 1/2\ C\ V^2$$

As this energy is lost in the driver each time the load is charged or discharged, for power dissipation calculations the 1/2 is removed. This equation also shows that it is good practice not to place more voltage in the capacitor than is necessary, as dissipation increases as the square of the voltage applied to the capacitor. For a driver with a capacitive load:

$$P_L = F\ C\ (V_S)^2$$

where:

F = Operating Frequency
C = Load Capacitance
V_S = Driver Supply Voltage

Inductive Load Power Dissipation

For inductive loads the situation is more complicated. For the part of the cycle in which the driver is actively forcing current into the inductor, the situation is the same as it is in the resistive case:

$$P_{L1} = I^2\ R_O\ D$$

However, in this instance the R_O required may be either the on resistance of the driver when its output is in the high state, or its on resistance when the driver is in the low state, depending on how the inductor is connected, and this is still only half the story. For the part of the cycle when the inductor is forcing current through the driver, dissipation is best described as

$$P_{L2} = I\ V_D\ (1 - D)$$

where V_D is the forward drop of the clamp diode in the driver (generally around 0.7V). The two parts of the load dissipation must be summed in to produce P_L

$$P_L = P_{L1} + P_{L2}$$

Quiescent Power Dissipation

Quiescent power dissipation (P_Q, as described in the input section) depends on whether the input is high or low. A low input will result in a maximum current drain (per driver) of ≤ 0.2mA; a logic high will result in a current drain of ≤ 3.0mA. Quiescent power can therefore be found from:

$$P_Q = V_S\ [D\ I_H + (1 - D)\ I_L]$$

where:

I_H = quiescent current with input high
I_L = quiescent current with input low
D = fraction of time input is high (duty cycle)
V_S = power supply voltage

Transition Power Dissipation

Transition power is dissipated in the driver each time its output changes state, because during the transition, for a very brief interval, both the N- and P-channel MOSFETs in the output totem-pole are ON simultaneously, and a current is conducted through them from V_S to ground. The transition power dissipation is approximately:

$$P_T = 2\ F\ V_S\ (A \bullet s)$$

where (A•s) is a time-current factor derived from the typical characteristic curve "Crossover Energy vs. Supply Voltage."

Total power (P_D) then, as previously described is just

$$P_D = P_L + P_Q + P_T$$

Definitions

C_L = Load Capacitance in Farads.

D = Duty Cycle expressed as the fraction of time the input to the driver is high.

F = Operating Frequency of the driver in Hertz

I_H = Power supply current drawn by a driver when both inputs are high and neither output is loaded.

I_L = Power supply current drawn by a driver when both inputs are low and neither output is loaded.

I_D = Output current from a driver in Amps.

P_D = Total power dissipated in a driver in Watts.

P_L = Power dissipated in the driver due to the driver's load in Watts.

P_Q = Power dissipated in a quiescent driver in Watts.

P_T = Power dissipated in a driver when the output changes states ("shoot-through current") in Watts. NOTE: The "shoot-through" current from a dual transition (once up, once down) for both drivers is stated in Figure 7 in ampere-nanoseconds. This figure must be multiplied by the number of repetitions per second (frequency) to find Watts.

R_O = Output resistance of a driver in Ohms.

V_S = Power supply voltage to the IC in Volts.

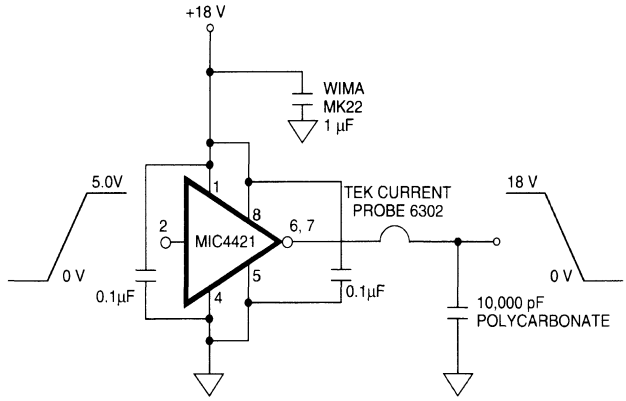


Figure 6. Peak Output Current Test Circuit

MIC4423/4424/4425

3A Dual High Speed MOSFET Driver

Bipolar/CMOS/DMOS Process

General Description

The MIC4423/4424/4425 family of parts are CMOS buffer/drivers built using a highly reliable BCD process. They are higher output current versions of the new MIC4426 family of buffer/drivers, which, in turn, are improved versions of the MIC426/427/428 family. All three families are pin-compatible. The MIC4423/24/25 drivers are capable of giving reliable service in far more demanding electrical environments than their antecedents. They will not latch under any conditions within their power and voltage ratings. They are not subject to damage when up to 5V of noise spiking, of either polarity, occurs on the ground pin. They can accept, without either damage or logic upset, up to half an amp of reverse current (of either polarity) being forced back into their outputs.

As a result, the MIC4423/24/25 series drivers are much easier to use, more flexible in operation, and much more forgiving than any other driver, CMOS or bipolar, currently available. Because they are fabricated in BiCMOS/DMOS, they dissipate a minimum of power, and provide rail-to-rail voltage swings to better insure the logic state of any load they drive.

Although primarily intended for driving power MOSFETs, the 4423/4424/4425 series drivers are equally well suited to driving any other load (capacitive, resistive, or inductive) which requires a low-impedance driver capable of high peak currents and fast switching times. For example, heavily loaded clock lines, coaxial cables, or piezoelectric transducers all can be driven from the MIC4423/24/25. The only known limitation on loading is that total power dissipated in the driver must be kept within the maximum power dissipation limits of the package.

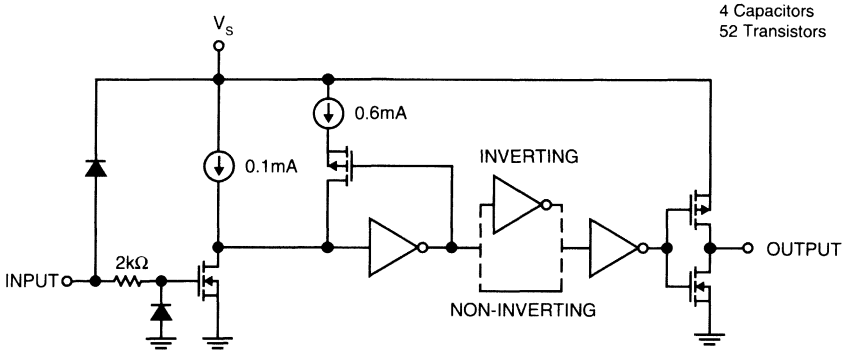
Features

- Built using reliable, low power Bipolar/CMOS/DMOS process
- Latch-Up Protected: Withstands >500mA Reverse Current
- Logic Input Will Withstand Negative Swing to –5V
- High Peak Output Current ..... 3A Peak
- Wide Operating Range ..... 4.5V to 18V
- High Capacitive Load Drive Capability ..... 1800pF in 25ns
- Short Delay Times ..... <40ns typ.
- Consistent Delay Times with Changes in Supply Voltage
- Matched Rise and Fall Times
- Logic High Input for Any Voltage From 2.4V to V_S
- Logic Input Threshold Independent of Supply Voltage
- Low Equivalent Input Capacitance (typ) 6pF
- Low Supply Current
  - 3.5mA with Logic 1 Inputs
  - 350µA with Logic 0 Inputs
- Low Output Impedance ..... 3.5Ω typ.
- Output Voltage Swing to Within 25mV of Ground or V_S
- Pin-Out Same as MIC426/427/428
- Available in Inverting, Non-Inverting, and Differential Configurations
- ESD Protected
- MIL-STD-883 Method 5004/5005 version available

As MOSFET drivers, the MIC4423/24/25 can easily switch 1800pF gate capacitances in 25ns, and provide low enough impedances in both the ON and OFF states to assure that a MOSFET's intended state will not be affected even by large transients.

Functional Diagram

Integrated Component Count:
4 Resistors
4 Capacitors
52 Transistors



Functional Diagram for One Driver (Two Drivers per Package—Ground Unused Drivers)

Ordering Information

Part Number	Temperature Range	Package	Configuration
MIC4423CWM MIC4423BWM	0°C to +70°C –40°C to +85°C	16-Pin SO Wide	Dual Inverting
MIC4423CN MIC4423BN	0°C to +70°C –40°C to +85°C	8-Pin Plastic DIP	Dual Inverting
MIC4423AJ MIC4423AJB*	–55°C to +125°C –55°C to +125°C	8-Pin CerDIP	Dual Inverting SMD#5962-8850304PX
MIC4424CWM MIC4424BWM	0°C to +70°C –40°C to +85°C	16-Pin SO Wide	Dual Non-Inverting
MIC4424CN MIC4424BN	0°C to +70°C –40°C to +85°C	8-Pin Plastic DIP	Dual Non-Inverting
MIC4424AJ MIC4424AJB*	–55°C to +125°C –55°C to +125°C	8-Pin CerDIP	Dual Non-Inverting SMD#5962-8850305PX
MIC4425CWM MIC4425BWM	0°C to +70°C –40°C to +85°C	16-Pin SO Wide	Inverting + Non Inverting
MIC4425CN MIC4425BN	0°C to +70°C –40°C to +85°C	8-Pin Plastic DIP	Inverting + Non Inverting
MIC4425AJ MIC4425AJB*	–55°C to +125°C –55°C to +125°C	8-Pin CerDIP	Inverting + Non Inverting SMD#5962-8850306PX

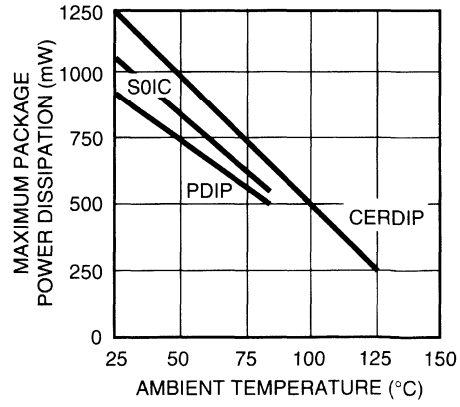
* AJB indicates units screened to MIL-STD 883, Method 5004, condition B, and burned-in for 1-week. Use SMD (Standard Military Drawing) number for ordering.

Absolute Maximum Ratings (Notes 1, 2, and 3)

If Military/Aerospace specified devices are required, contact Micrel for availability and specifications.

Supply Voltage	22V
Maximum Chip Temperature	150°C
Storage Temperature Range	–65°C to 150°C
Lead Temperature (10 sec.)	300°C
Package Thermal Resistance	
CERDIP $R_{\theta J-A}$	100°C/W
CERDIP $R_{\theta J-C}$	50°C/W
PDIP $R_{\theta J-A}$	130°C/W
PDIP $R_{\theta J-C}$	42°C/W
SOIC $R_{\theta J-A}$	120°C/W
SOIC $R_{\theta J-C}$	75°C/W
Operating Temperature Range	
C Version	0°C to +70°C
B Version	–40°C to +85°C
A Version	–55°C to +125°C

Package Power Dissipation



MIC4423/4424/4425 Electrical Characteristics:

Specifications measured at T_A = 25°C with 4.5V ≤ V_S ≤ 18V unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
INPUT						
V_{IH}	Logic 1 Input Voltage		2.4			V
V_{IL}	Logic 0 Input Voltage				0.8	V
I_{IN}	Input Current	0V ≤ V_{IN} ≤ V_S	−1		1	µA
OUTPUT						
V_{OH}	High Output Voltage		V_S−0.025			V
V_{OL}	Low Output Voltage				0.025	V
R_O	Output Resistance HI State	I_{OUT} = 10mA, V_S = 18V		2.8	5	Ω
R_O	Output Resistance LO State	I_{OUT} = 10mA, V_S = 18V		3.5	5	Ω
I_{PK}	Peak Output Current			3		A
I	Latch-Up Protection Withstand Reverse Current		>500			mA
SWITCHING TIME						
T_R	Rise Time	Test Figure 1, C_L = 1800pF		23	35	ns
T_F	Fall Time	Test Figure 1, C_L = 1800pF		25	35	ns
T_{D1}	Delay Time	Test Figure 1, C_L = 1800pF		33	75	ns
T_{D2}	Delay Time	Test Figure 1, C_L = 1800pF		38	75	ns
POWER SUPPLY						
I_S	Power Supply Current	V_{IN} = 3.0V (Both Inputs)		1.5	2.5	mA
I_S	Power Supply Current	V_{IN} = 0.0V (Both Inputs)		0.15	0.25	mA

MIC4423/4424/4425 Electrical Characteristics:

Specifications measured over operating temperature range with 4.5V ≤ V_S ≤ 18V unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
INPUT						
V_{IH}	Logic 1 Input Voltage		2.4			V
V_{IL}	Logic 0 Input Voltage				0.8	V
I_{IN}	Input Current	0 ≤ V_{IN} ≤ V_S	−10		10	µA
OUTPUT						
V_{OH}	High Output Voltage		V_S−0.025			V
V_{OL}	Low Output Voltage				0.025	V

MIC4423/4424/4425 Electrical Characteristics:

Specifications measured over operating temperature range with $4.5V \leq V_S \leq 18V$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OUTPUT						
R_O	Output Resistance, Output High	V_{IN} = 0.8V I_{OUT} = 10mA, V_S = 18V		3.7	8	Ω
R_O	Output Resistance, Output Low	V_{IN} = 2.4V I_{OUT} = 10mA, V_S = 18V		4.3	8	Ω
SWITCHING TIME						
T_R	Rise Time	Test Figure 1, C_L = 1800pF		28	60	ns
T_F	Fall Time	Test Figure 1, C_L = 1800pF		32	60	ns
T_{D1}	Delay TIme	Test Figure 1, C_L = 1800pF		32	100	ns
T_{D2}	Delay Time	Test Figure 1, C_L = 1800pF		38	100	ns
POWER SUPPLY						
I_S	Power Supply Current	V_{IN} = 3.0V (Both Inputs)		2	3.5	mA
I_S	Power Supply Current	V_{IN} = 0.0V (Both Inputs)		0.20	0.3	mA

Note 1: Functional operation above the absolute maximum stress ratings is not implied.
Note 2: Static Sensitive device. Unused devices must be stored in conductive material to protect devices from static discharge and static fields.
Note 3: Switching times guaranteed by design.

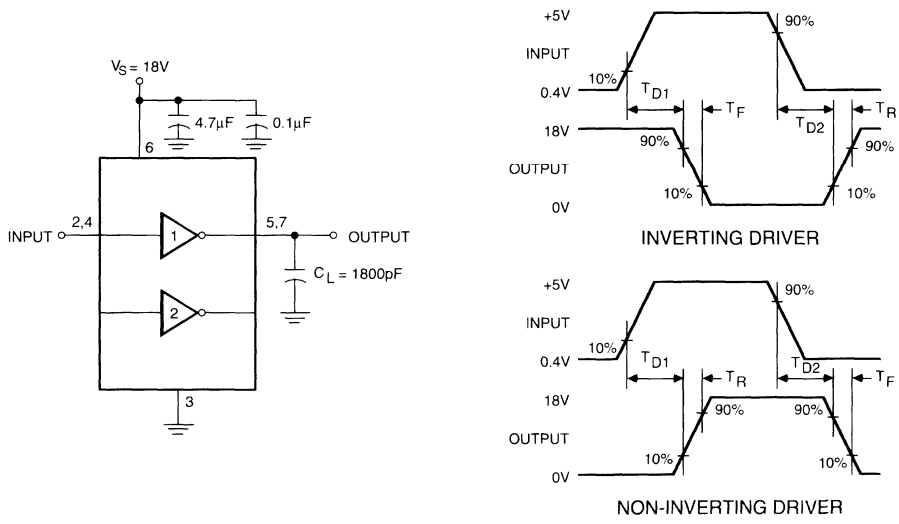
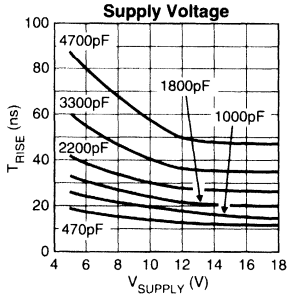


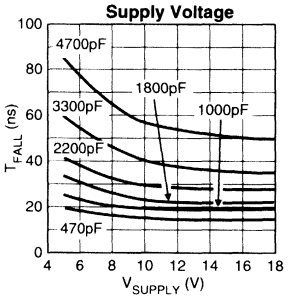
Figure 1. Switching Time Test Circuit

Typical Characteristic Curves

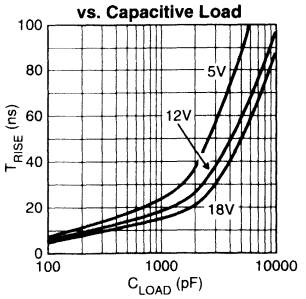
Rise Time vs. Supply Voltage



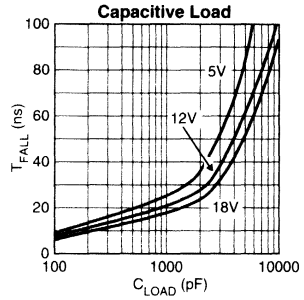
Fall Time vs. Supply Voltage



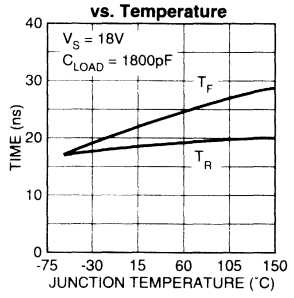
Rise Time vs. Capacitive Load



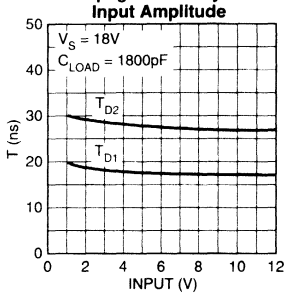
Fall Time vs. Capacitive Load



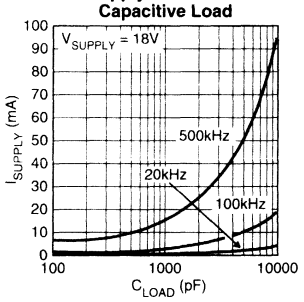
Rise and Fall Time vs. Temperature



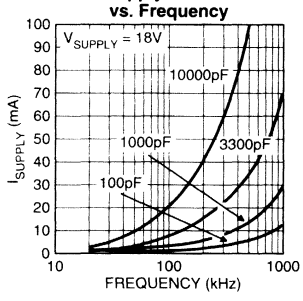
Propagation Delay vs. Input Amplitude



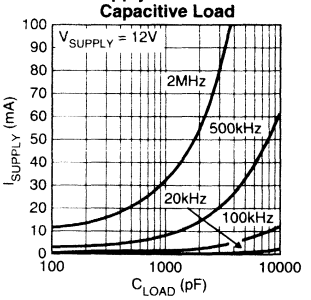
Supply Current vs. Capacitive Load



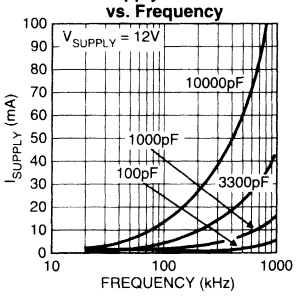
Supply Current vs. Frequency



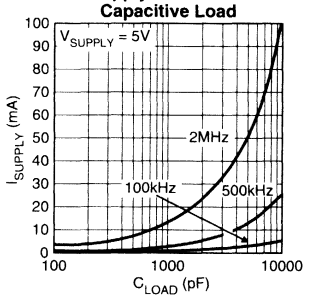
Supply Current vs. Capacitive Load



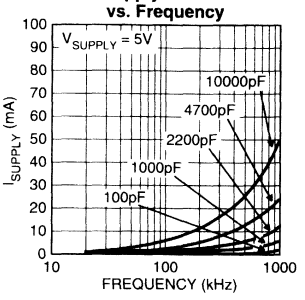
Supply Current vs. Frequency



Supply Current vs. Capacitive Load

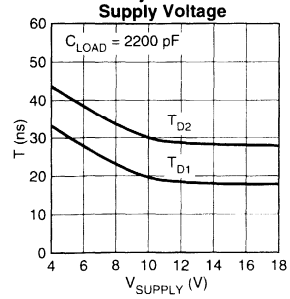


Supply Current vs. Frequency

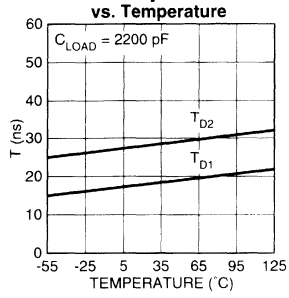


Typical Characteristic Curves (Continued)

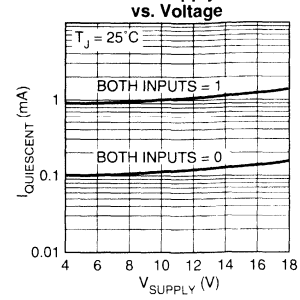
Delay Time vs. Supply Voltage



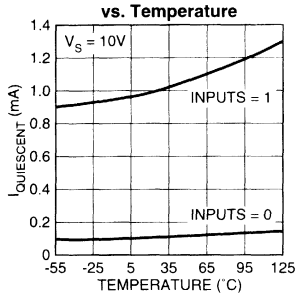
Delay Time vs. Temperature



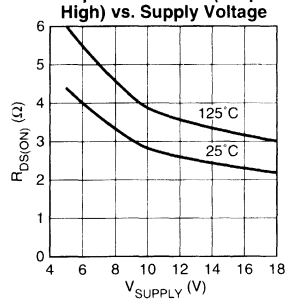
Quiescent Supply Current vs. Voltage



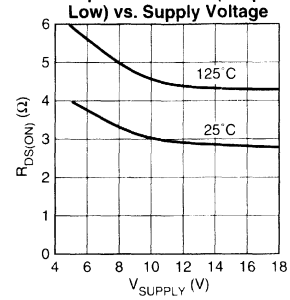
Quiescent Current vs. Temperature



Output Resistance (Output High) vs. Supply Voltage



Output Resistance (Output Low) vs. Supply Voltage



Application Information

Although the MIC4423/24/25 drivers have been specifically constructed to operate reliably under any practical circumstances, there are nonetheless details of usage which will provide better operation of the device.

Supply Bypassing

Charging and discharging large capacitive loads quickly requires large currents. For example, charging 2000pF from 0 to 15 volts in 20ns requires a constant current of 1.5A. In practice, the charging current is not constant, and will usually peak at around 3A. In order to charge the capacitor, the driver must be capable of drawing this much current, this quickly, from the system power supply. In turn, this means that as far as the driver is concerned, the system power supply, as seen by the driver, must have a **VERY** low impedance.

As a practical matter, this means that the power supply bus must be capacitively bypassed at the driver with at least 100X the load capacitance in order to achieve optimum driving speed. It also implies that the bypassing capacitor must have very low internal inductance and resistance at all frequencies of interest. Generally, this means using two capacitors, one a high-performance low ESR film, the other a low internal resistance ceramic, as together the valleys in their two impedance curves allow adequate performance over a broad enough band to get the job done. PLEASE NOTE that many film capacitors can be sufficiently inductive as to be useless for this service. Likewise, many multilayer ceramic capacitors have unacceptably high internal resistance. Use capacitors intended for high pulse current service (in-house we use WIMA™ film capacitors and AVX Ramguard™ ceramics; several other manufacturers of equivalent devices also exist). The high pulse current demands of capacitive drivers also mean that the bypass capacitors must be mounted very close to the driver in order to prevent the effects of lead inductance or PCB land inductance from nullifying what you are trying to accomplish. For optimum results the sum of the lengths of the leads and the lands from the capacitor body to the driver body should total 2.5cm or less.

Bypass capacitance, and its close mounting to the driver serves two purposes. Not only does it allow optimum performance from the driver, it minimizes the amount of lead length radiating at high frequency during switching, (due to the large Δ I) thus minimizing the amount of EMI later available for system disruption and subsequent cleanup. It should also be noted that the actual frequency of the EMI produced by a driver is not the clock frequency at which it is driven, but is related to the highest rate of change of current produced during switching, a frequency generally one or two orders of magnitude higher, and thus more difficult to filter if you let it permeate your system. ***Good bypassing practice is essential to proper operation of high speed driver ICs.***

Grounding

Both proper bypassing and proper grounding are necessary for optimum driver operation. Bypassing capacitance only allows a driver to turn the load ON. Eventually (except in rare circumstances) it is also necessary to turn the load OFF. This requires attention to the ground path. Two things other than the driver affect the rate at which it is possible to turn a load off: The adequacy of the grounding available for the driver, and the inductance of the leads from the driver to the load. The latter will be discussed in a separate section.

Best practice for a ground path is obviously a well laid out ground plane. However, this is not always practical, and a poorly-laid out ground plane can be worse than none. Attention to the paths taken by return currents even in a ground plane is essential. In general, the leads from the driver to its load, the driver to the power supply, and the driver to whatever is driving it should all be as low in resistance and inductance as possible. Of the three paths, the ground lead from the driver to the logic driving it is most sensitive to resistance or inductance, and ground current from the load are what is most likely to cause disruption. Thus, these ground paths should be arranged so that they never share a land, or do so for as short a distance as is practical.

To illustrate what can happen, consider the following: The inductance of a 2cm long land, 1.59mm (0.062") wide on a PCB with no ground plane is approximately 45nH. Assuming a dI/dt of 0.3A/ns (which will allow a current of 3A to flow after 10ns, and is thus slightly slow for our purposes) a voltage of 13.5 Volts will develop along this land in response to our postulated ΔI. For a 1cm land, (approximately 15nH) 4.5 Volts is developed. Either way, anyone using TTL-level input signals to the driver will find that the response of their driver has been seriously degraded by a common ground path for input to and output from the driver of the given dimensions. Note that this is before accounting for any resistive drops in the circuit. The resistive drop in a 1.59mm (0.062") land of 2oz. Copper carrying 3A will be about 4mV/cm (10mV/in) at DC, and the resistance will increase with frequency as skin effect comes into play.

The problem is most obvious in inverting drivers where the input and output currents are in phase so that any attempt to raise the driver's input voltage (in order to turn the driver's load off) is countered by the voltage developed on the common ground path as the driver attempts to do what it was supposed to. It takes very little common ground path, under these circumstances, to alter circuit operation drastically.

Output Lead Inductance

The same descriptions just given for PCB land inductance apply equally well for the output leads from a driver to its load, except that commonly the load is located much further away from the driver than the driver's ground bus.

Generally, the best way to treat the output lead inductance problem, when distances greater than 4cm (2") are involved, requires treating the output leads as a transmission line. Unfortunately, as both the output impedance of the driver and the input impedance of the MOSFET gate are at least an order of magnitude lower than the impedance of common coax, using coax is seldom a cost-effective solution. A twisted pair works about as well, is generally lower in cost, and allows use of a wider variety of connectors. The second wire of the

twisted pair should carry common from as close as possible to the ground pin of the driver directly to the ground terminal of the load. Do not use a twisted pair where the second wire in the pair is the output of the other driver, as this will not provide a complete current path for either driver. Likewise, do not use a twisted triad with two outputs and a common return unless both of the loads to be driver are mounted extremely close to each other, and you can guarantee that they will never be switching at the same time.

For output leads on a printed circuit, the general rule is to make them as short and as wide as possible. The lands should also be treated as transmission lines: i.e. minimize sharp bends, or narrowings in the land, as these will cause ringing. For a rough estimate, on a 1.59mm (0.062") thick G-10 PCB a pair of opposing lands each 2.36mm (0.093") wide translates to a characteristic impedance of about 50Ω. Half that width suffices on a 0.787mm (0.031") thick board. For accurate impedance matching with a MIC4423/24/25 driver, on a 1.59mm (0.062") board a land width of 42.75mm (1.683") would be required, due to the low impedance of the driver and (usually) its load. This is obviously impractical under most circumstances. Generally the tradeoff point between lands and wires comes when lands narrower than 3.18mm (0.125") would be required on a 1.59mm (0.062") board.

To obtain minimum delay between the driver and the load, it is considered best to locate the driver as close as possible to the load (using adequate bypassing). Using matching transformers at both ends of a piece of coax, or several matched lengths of coax between the driver and the load, works in theory, but is not optimum.

Driving At Controlled Rates

Occasionally there are situations where a controlled rise or fall time (which may be considerably longer than the normal rise or fall time of the driver's output) is desired for a load. In such cases it is still prudent to employ best possible practice in terms of bypassing, grounding and PCB layout, and then reduce the switching speed of the load (NOT the driver) by adding a noninductive series resistor of appropriate value between the output of the driver and the load. For situations where only rise or only fall should be slowed, the resistor can be paralleled with a fast diode so that switching in the other direction remains fast. Due to the Schmitt-trigger action of the driver's input it is not possible to slow the rate of rise (or fall) of the driver's input signal to achieve slowing of the output.

Input Stage

The input stage of the MIC4423/24/25 consists of a single-MOSFET class A stage with an input capacitance of ≤38pF. This capacitance represents the maximum load from the driver that will be seen by its controlling logic. The drain load on the input MOSFET is a –2mA current source. Thus, the quiescent current drawn by the driver varies, depending on the logic state of the input.

Following the input stage is a buffer stage which provides ~400mV of hysteresis for the input, to prevent oscillations when slowly-changing input signals are used or when noise is present on the input. Input voltage switching threshold is approximately 1.5V which makes the driver directly compatible with TTL signals, or with CMOS powered from any supply voltage between 3V and 15V.

The MIC4423/24/25 drivers can also be driven directly by the SG1524/25/26/27, TL494/95, TL594/95, NE5560/61/62/68, TSC170, MIC38C42, and similar switch mode power supply ICs. By relocating the main switch drive function into the driver rather than using the somewhat limited drive capabilities of a PWM IC. The PWM IC runs cooler, which generally improves its performance and longevity, and the main switches switch faster, which reduces switching losses and increase system efficiency.

The input protection circuitry of the MIC4423/24/25, in addition to providing 2kV or more of ESD protection, also works to prevent latchup or logic upset due to ringing or voltage spiking on the logic input terminal. In most CMOS devices when the logic input rises above the power supply terminal, or descends below the ground terminal, the device can be destroyed or rendered inoperable until the power supply is cycled OFF and ON. The MIC4423/24/25 drivers have been designed to prevent this. Input voltages excursions as great as 5V below ground will not alter the operation of the device. Input excursions above the power supply voltage will result in the excess voltage being conducted to the power supply terminal of the IC. Because the excess voltage is simply conducted to the power terminal, if the input to the driver is left in a high state when the power supply to the driver is turned off, currents as high as 30mA can be conducted through the driver from the input terminal to its power supply terminal. This may overload the output of whatever is driving the driver, and may cause other devices that share the driver's power supply, as well as the driver, to operate when they are assumed to be off, but it will not harm the driver itself. Excessive input voltage will also slow the driver down, and result in much longer internal propagation delays within the drivers. T_{D2}, for example, may increase to several hundred nanoseconds. In general, while the driver will accept this sort of misuse without damage, proper termination of the line feeding the driver so that line spiking and ringing are minimized, will always result in faster and more reliable operation of the device, leave less EMI to be filtered elsewhere, be less stressful to other components in the circuit, and leave less chance of unintended modes of operation.

Power Dissipation

CMOS circuits usually permit the user to ignore power dissipation. Logic families such as 4000 series and 74Cxxx have outputs which can only source or sink a few milliamps of current, and even shorting the output of the device to ground or V_{CC} may not damage the device. CMOS drivers, on the other hand, are intended to source or sink several Amps of current. This is necessary in order to drive large capacitive loads at frequencies into the megahertz range. Package power dissipation of driver ICs can easily be exceeded when driving large loads at high frequencies. Care must therefore be paid to device dissipation when operating in this domain.

The Supply Current vs Frequency and Supply Current vs Load characteristic curves furnished with this data sheet aid in estimating power dissipation in the driver. Operating frequency, power supply voltage, and load all affect power dissipation.

Given the power dissipation in the device, and the thermal resistance of the package, junction operating temperature for any ambient is easy to calculate. For example, the thermal resistance of the 8-pin CerDIP package, from the datasheet, is 150°C/W. In a 25°C ambient, then, using a maximum junction temperature of 150°C, this package will dissipate 800mW.

Accurate power dissipation numbers can be obtained by summing the three sources of power dissipation in the device:

- Load power dissipation (P_L)
- Quiescent power dissipation (P_Q)
- Transition power dissipation (P_T)

Calculation of load power dissipation differs depending on whether the load is capacitive, resistive or inductive.

Resistive Load Power Dissipation

Dissipation caused by a resistive load can be calculated as:

$$P_L = I^2 R_O D$$

where:

I = the current drawn by the load
R_O = the output resistance of the driver when the output is high, at the power supply voltage used (See characteristic curves)
D = fraction of time the load is conducting (duty cycle)

Capacitive Load Power Dissipation

Dissipation caused by a capacitive load is simply the energy placed in, or removed from, the load capacitance by the driver. The energy stored in a capacitor is described by the equation:

$$E = 1/2\ C\ V^2$$

As this energy is lost in the driver each time the load is charged or discharged, for power dissipation calculations the 1/2 is removed. This equation also shows that it is good practice not to place more voltage in the capacitor than is necessary, as dissipation increases as the square of the voltage applied to the capacitor. For a driver with a capacitive load:

$$P_L = F\ C\ (V_S)^2$$

where:

F = Operating Frequency
C = Load Capacitance
V_S = Driver Supply Voltage

Inductive Load Power Dissipation

For inductive loads the situation is more complicated. For the part of the cycle in which the driver is actively forcing current into the inductor, the situation is the same as it is in the resistive case:

$$P_{L1} = I^2 R_O D$$

However, in this instance the R_O required may be either the on resistance of the driver when its output is in the high state, or its on resistance when the driver is in the low state, depending on how the inductor is connected, and this is still only half the story. For the part of the cycle when the inductor is forcing current through the driver, dissipation is best described as

$$P_{L2} = I\ V_D\ (1 - D)$$

where V_D is the forward drop of the clamp diode in the driver (generally around 0.7V). The two parts of the load dissipation must be summed in to produce P_L

$$P_L = P_{L1} + P_{L2}$$

Quiescent Power Dissipation

Quiescent power dissipation (P_Q, as described in the input section) depends on whether the input is high or low. A low input will result in a maximum current drain (per driver) of ≤0.2mA; a logic high will result in a current drain of ≤2.0mA. Quiescent power can therefore be found from:

$$P_Q = V_S\ [D\ I_H + (1 - D)\ I_L]$$

where:

I_H = quiescent current with input high
I_L = quiescent current with input low
D = fraction of time input is high (duty cycle)
V_S = power supply voltage

Transition Power Dissipation

Transition power is dissipated in the driver each time its output changes state, because during the transition, for a very brief interval, both the N- and P-channel MOSFETs in the output totem-pole are ON simultaneously, and a current is conducted through them from V_S to ground. The transition power dissipation is approximately:

$$P_T = F\ V_S\ (A \bullet S)$$

where (A•S) is a time-current factor derived from Figure 2.

Total power (PD) then, as previously described is just

$$P_D = P_L + P_Q + P_T$$

Examples show the relative magnitude for each term.

EXAMPLE 1: A MIC4423 operating on a 12V supply driving two capacitive loads of 3000pF each, operating at 250kHz, with a duty cycle of 50%, in a maximum ambient of 60°C.

First calculate load power loss:

$$P_L = F \times C \times (V_S)^2$$
$$P_L = 250{,}000 \times (3 \times 10^{-6} + 3 \times 10^{-6}) \times 12^2$$
$$= 0.2160W$$

Then transition power loss:

$$P_T = F \times V_S \times (A \bullet S)$$
$$= 250{,}000 \bullet 12 \bullet 2.2 \times 10^{-9} = 6.6mW$$

Then quiescent power loss:

$$P_Q = V_S \times [D \times I_H + (1 - D) \times I_L]$$
$$= 12 \times [(0.5 \times 0.0035) + (0.5 \times 0.0003)]$$
$$= 0.0228W$$

Total power dissipation, then, is:

$$P_D = 0.2160 + 0.0066 + 0.0228$$
$$= 0.2454W$$

Assuming an SOIC package, with an $R_{\theta J\text{-}A}$ of 120°C/W, this will result in the junction running at:

$$0.2454 \times 120 = 29.4°C$$

above ambient, which, given a maximum ambient temperature of 60°C, will result in a maximum junction temperature of 89.4°C.

EXAMPLE 2: A MIC4424 operating on a 15V input, with one driver driving a 50Ω resistive load at 1MHz, with a duty cycle of 67%, and the other driver quiescent, in a maximum ambient temperature of 40°C:

$$P_L = I^2 \times R_O \times D$$

First, I_O must be determined.

$$I_O = V_S / (R_O + R_{LOAD})$$

Given R_O from the characteristic curves then,

$$I_O = 15 / (3.3 + 50)$$

$$I_O = 0.281A$$

and:

$$P_L = (0.281)^2 \times 3.3 \times 0.67$$
$$= 0.174W$$
$$P_T = F \times V_S \times (A \bullet S)/2$$

(because only one side is operating)

$$= (1{,}000{,}000 \times 15 \times 3.3 \times 10^{-9}) / 2$$
$$= 0.025\ W$$

and:

$$P_Q = 15 \times [(0.67 \times 0.00125) + (0.33 \times 0.000125) + (1 \times 0.000125)]$$

(this assumes that the unused side of the driver has its input grounded, which is more efficient)

$$= 0.015W$$

then:

$$P_D = 0.174 + 0.025 + 0.0150$$
$$= 0.213W$$

In a ceramic package with an $R_{\theta J\text{-}A}$ of 100°C/W, this amount of power results in a junction temperature given the maximum 40°C ambient of:

$$(0.213 \times 100) + 40 = 61.4°C$$

The actual junction temperature will be lower than calculated both because duty cycle is less than 100% and because the graph lists $R_{DS(on)}$ at a T_J of 125°C and the $R_{DS(on)}$ at 61°C T_J will be somewhat lower.

Definitions

C_L = Load Capacitance in Farads.

D = Duty Cycle expressed as the fraction of time the input to the driver is high.

F = Operating Frequency of the driver in Hertz

I_H = Power supply current drawn by a driver when both inputs are high and neither output is loaded.

I_L = Power supply current drawn by a driver when both inputs are low and neither output is loaded.

I_D = Output current from a driver in Amps.

P_D = Total power dissipated in a driver in Watts.

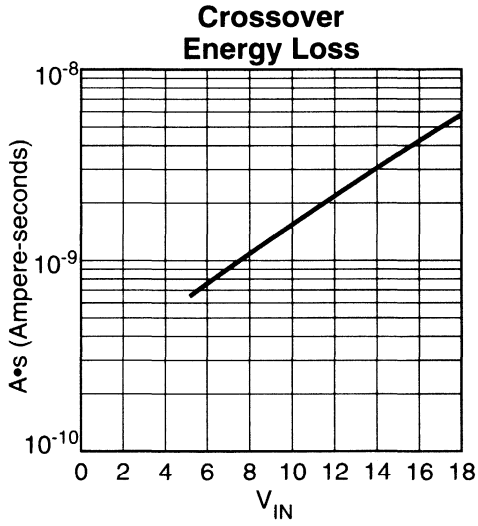
P_L = Power dissipated in the driver due to the driver's load in Watts.

P_Q = Power dissipated in a quiescent driver in Watts.

P_T = Power dissipated in a driver when the output changes states ("shoot-through current") in Watts. NOTE: The "shoot-through" current from a dual transition (once up, once down) for both drivers is stated in the graph on the following page in ampere-nanoseconds. This figure must be multiplied by the number of repetitions per second (frequency to find Watts).

R_O= Output resistance of a driver in Ohms.

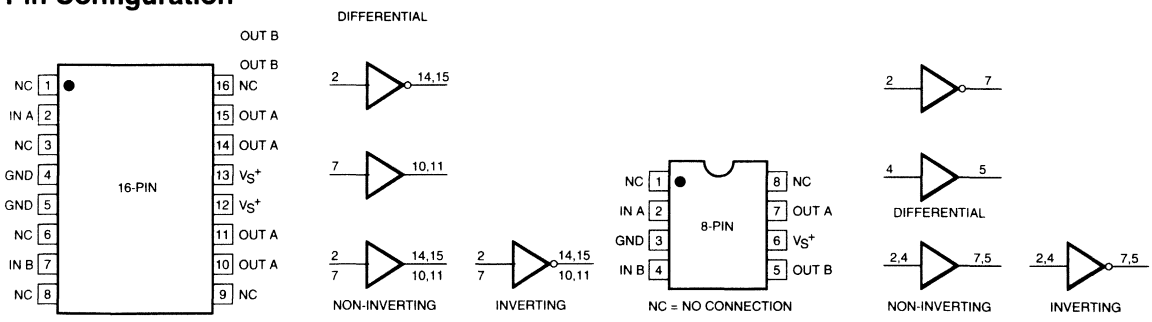
V_S= Power supply voltage to the IC in Volts.



NOTE: THE VALUES ON THIS GRAPH REPRESENT THE LOSS SEEN BY BOTH DRIVERS IN A PACKAGE DURING ONE COMPLETE CYCLE. FOR A SINGLE DRIVER DIVIDE THE STATED VALUES BY 2. FOR A SINGLE TRANSITION OF A SINGLE DRIVER, DIVIDE THE STATED VALUE BY 4.

Figure 2.

Pin Configuration



MIC4426/4427/4428

Dual High Speed MOSFET Driver

Bipolar/CMOS/DMOS Process

General Description

The MIC4426/4427/4428 family of buffer/drivers are built using a new, highly reliable BiCMOS/DMOS process. They are improved versions of the MIC426/427/428 family of buffer/drivers (with which they are pin compatible) and are capable of giving reliable service in far more demanding electrical environments: they will not latch under any conditions within their power and voltage ratings. They are not subject to damage when up to 5V of noise spiking, of either polarity, occurs on the ground pin. They can accept, without either damage or logic upset, up to half an amp of reverse current (of either polarity) being forced back into their outputs.

As a result, the MIC4426/27/28 series drivers are much easier to use, more flexible in operation, and much more forgiving than any other driver, CMOS or bipolar, currently available. Because they are fabricated in BiCMOS/DMOS, they dissipate a minimum of power, and provide rail-to-rail voltage swings to better insure the logic state of any load they are driving.

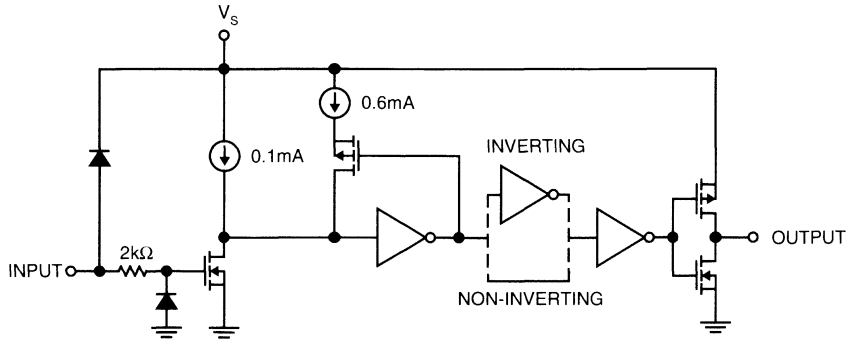
Although primarily intended for driving power MOSFETs, the 4426/4427/4428 series drivers are equally well suited to driving any other load (capacitive, resistive, or inductive) which requires a low-impedance driver capable of high peak currents and fast switching times. For example, heavily loaded clock lines, coaxial cables, or piezoelectric transducers all can be driven from the MIC4426/27/28. The only known limitation on loading is that total power dissipated in the driver must be kept within the maximum power dissipation limits of the package.

Features

- Built using reliable, low power Bipolar/CMOS/DMOS processes
- Latch-Up Protected: Withstands >500mA Reverse Current
- Logic Input Will Withstand Negative Swing Up to 5V
- High Peak Output Current ..... 1.5A Peak
- Wide Operating Range ..... 4.5V to 18V
- High Capacitive Load Drive Capability ..... 1000pF in 25ns
- Short Delay Times ..... <40ns typ.
- Consistent Delay Times with Changes in Supply Voltage
- Matched Rise and Fall Times
- Logic High Input for Any Voltage From 2.4V to V_S
- Logic Input Threshold Independent of Supply Voltage
- Low Equivalent Input Capacitance (typ) 6pF
- Low Supply Current
  - 4 mA with Logic 1 Inputs
  - 400 µA with Logic 0 Inputs
- Low Output Impedance 7Ω
- Output Voltage Swing to Within 25mV of Ground or V_S
- Pin-Out Same as MIC426/427/428
- Available in Inverting, Non-Inverting, and Differential Configurations
- ESD Protected
- MIL-STD-883 Method 5004/5005 version available

As MOSFET drivers, the MIC4426/27/28 can easily switch 1000pF gate capacitances in under 30ns, and provide low enough impedances in both the ON and OFF states to assure that a MOSFET's intended state will not be affected even by large transients.

Functional Diagram



Functional Diagram for One Driver (Two Drivers per Package—Ground Unused Drivers)

Ordering Information

Part Number	Temperature Range	Package	Configuration
MIC4426CM MIC4426BM	0°C to +70°C –40°C to+85°C	8-Pin SOIC	Dual Inverting
MIC4426CN MIC4426BN	0°C to +70°C –40°C to +85°C	8-Pin Plastic DIP	Dual Inverting
MIC4426AJ MIC4426AJB*	–55°C to +125°C –55°C to +125°C	8-Pin CerDIP	Dual Inverting SMD#5962-8850307PX
MIC4427CM MIC4427BM	0°C to +70°C –40°C to +85°C	8-Pin SOIC	Dual Non-Inverting
MIC4427CN MIC4427BN	0°C to +70°C –40°C to +85°C	8-Pin Plastic DIP	Dual Non-Inverting
MIC4427AJ MIC4427AJB*	–55°C to +125°C –55°C to +125°C	8-Pin CerDIP	Dual Non-Inverting SMD#5962-8850308PX
MIC4428CM MIC4428BM	0°C to +70°C –40°C to +85°C	8-Pin SOIC	Inverting + Non-Inverting
MIC4428CN MIC4428BN	0°C to +70°C –40°C to +85°C	8-Pin Plastic DIP	Inverting + Non-Inverting
MIC4428AJ MIC4428AJB*	–55°C to +125°C –55°C to +125°C	8-Pin CerDIP	Inverting + Non-Inverting SMD#5962-8850309PX
MIC4426CY MIC4427CY MIC4428CY	0°C to +70°C 0°C to +70°C 0°C to +70°C	Die Die Die	Dual Inverting Dual Non-Inverting Inverting + Non-Inverting

* AJB indicates units screened to MIL-STD 883, Method 5004, condition B, and burned-in for 1-week. Use SMD (Standard Military Drawing) number for ordering.

Absolute Maximum Ratings (Notes 1 and 2)

If Military/Aerospace specified devices are required, contact Micrel for availability and specifications.

Supply Voltage	22 V
Maximum Chip Temperature	150°C
Storage Temperature Range	–65°C to 150°C
Lead Temperature (10 sec.)	300°C
Package Thermal Resistance	
CERDIP $R_{\theta J\text{-}A}$	100°C/W
CERDIP $R_{\theta J\text{-}C}$	50°C/W
PDIP $R_{\theta J\text{-}A}$	130°C/W
PDIP $R_{\theta J\text{-}C}$	42°C/W
SOIC $R_{\theta J\text{-}A}$	120°C/W
SOIC $R_{\theta J\text{-}C}$	75°C/W
Operating Temperature Range	
C Version	0°C to +70°C
B Version	–40°C to +85°C
A Version	–55°C to +125°C

MIC4426/4427/4428 Electrical Characteristics:

Specifications measured at T_A = 25°C with 4.5V ≤ V_S ≤ 18V unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
INPUT						
V_{IH}	Logic 1 Input Voltage		2.4	1.4		V
V_{IL}	Logic 0 Input Voltage			1.1	0.8	V
I_{IN}	Input Current	0 ≤ V_{IN} ≤ V_S	−1		1	µA
OUTPUT						
V_{OH}	High Output Voltage		V_S–0.025			V
V_{OL}	Low Output Voltage				0.025	V
R_O	Output Resistance	I_{OUT} = 10mA, V_S = 18V		6	10	Ω
I_{PK}	Peak Output Current			1.5		A
I	Latch-Up Protection Withstand Reverse Current		>500			mA
SWITCHING TIME						
T_R	Rise Time	Test Figure 1		18	30	ns
T_F	Fall Time	Test Figure 1		23	30	ns
T_{D1}	Delay TIme	Test FIgure 1		17	30	ns
T_{D2}	Delay Time	Test Figure 1		23	50	ns
POWER SUPPLY						
I_S	Power Supply Current	V_{IN} = 3.0V (Both Inputs)		1.4	4.5	mA
I_S	Power Supply Current	V_{IN} = 0.0V (Both Inputs)		0.18	0.4	mA

MIC4426/4427/4428 Electrical Characteristics:

Specifications measured over operating temperature range with 4.5V ≤ V_S ≤ 18V unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
INPUT						
V_{IH}	Logic 1 Input Voltage		2.4	1.5		V
V_{IL}	Logic 0 Input Voltage			1.0	0.8	V
I_{IN}	Input Current	0 ≤ V_{IN} ≤ V_S	−1		1	µA
OUTPUT						
V_{OH}	High Output Voltage		V_S–0.025			V
V_{OL}	Low Output Voltage				0.025	V
R_O	Output Resistance	I_{OUT} = 10mA, V_S = 18V		8	12	Ω

MIC4426/4427/4428 Electrical Characteristics:

Specifications measured over operating temperature range with 4.5 V ≤ V_S ≤ 18 V unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OUTPUT						
I_{PK}	Peak Output Current			1.5		A
I	Latch-Up Protection Withstand Reverse Current		>500			mA
SWITCHING TIME						
T_R	Rise Time	Test Figure 1		20	40	ns
T_F	Fall Time	Test Figure 1		29	40	ns
T_{D1}	Delay TIme	Test FIgure 1		19	40	ns
T_{D2}	Delay Time	Test Figure 1		27	60	ns
POWER SUPPLY						
I_S	Power Supply Current	V_{IN} = 3.0 V (Both Inputs)		1.5	8	mA
I_S	Power Supply Current	V_{IN} = 0.0 V (Both Inputs)		0.19	0.6	mA

Note 1: Functional operation above the absolute maximum stress ratings is not implied.
Note 2: Static Sensitive device. Store only in conductive containers. Handling personnel and equipment should be grounded to prevent static damage.

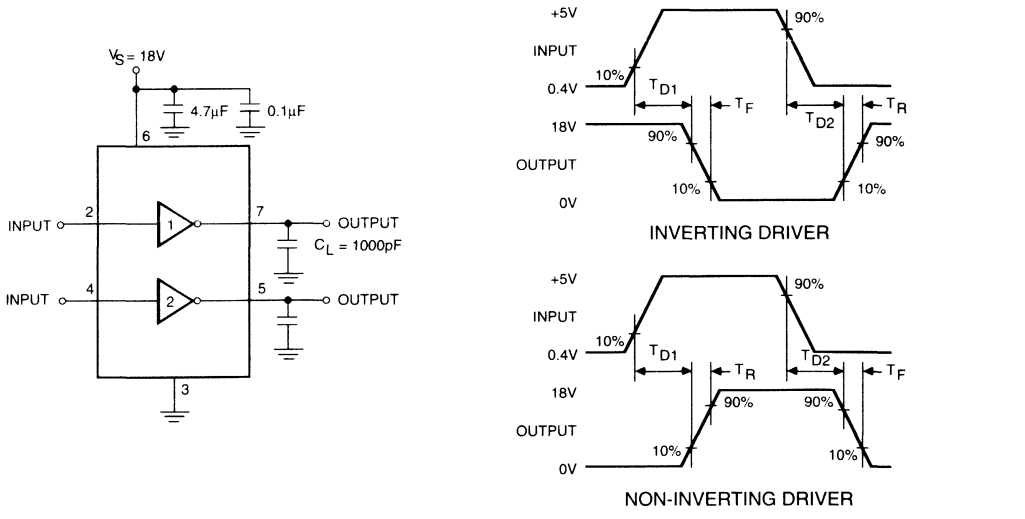
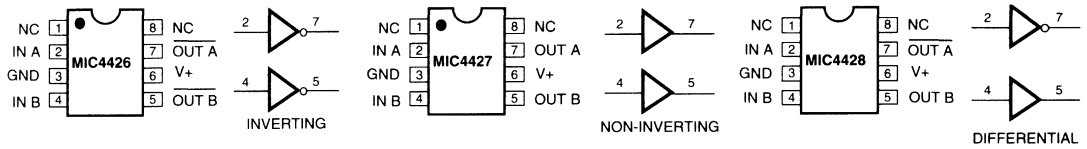


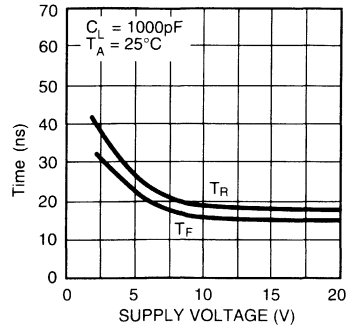
Figure 1. Switching Time Test Circuit

Pin Configuration

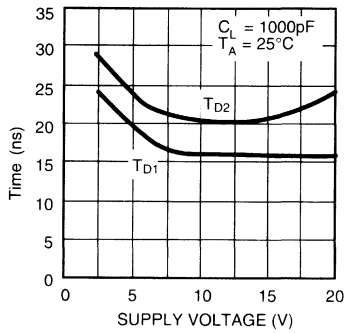


Typical Characteristic Curves

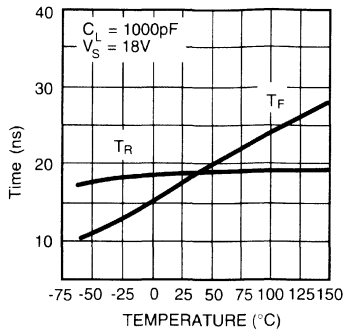
Rise and Fall Time vs. Supply Voltage



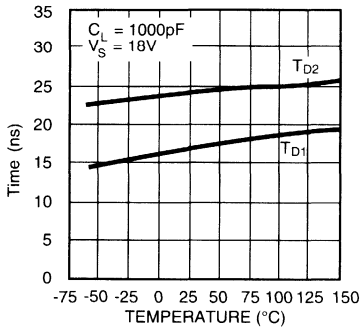
Delay Time vs. Supply Voltage



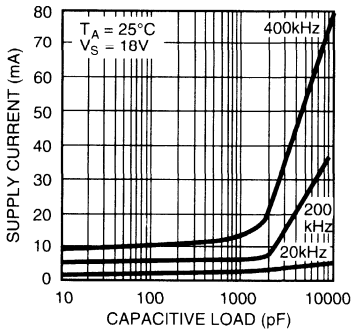
Rise and Fall Time vs. Temperature



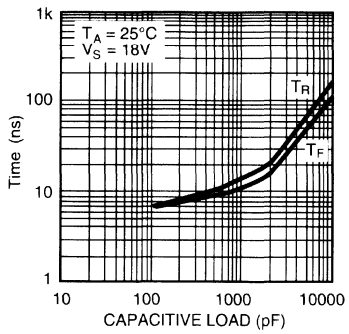
Delay Time vs. Temperature



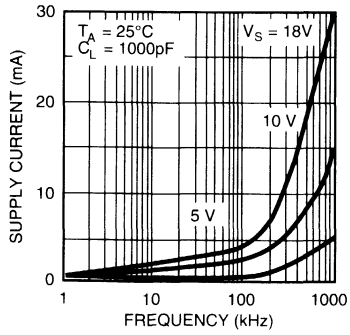
Supply Current vs. Capacitive Load



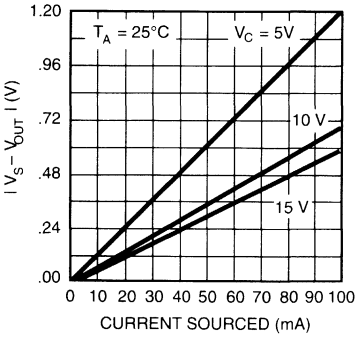
Rise and Fall Time vs. Capacitive Load



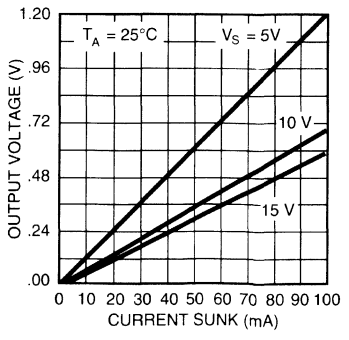
Supply Current vs. Frequency



High Output vs. Current

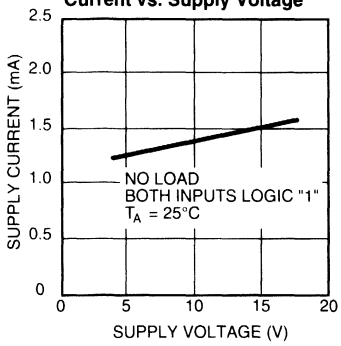


Low Output vs. Current

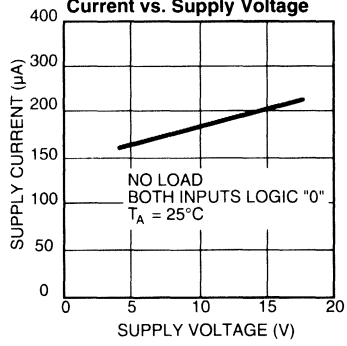


Typical Characteristic Curves (Continued)

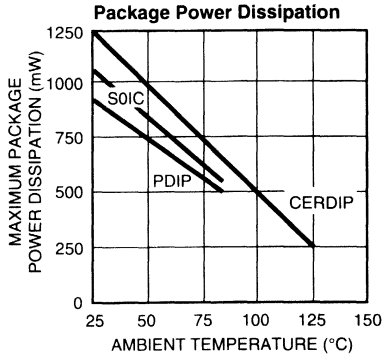
Quiescent Power Supply Current vs. Supply Voltage



Quiescent Power Supply Current vs. Supply Voltage

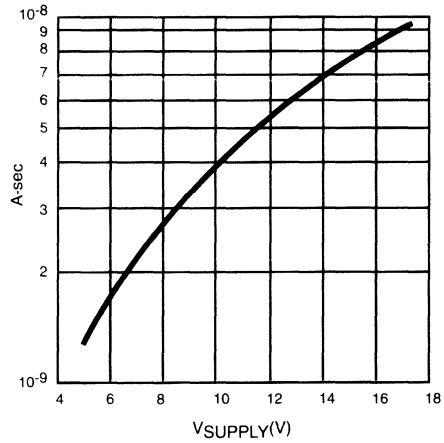


Package Power Dissipation



2

Crossover Energy Loss



Note: The values on this graph represent the loss seen by a single transition of a single driver. For a complete cycle of a single driver multiply the stated value by 2.

MIC4451/4452

12A High-Speed High-Current Single MOSFET Driver

Preliminary

General Description

MIC4451 and MIC4452 CMOS MOSFET drivers are tough, efficient, and easy to use. The MIC4451 is an inverting driver, while the MIC4452 is a non-inverting driver.

Both versions are capable of 12A (peak) output and can drive the largest MOSFETs with an improved safe operating margin. The MIC4451/4452 accepts any logic input from 2.4V to V_S without external speed-up capacitors or resistor networks. Proprietary circuits allow the input to swing negative by as much as 5V without damaging the part. Additional circuits protect against damage from electrostatic discharge.

MIC4451/4452 drivers can replace three or more discrete components, reducing PCB area requirements, simplifying product design, and reducing assembly cost.

Modern Bipolar/CMOS/DMOS construction guarantees freedom from latch-up. The rail-to-rail swing capability of CMOS/DMOS insures adequate gate voltage to the MOSFET during power up/down sequencing. Since these devices are fabricated on a self-aligned process, they have very low crossover current, run cool, use little power, and are easy to drive.

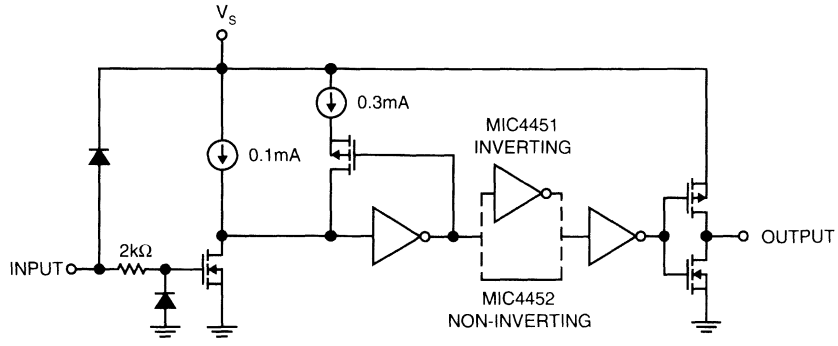
Features

- BiCMOS/DMOS Construction
- Latch-Up Proof: Fully Isolated Process is Inherently Immune to Any Latch-up.
- Input Will Withstand Negative Swing of Up to 5V
- Matched Rise and Fall Times 25ns
- High Peak Output Current ..... 12A Peak
- Wide Operating Range ..... 4.5V to 18V
- High Capacitive Load Drive 62,000pF
- Low Delay Time ..... 30ns Typ.
- Logic High Input for Any Voltage from 2.4V to V_S
- Low Supply Current ..... 450µA With Logic 1 Input
- Low Output Impedance 1.0Ω
- Output Voltage Swing to Within 25mV of GND or V_S
- MIL-STD-883 Method 5004/5005 Version Available
- Low Equivalent Input Capacitance (typ) 7pF

Applications

- Switch Mode Power Supplies
- Motor Controls
- Pulse Transformer Driver
- Class D Switching Amplifiers
- Line Drivers
- Driving MOSFET or IGBT Parallel Chip Modules
- Local Power ON/OFF Switch
- Pulse Generators

Functional Diagram

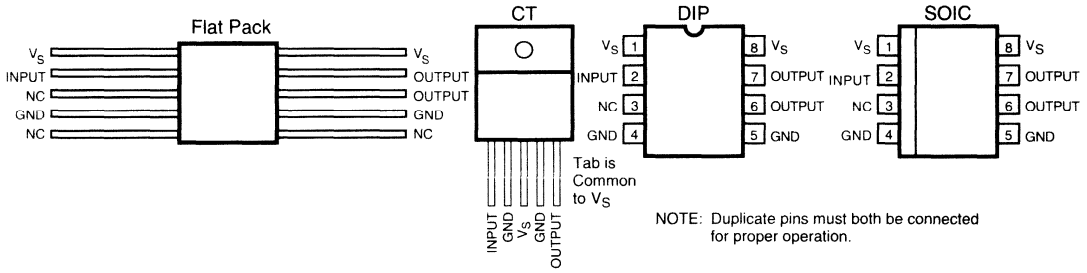


Ordering Information

Part No.	Temperature Range	Package	Configuration
MIC4451CN	0°C to +70°C	8-Pin PDIP	Inverting
MIC4451BN	–40°C to +85°C	8-Pin PDIP	Inverting
MIC4451CM	0°C to +70°C	8-Pin SOIC	Inverting
MIC4451BM	–40°C to +85°C	8-Pin SOIC	Inverting
MIC4451AJ	–55°C to +125°C	8-Pin CerDIP	Inverting
MIC4451AJB*	–55°C to +125°C	8-Pin CerDIP	Inverting
MIC4451AF	–55°C to +125°C	10-Pin Flat Pack	Inverting
MIC4451CT	0°C to +70°C	5-Pin TO-220	Inverting
MIC4452CN	0°C to +70°C	8-Pin PDIP	Non-Inverting
MIC4452BN	–40°C to +85°C	8-Pin PDIP	Non-Inverting
MIC4452CM	0°C to +70°C	8-Pin SOIC	Non-Inverting
MIC4452BM	–40°C to +85°C	8-Pin SOIC	Non-Inverting
MIC4452AJ	–55°C to +125°C	8-Pin CerDIP	Non-Inverting
MIC4452AJB*	–55°C to +125°C	8-Pin CerDIP	Non-Inverting
MIC4452AF	–55°C to +125°C	10-Pin Flat Pack	Non-Inverting
MIC4452CT	0°C to +70°C	5-Pin TO-220	Non-Inverting

* AJB indicates units screened to MIL-STD 883, Method 5004, condition B, and burned-in for 1-week.

Pin Configurations



Absolute Maximum Ratings (Notes 1, 2 and 3)

Power Dissipation, $T_{AMBIENT} \leq 25°C$
- PDIP 960mW
- SOIC 1040mW
- CerDIP 1250 mW
- 5-Pin TO-220 2W

Power Dissipation, $T_{CASE} \leq 25°C$
- 5-Pin TO-220 12.5W

Derating Factors (To Ambient)
- PDIP 7.7mW/°C
- SOIC 8.3 mW/°C
- CerDIP 10 mW/°C
- 5-Pin TO-220 17mW/°C

Thermal Impedances (To Case)
- 5-Pin TO-220 $R_{\theta J-C}$ 10°C/W

Storage Temperature –65°C to +150°C

Operating Temperature (Chip) 150°C

Operating Temperature (Ambient)
- C Version 0°C to +70°C
- B Version –40°C to +85°C
- A Version –55°C to +125°C

Lead Temperature (10 sec) 300°C

Supply Voltage 20V

Input Voltage V_S + 0.3V to GND – 5V

Input Current ($V_{IN} > V_S$) 50 mA

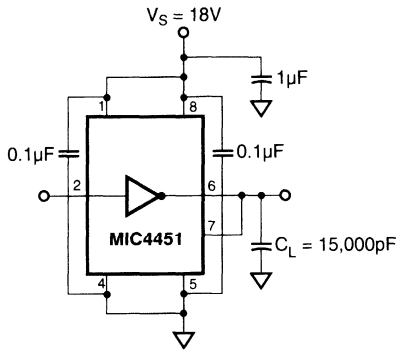
Electrical Characteristics: (T_A = 25°C with 4.5 V ≤ V_S ≤ 18 V unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
INPUT						
V_{IH}	Logic 1 Input Voltage		2.4	1.3		V
V_{IL}	Logic 0 Input Voltage			1.1	0.8	V
V_{IN}	Input Voltage Range		–5		V_S + 0.3	V
I_{IN}	Input Current	0 V ≤ V_{IN} ≤ V_S	–10		10	µA
OUTPUT						
V_{OH}	High Output Voltage	See Figure 1	V_S–0.025			V
V_{OL}	Low Output Voltage	See Figure 1			0.025	V
R_O	Output Resistance, Output High	I_{OUT} = 10 mA, V_S = 18 V		0.6	1.5	Ω
R_O	Output Resistance, Output Low	I_{OUT} = 10 mA, V_S = 18 V		0.8	1.5	Ω
I_{PK}	Peak Output Current	V_S = 18 V (See Figure 5)		12		A
I_{DC}	Continuous Output Current		2			A
I_R	Latch-Up Protection Withstand Reverse Current	Duty Cycle ≤ 2% t ≤ 300 µs	>1500			mA
SWITCHING TIME (Note 3)						
t_R	Rise Time	Test Figure 1, C_L = 15,000 pF		20	40	ns
t_F	Fall Time	Test Figure 1, C_L = 15,000 pF		24	50	ns
t_{D1}	Delay Time	Test Figure 1		15	30	ns
t_{D2}	Delay Time	Test Figure 1		35	60	ns
Power Supply						
I_S	Power Supply Current	V_{IN} = 3 V V_{IN} = 0 V		0.4 80	1.5 150	mA µA
V_S	Operating Input Voltage		4.5		18	V

Electrical Characteristics: (Over operating temperature range with 4.5V < V_S < 18V unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
INPUT						
V_{IH}	Logic 1 Input Voltage		2.4	1.4		V
V_{IL}	Logic 0 Input Voltage			1.0	0.8	V
V_{IN}	Input Voltage Range		–5		V_S + 0.3	V
I_{IN}	Input Current	0V ≤ V_{IN} ≤ V_S	–10		10	µA
OUTPUT						
V_{OH}	High Output Voltage	Figure 1	V_S–0.025			V
V_{OL}	Low Output Voltage	Figure 1			0.025	V
R_O	Output Resistance, Output High	I_{OUT} = 10mA, V_S = 18V		0.8	2.2	Ω
R_O	Output Resistance, Output Low	I_{OUT} = 10mA, V_S = 18V		1.3	2.2	Ω
SWITCHING TIME (Note 3)						
t_R	Rise Time	Figure 1, C_L = 15,000pF		23	50	ns
t_F	Fall Time	Figure 1, C_L = 15,000pF		30	60	ns
t_{D1}	Delay Time	Figure 1		20	40	ns
t_{D2}	Delay Time	Figure 1		40	80	ns
POWER SUPPLY						
I_S	Power Supply Current	V_{IN} = 3V V_{IN} = 0V		0.6 0.1	3 0.2	mA
V_S	Operating Input Voltage		4.5		18	V

NOTE 1: Functional operation above the absolute maximum stress ratings is not implied.
NOTE 2: Static-sensitive device. Store only in conductive containers. Handling personnel and equipment should be grounded to prevent damage from static discharge.
NOTE 3: Switching times guaranteed by design.



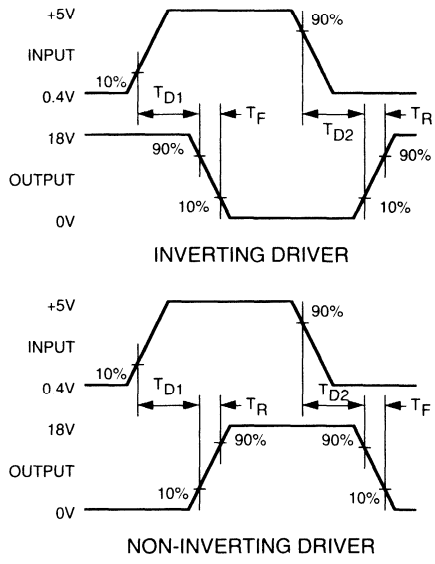
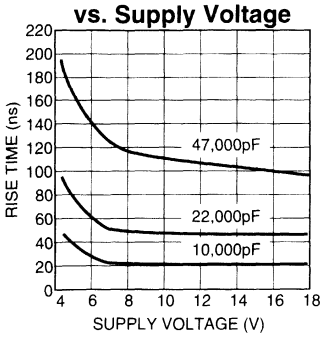


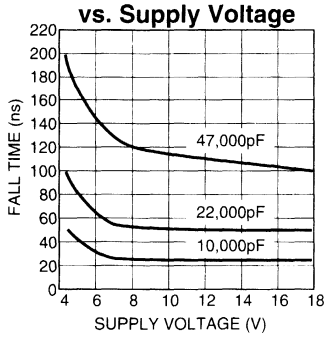
Figure 1. Switching Time Test Circuit

Typical Characteristic Curves

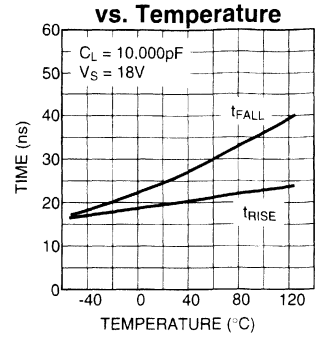
Rise Time vs. Supply Voltage



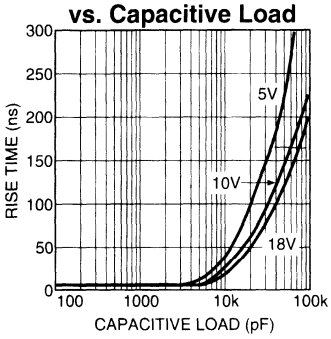
Fall Time vs. Supply Voltage



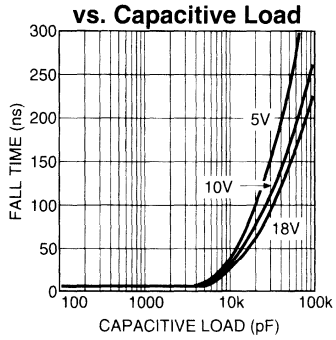
Rise and Fall Times vs. Temperature



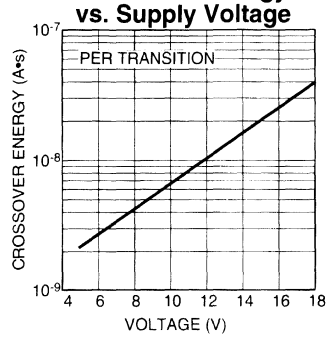
Rise Time vs. Capacitive Load



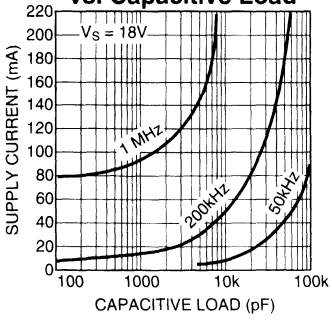
Fall Time vs. Capacitive Load



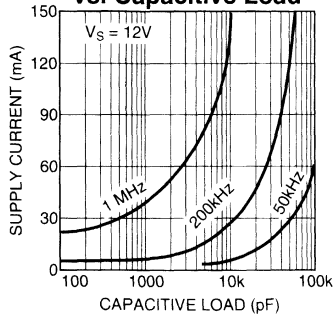
Crossover Energy vs. Supply Voltage



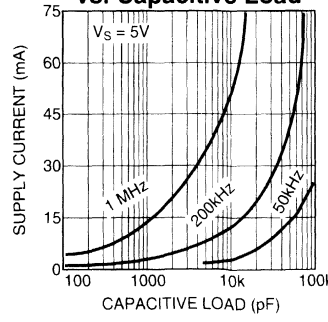
Supply Current vs. Capacitive Load



Supply Current vs. Capacitive Load

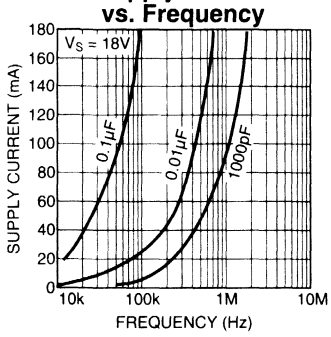


Supply Current vs. Capacitive Load

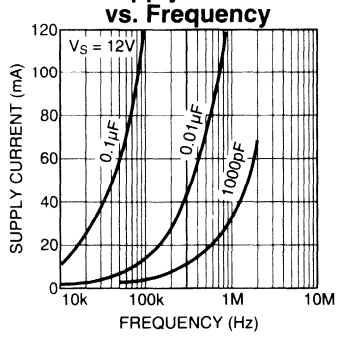


Typical Characteristic Curves (Cont.)

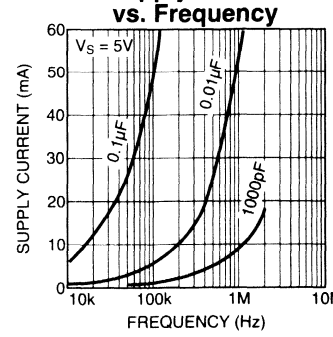
Supply Current vs. Frequency



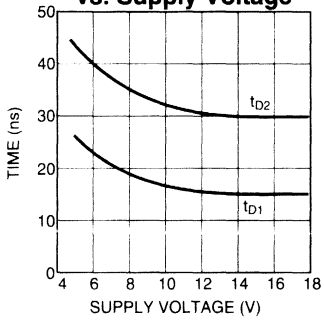
Supply Current vs. Frequency



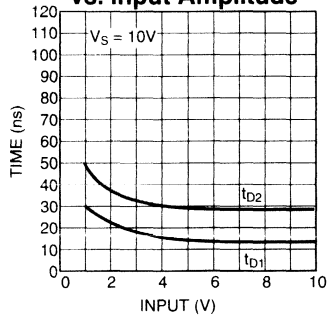
Supply Current vs. Frequency



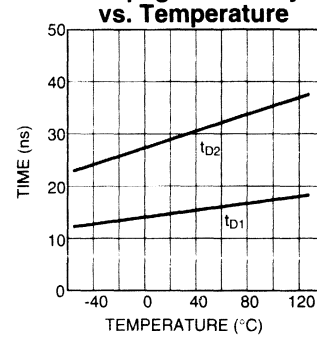
Propagation Delay vs. Supply Voltage



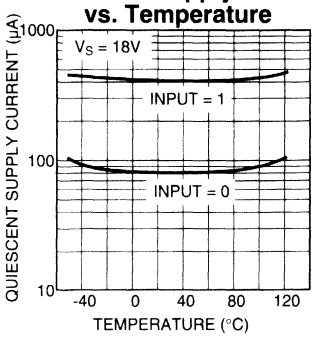
Propagation Delay vs. Input Amplitude



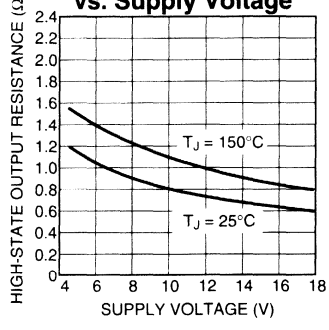
Propagation Delay vs. Temperature



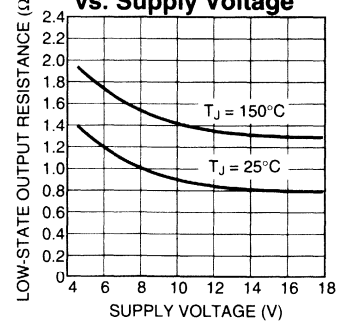
Quiescent Supply Current vs. Temperature



High-State Output Resist. vs. Supply Voltage



Low-State Output Resist. vs. Supply Voltage



Applications Information

Supply Bypassing

Charging and discharging large capacitive loads quickly requires large currents. For example, changing a 10,000pF load to 18V in 50ns requires 3.6A.

The MIC4451/4452 has double bonding on the supply pins, the ground pins and output pins. This reduces parasitic lead inductance. Low inductance enables large currents to be switched rapidly. It also reduces internal ringing that can cause voltage breakdown when the driver is operated at or near the maximum rated voltage.

Internal ringing can also cause output oscillation due to feedback. This feedback is added to the input signal since it is referenced to the same ground.

To guarantee low supply impedance over a wide frequency range, a parallel capacitor combination is recommended for supply bypassing. Low inductance ceramic disk capacitors with short lead lengths (< 0.5 inch) should be used. A 1µF low ESR film capacitor in parallel with two 0.1µF low ESR ceramic capacitors, (such as AVX RAM GUARD®), provides adequate bypassing. Connect one ceramic capacitor directly between pins 1 and 4. Connect the second ceramic capacitor directly between pins 8 and 5.

Grounding

The high current capability of the MIC4451/4452 demands careful PC board layout for best performance. Since the MIC4451 is an inverting driver, any ground lead impedance will appear as negative feedback which can degrade switching speed. Feedback is especially noticeable with slow-rise time inputs. The MIC4451 input structure includes 200mV of hysteresis to ensure clean transitions and freedom from oscillation, but attention to layout is still recommended.

Figure 5 shows the feedback effect in detail. As the MIC4451 input begins to go positive, the output goes negative and several amperes of current flow in the ground lead. As little as 0.05Ω of PC trace resistance can produce hundreds of millivolts at the MIC4451 ground pins. If the driving logic is referenced to power ground, the effective logic input level is reduced and oscillation may result.

To insure optimum performance, separate ground traces should be provided for the logic and power connections. Connecting the logic ground directly to the MIC4451 GND pins will ensure full logic drive to the input and ensure fast output switching. Both of the MIC4451 GND pins should, however, still be connected to power ground.

Input Stage

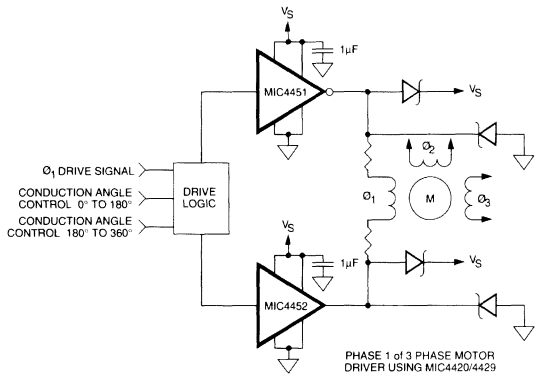
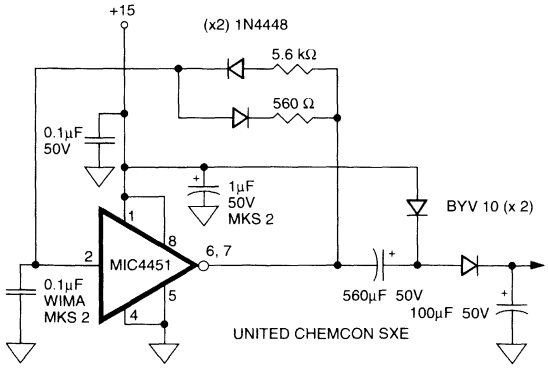


Figure 3. Direct Motor Drive



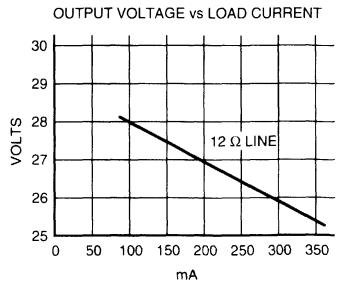


Figure 4. Self Contained Voltage Doubler

The input voltage level of the MIC4451 changes the quiescent supply current. The N channel MOSFET input stage transistor drives a 320µA current source load. With a logic "1" input, the maximum quiescent supply current is 400µA. Logic "0" input level signals reduce quiescent current to 80µA typical.

The MIC4451/4452 input is designed to provide 200mV of hysteresis. This provides clean transitions, reduces noise sensitivity, and minimizes output stage current spiking when changing states. Input voltage threshold level is approximately 1.5V, making the device TTL compatible over the full temperature and operating supply voltage ranges. Input current is less than ±10µA.

The MIC4451 can be directly driven by the TL494, SG1526/1527, SG1524, TSC170, MIC38C42, and similar switch mode power supply integrated circuits. By offloading the power-driving duties to the MIC4451/4452, the power supply controller can operate at lower dissipation. This can improve performance and reliability.

The input can be greater than the V_S supply, however, current will flow into the input lead. The input currents can be as high as 30mA p-p (6.4mA$_{RMS}$) with the input. No damage will occur to MIC4451/4452 however, and it will not latch.

The input appears as a 7pF capacitance and does not change even if the input is driven from an AC source. While the device will operate and no damage will occur up to 25V below the negative rail, input current will increase up to 1mA/V due to the clamping action of the input, ESD diode, and 1kΩ resistor.

Power Dissipation

CMOS circuits usually permit the user to ignore power dissipation. Logic families such as 4000 and 74C have outputs which can only supply a few milliamperes of current, and even shorting outputs to ground will not force enough current to destroy the device. The MIC4451/4452 on the other hand, can source or sink several amperes and drive large capacitive loads at high frequency. The package power dissipation limit can easily be exceeded. Therefore, some attention should be given to power dissipation when driving low impedance loads and/or operating at high frequency.

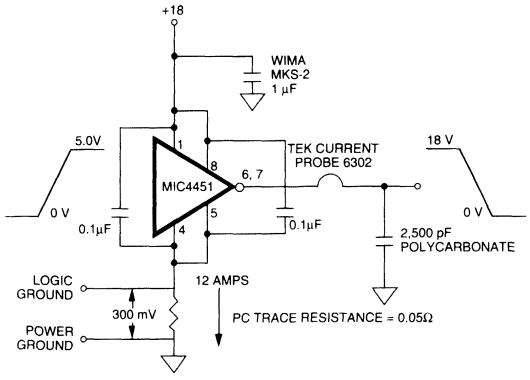


Figure 5. Switching Time Degradation Due to Negative Feedback

The supply current vs. frequency and supply current vs capacitive load characteristic curves aid in determining power dissipation calculations. Table 1 lists the maximum safe operating frequency for several power supply voltages when driving a 10,000pF load. More accurate power dissipation figures can be obtained by summing the three dissipation sources.

Given the power dissipation in the device, and the thermal resistance of the package, junction operating temperature for any ambient is easy to calculate. For example, the thermal resistance of the 8-pin CerDIP package, from the data sheet, is 100°C/W. In a 25°C ambient, then, using a maximum junction temperature of 125°C, this package will dissipate 1W.

Accurate power dissipation numbers can be obtained by summing the three sources of power dissipation in the device:

- Load Power Dissipation (P_L)
- Quiescent power dissipation (P_Q)
- Transition power dissipation (P_T)

Calculation of load power dissipation differs depending on whether the load is capacitive, resistive or inductive.

Resistive Load Power Dissipation

Dissipation caused by a resistive load can be calculated as:

$$P_L = I^2 R_O D$$

where:

I = the current drawn by the load
R_O = the output resistance of the driver when the output is high, at the power supply voltage used. (See data sheet)
D = fraction of time the load is conducting (duty cycle)

Capacitive Load Power Dissipation

Table 1: MIC4451 Maximum Operating Frequency

V_S	Max Frequency
18V	220kHz
15V	300kHz
10V	640kHz
5V	2MHz

Conditions: 1. CerDIP Package (θ_{JA} = 150°C/W)
2. T_A = 25°C
3. C_L = 10,000pF

Dissipation caused by a capacitive load is simply the energy placed in, or removed from, the load capacitance by the driver. The energy stored in a capacitor is described by the equation:

$$E = 1/2\ C\ V^2$$

As this energy is lost in the driver each time the load is charged or discharged, for power dissipation calculations the 1/2 is removed. This equation also shows that it is good practice not to place more voltage on the capacitor than is necessary, as dissipation increases as the square of the voltage applied to the capacitor. For a driver with a capacitive load:

$$P_L = F\ C\ (V_S)^2$$

where:

F = Operating Frequency
C = Load Capacitance
V_S = Driver Supply Voltage

Inductive Load Power Dissipation

For inductive loads the situation is more complicated. For the part of the cycle in which the driver is actively forcing current into the inductor, the situation is the same as it is in the resistive case:

$$P_{L1} = I^2\ R_O\ D$$

However, in this instance the R_O required may be either the on resistance of the driver when its output is in the high state, or its on resistance when the driver is in the low state, depending on how the inductor is connected, and this is still only half the story. For the part of the cycle when the inductor is forcing current through the driver, dissipation is best described as

$$P_{L2} = I\ V_D\ (1 - D)$$

where V_D is the forward drop of the clamp diode in the driver (generally around 0.7V). The two parts of the load dissipation must be summed in to produce P_L

$$P_L = P_{L1} + P_{L2}$$

Quiescent Power Dissipation

Quiescent power dissipation (P_Q, as described in the input section) depends on whether the input is high or low. A low input will result in a maximum current drain (per driver) of ≤ 0.2mA; a logic high will result in a current drain of ≤ 3.0mA. Quiescent power can therefore be found from:

$$P_Q = V_S\ [D\ I_H + (1 - D)\ I_L]$$

where:

I_H = quiescent current with input high
I_L = quiescent current with input low
D = fraction of time input is high (duty cycle)
V_S = power supply voltage

Transition Power Dissipation

Transition power is dissipated in the driver each time its output changes state, because during the transition, for a very brief interval, both the N- and P-channel MOSFETs in the output totem-pole are ON simultaneously, and a current is conducted through them from V_S to ground. The transition power dissipation is approximately:

$$P_T = 2\ F\ V_S\ (A \bullet S)$$

where (A•S) is a time-current factor derived from the typical characteristic curve "Crossover Energy vs. Supply Voltage."

Total power (P_D) then, as previously described is:

$$P_D = P_L + P_Q + P_T$$

Definitions

C_L = Load Capacitance in Farads.

D = Duty Cycle expressed as the fraction of time the input to the driver is high.

F = Operating Frequency of the driver in Hertz

I_H = Power supply current drawn by a driver when both inputs are high and neither output is loaded.

I_L = Power supply current drawn by a driver when both inputs are low and neither output is loaded.

I_D = Output current from a driver in Amps.

P_D = Total power dissipated in a driver in Watts.

P_L = Power dissipated in the driver due to the driver's load in Watts.

P_Q = Power dissipated in a quiescent driver in Watts.

P_T = Power dissipated in a driver when the output changes states ("shoot-through current") in Watts. NOTE: The "shoot-through" current from a dual transition (once up, once down) for both drivers is stated in Figure 7 in ampere-nanoseconds. This figure must be multiplied by the number of repetitions per second (frequency) to find Watts.

R_O = Output resistance of a driver in Ohms.

V_S = Power supply voltage to the IC in Volts.

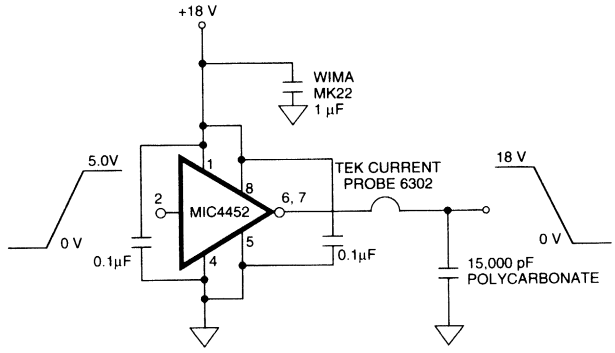


Figure 6. Peak Output Current Test Circuit

MIC4467/4468/4469

Power Logic CMOS Quad Drivers

Bipolar/CMOS/DMOS

General Description

The MIC4467/8/9 family of 4-output CMOS buffer/drivers is an expansion from the earlier single- and dual-output drivers, to which they are functionally closely related. Because package pin count permitted it, each driver has been equipped with a 2-input logic gate for added flexibility. Placing four high-power drivers in a single package also improves system reliability and reduces total system cost. In some applications, one of these drivers can replace not only two packages of single-input drivers, but some of the associated logic as well.

Although primarily intended for driving power MOSFETs, and similar highly capacitive loads, these drivers are equally well suited to driving any other load (capacitive, resistive, or inductive), which requires a high-efficiency, low-impedance driver capable of high peak currents, rail-to-rail voltage swings, and fast switching times. For example, heavily loaded clock lines, coaxial cables, and piezoelectric transducers can all be driven easily with MIC446X series drivers. The only limitation

Features

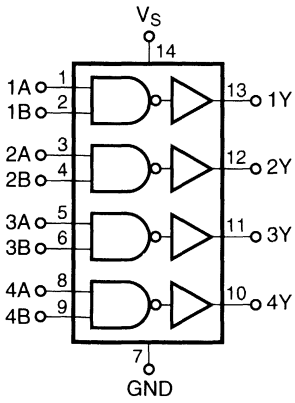
- Built using reliable, low power CMOS processes
- Latchproof. Withstands 500mA Inductive Kickback
- 3 Input Logic Choices
- Symmetrical Rise and Fall Times 25ns
- Short, Equal Delay Times 75ns
- High Peak Output Current 1.2A
- Wide Operating Range ..... 4.5 to 18V
- Low Equivalent Input Capacitance (typ) 6pF
- Inputs = Logic 1 for Any Input From 2.4V to V_S
- ESD Protected

Applications

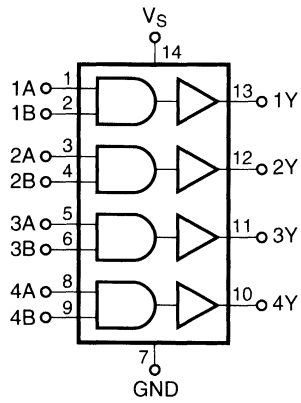
- General-Purpose CMOS Logic Buffer
- Driving All 4 MOSFETs in an H-Bridge
- Direct Small-Motor Driver
- Relay or Peripheral Drivers
- Dual Differential Output Power Drivers
- CCD Driver
- Pin-Switching Network Driver

Logic Diagrams

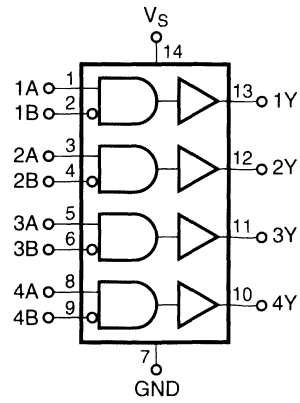
MIC4467



MIC4468



MIC4469



on loading is that total power dissipation in the IC must be kept within the power dissipation limits of the package.

The MIC446X series drivers are built using a BCD process. They will not latch under any conditions within their power and voltage ratings. They are not subject to damage when up to 5V of noise spiking (either polarity) occurs on the ground line. They can accept up to half an amp of inductive kickback current (either polarity) into their outputs without damage or logic upset.

Ordering Information

Part No.	Package	Temp. Range
MIC44**CN	14-Pin Plastic DIP	0° to +70°C
MIC44**CWM	16-Pin Wide SOIC	0° to +70°C
MIC44**BN	14-Pin Plastic DIP	–40° to +85°C
MIC44**BWM	16-Pin Wide SOIC	–40° to +85°C
MIC44**BJ	14-Pin CerDIP	–40° to +85°C
MIC44**AJB*	14-Pin CerDIP	–55° to +125°C
MIC44**AL	20-Pin LCC	–55° to +125°C
MIC44**CY	Die	0° to +70°C

* AJB indicates units screened to MIL-STD 883, Method 5004, condition B, and burned-in for 1-week.

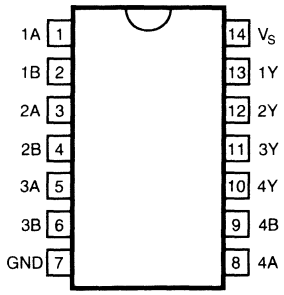
**Two digits must be added in this position to define the device logic:
67 — NAND 68 — AND
69 — AND with one inverting input

Truth Table

Part No.	Inputs A	Inputs B	Output Y
MIC4467 (Each Driver)	L	X	H
	X	L	H
	H	H	L
MIC4468 (Each Driver)	H	H	H
	L	X	L
	X	L	L
MIC4469 (Each Driver)	L	X	L
	X	H	L
	H	L	H

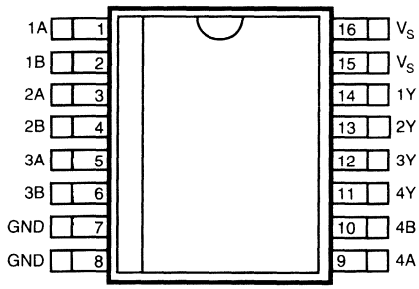
Pin Configurations

14-Pin Dual-In-Line Package - N, J



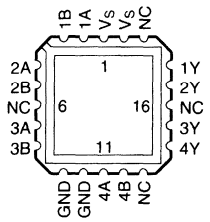
TOP VIEW

16-Pin Wide SOIC - WM

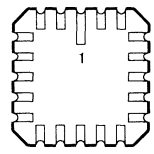


TOP VIEW

20-Pin LCC - L



TOP VIEW



BOTTOM VIEW

Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage	22V
Input Voltage	(GND – 5V) to (V_S + 0.3V)
Maximum Chip Temperature	
Operating	150°C
Storage	–65° to +150°C
Maximum Load Temperature	
(10 sec, for soldering)	300°C
Operating Ambient Temperature	
C Version	0° to +70°C
B Version	–40° to +85°C
A Version	–55° to +125°C

Power Dissipation	
P Package (14-Pin Plastic DIP)	1.5W
WM Package (16-Pin Wide SOIC)	1W
J Package (14-Pin CerDIP)	1.25W
L Package (20-Pin LCC)	1W
Package Thermal Resistance	
P Package (14-Pin Plastic DIP) $R_{\theta J-A}$	80°C/W
WM Package (16-Pin Wide SOIC) $R_{\theta J-A}$	120°C/W
J Package (14-Pin CerDIP) $R_{\theta J-A}$	100°C/W
L Package (20-Pin LCC) $R_{\theta J-A}$	120°C/W

Electrical Characteristics: Measured at T_A = 25°C with 4.5V ≤ V_S ≤ 18V unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
INPUT						
V_{IH}	Logic 1 Input Voltage		2.4	1.3		V
V_{IL}	Logic 0 Input Voltage			1.2	0.8	V
I_{IN}	Input Current	$0 \le V_{IN} \le V_S$	–1		1	µA
OUTPUT						
V_{OH}	High Output Voltage	I_{LOAD} = 10mA	V_S-0.15			V
V_{OL}	Low Output Voltage	I_{LOAD} = 10mA			0.15	V
R_O	Output Resistance	I_{OUT} = 10mA, V_S = 18V		5	15	Ω
I_{PK}	Peak Output Current			1.2		A
I	Latch-Up Protection Withstand Reverse Current		>500			mA
SWITCHING TIME						
t_R	Rise Time	Test Figure 1		14	25	ns
t_F	Fall Time	Test Figure 1		13	25	ns
t_{D1}	Delay Time	Test Figure 1		30	75	ns
t_{D2}	Delay Time	Test Figure 1		45	75	ns
POWER SUPPLY						
I_S	Power Supply Current Supply			0.2	4	mA

Electrical Characteristics:

Measured over operating temperature range with $4.5V \leq V_S \leq 18V$ unless otherwise specified.

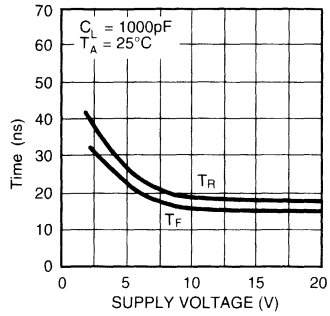
Symbol	Parameter	Conditions	Min	Typ	Max	Units
INPUT						
V_{IH}	Logic 1 Input Voltage		2.4	1.4		V
V_{IL}	Logic 0 Input Voltage			1.0	0.8	V
I_{IN}	Input Current	$0 \leq V_{IN} \leq V_S$	–1		1	µA
OUTPUT						
V_{OH}	High Output Voltage	I_{LOAD} = 10 mA	V_S-0.3			V
V_{OL}	Low Output Voltage	I_{LOAD} = 10 mA			0.3	V
R_O	Output Resistance	I_{OUT} = 10 mA, V_S = 18V		7	30	Ω
I_{PK}	Peak Output Current			1.2		A
I	Latch-Up Protection Withstand Reverse Current		500			mA
SWITCHING TIME						
t_R	Rise Time	Test Figure 1		17	50	ns
t_F	Fall Time	Test Figure 1		16	50	ns
t_{D1}	Delay Time	Test Figure 1		35	100	ns
t_{D2}	Delay Time	Test Figure 1		55	100	ns
POWER SUPPLY						
I_S	Power Supply Current Supply			0.4	8	mA

NOTE 1: Functional operation above the absolute maximum stress ratings is not implied.

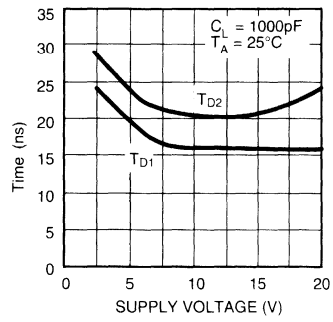
NOTE 2: Static sensitive device. Store only in conductive containers. Handling personnel and equipment should be grounded to prevent static damage.

Typical Characteristics

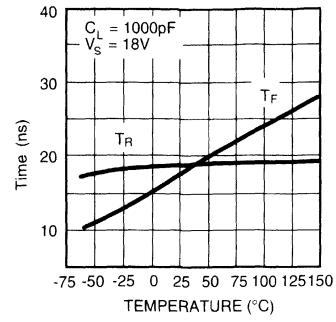
Rise and Fall Time vs. Supply Voltage



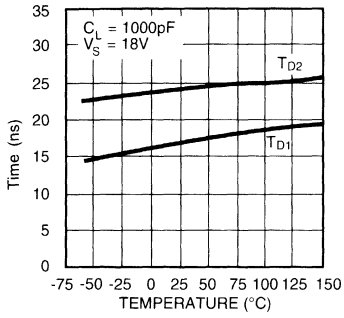
Delay Time vs. Supply Voltage



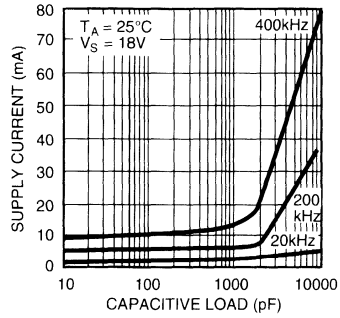
Rise and Fall Time vs. Temperature



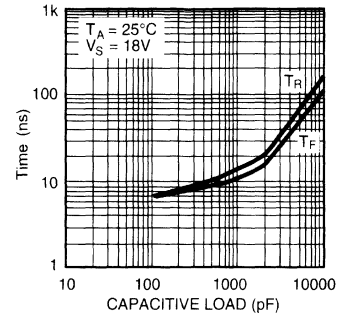
Delay Time vs. Temperature



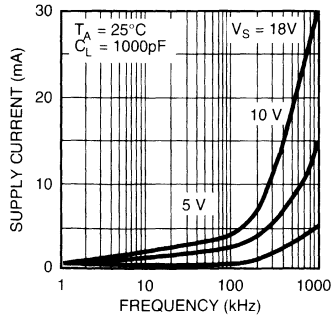
Supply Current vs. Capacitive Load



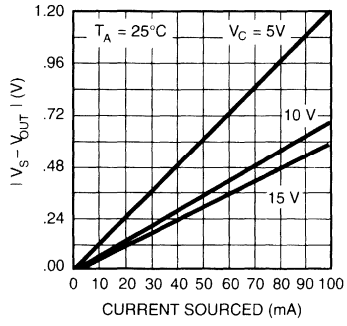
Rise and Fall Time vs. Capacitive Load



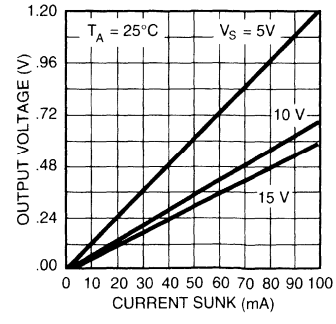
Supply Current vs. Frequency

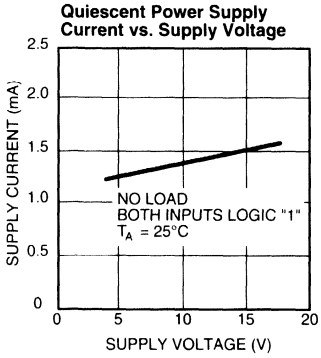


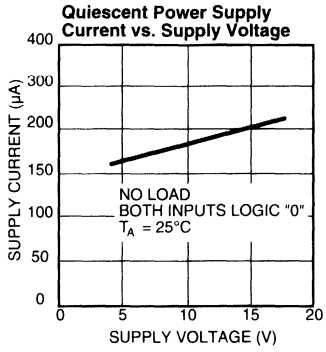
High Output vs. Current

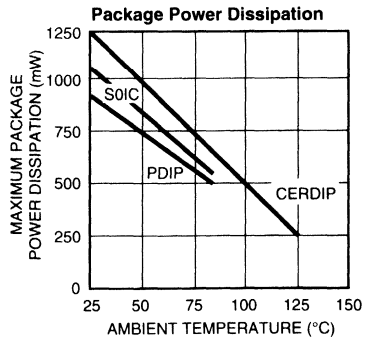


Low Output vs. Current

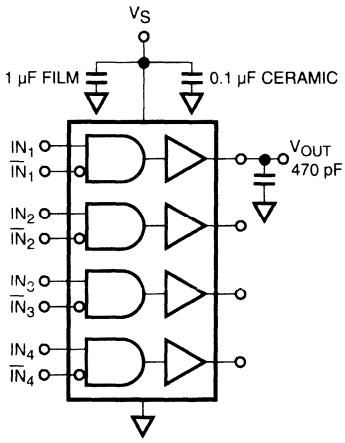


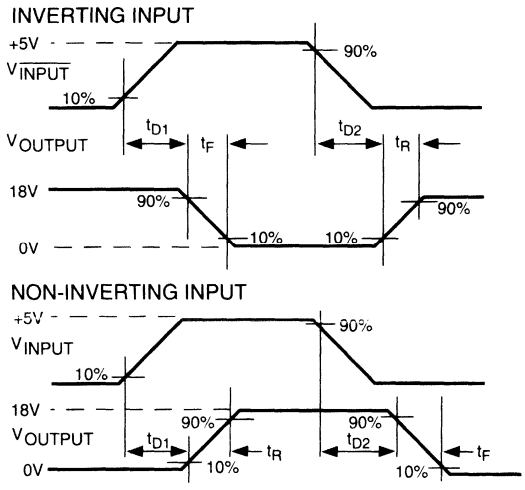




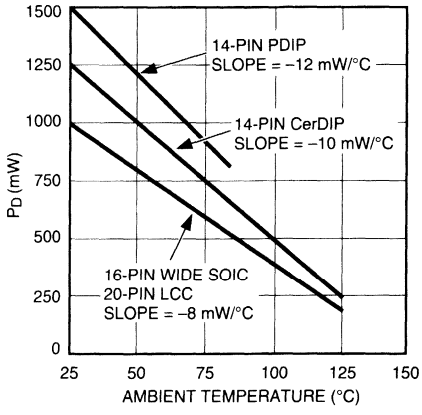


Test Figure 1

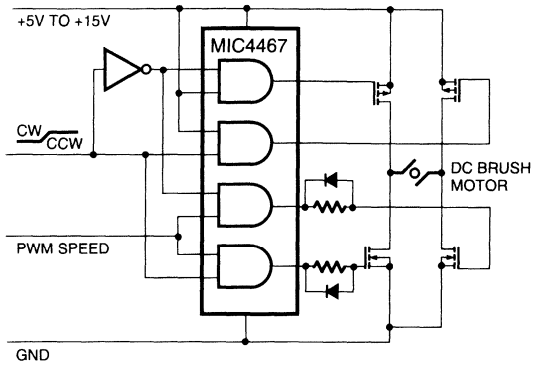




Package Power Dissipation



Quad Driver Drives H Bridge to Control Motor Speed and Direction



MIC5010

Full-Featured Power MOSFET Predriver

General Description

The MIC5010 is the full-featured member of the Micrel MIC501X predriver family. These ICs are designed to drive the gate of an N-channel power MOSFET above the supply rail in high-side power switch applications. The MIC5010 is compatible with standard or current-sensing power FETs in both high- and low-side driver topologies.

The MIC5010 charges a 1nF load in 60µs typical and protects the MOSFET from over-current conditions. Faster switching is achieved by adding two 1nF charge pump capacitors. The current sense trip point is fully programmable and a dynamic threshold allows high in-rush current loads to be started. A fault pin indicates when the MIC5010 has turned off the FET due to excessive current.

Other members of the Micrel predriver family include the MIC5011 minimum parts count 8 pin predriver, MIC5012 dual predriver, and MIC5013 protected 8 pin predriver.

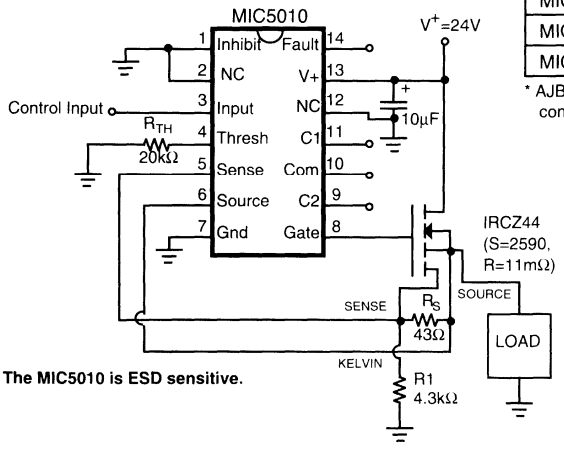
Features

- 7V to 32V operation
- Less than 1µA standby current in the "OFF" state
- Internal charge pump to drive the gate of an N-channel power FET above supply
- MIL-STD-883 Method 5004/5005 version available
- Available in small outline SOIC packages
- Internal zener clamp for gate protection
- 25µs typical turn-on time to 50% gate overdrive
- Programmable over-current sensing
- Dynamic current threshold for high in-rush loads
- Fault output pin indicates current faults
- Implements high- or low-side switches

Applications

- Lamp drivers
- Relay and solenoid drivers
- Heater switching
- Power bus switching
- Motion control
- Half or full H-bridge drivers

Typical Application



Note: The MIC5010 is ESD sensitive.

Ordering Information

Part Number	Temperature Range	Package
MIC5010BN	–40°C to +85°C	14-pin Plastic DIP
MIC5010BJ	–40°C to +85°C	14-pin Ceramic DIP
MIC5010BM	–40°C to +85°C	14-pin SOIC
MIC5010AJ	–55°C to +125°C	14-pin Ceramic DIP
MIC5010AJB*	–55°C to +125°C	14-pin Ceramic DIP
MIC5010B	–40°C to +85°C	Die

* AJB indicates units screened to MIL-STD 883, Method 5004, condition B, and burned-in for 1-week.

$$R_S = \frac{SR(V_{TRIP} + 100mV)}{R\,I_L - (V_{TRIP} + 100mV)}$$

$$R1 = \frac{V^+ SRR_S}{100mV\,(SR + R_S)}$$

$$R_{TH} = \frac{2200}{V_{TRIP}} - 1000$$

For this example:

I_L =30A (trip current)

V_{TRIP} =100mV

Figure 1. High-Side Driver with Current-Sensing MOSFET

Absolute Maximum Ratings (Note 1, 2)

Inhibit Voltage, Pin 1	–1V to V+
Input Voltage, Pin 3	–10V to V+
Threshold Voltage, Pin 4	– 0.5 to +5V
Sense Voltage, Pin 5	–10V to V+
Source Voltage, Pin 6	–10V to V+
Current into Pin 6	50 mA
Gate Voltage, Pin 8	–1V to 50V
Supply Voltage (V^+), Pin 13	–0.5V to 36V
Fault Output Current, Pin 14	–1mA to +1mA
Junction Temperature	150°C

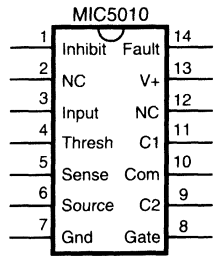
Operating Ratings (Notes 1, 2)

Power Dissipation	1.56W
θ_{JA} (Plastic DIP)	80 °C/W
θ_{JA} (Ceramic DIP)	105°C/W
θ_{JA} (SOIC)	115°C/W
Ambient Temperature: B version	–40°C to +85°C
Ambient Temperature: A version	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C
Supply Voltage (V^+), Pin 13	7V to 32V high side 7V to 15V low side

Pin Description (Refer to Figures 1 and 2)

Pin Number	Pin Name	Pin Function
1	Inhibit	Inhibits current sense function when connected to supply. Normally grounded.
3	Input	Resets current sense latch and turns on power MOSFET when taken above threshold (3.5V typical). Pin 3 requires <1µA to switch.
4	Threshold	Sets current sense trip voltage according to: $V_{TRIP} = \frac{2200}{R_{TH} + 1000}$ where R_{TH} to ground is 3.3k to 20kΩ. Adding capacitor C_{TH} increases the trip voltage at turn-on to 2V. Use C_{TH} =10µF for a 10mS turn-on time constant.
5	Sense	The sense pin causes the current sense to trip when V_{SENSE} is V_{TRIP} above V_{SOURCE}. Pin 5 is used in conjunction with a current shunt in the source of a 3 lead FET or a resistor R_S in the sense lead of a current sensing FET.
6	Source	Reference for the current sense voltage on pin 5 and return for the gate clamp zener. Connect to the load side of current shunt or Kelvin lead of current sensing FET. Pins 5 and 6 can safely swing to –10V when turning off inductive loads.
7	Ground	
8	Gate	Drives and clamps the gate of the power FET. Pin 8 will be clamped to approximately –0.7V by an internal diode when turning off inductive loads.
9, 10, 11	C2, Com, C1	Optional 1nF capacitors reduce gate turn-on time; C2 has dominant effect.
13	V^+	Supply pin; must be decoupled to isolate from large transients caused by the power FET drain. 10µF is recommended close to pins 13 and 7.
14	Fault	Outputs status of protection circuit when pin 3 is high. Fault low indicates normal operation; fault high indicates current sense tripped.

Pin Configuration



Electrical Characteristics (Note 3) Test circuit. T_A = –55°C to +125°C, V^+ = 15V, V_1 = 0 V, $I_4 = I_5 = I_{14} = 0$, all switches open, unless otherwise specified.

Parameter	Conditions			Min	Typical	Max	Units
Supply Current, I_{13}	V^+ = 32V	V_{IN} = 0V, S4 closed			0.1	10	µA
		$V_{IN} = V_S$ = 32V, I_4 = 200µA			8	20	mA
Logic Input Voltage, V_{IN}	V^+ = 4.75V	Adjust V_{IN} for V_{GATE} low				2	V
		Adjust V_{IN} for V_{GATE} high		4.5			V
	V^+ = 15V	Adjust V_{IN} for V_{GATE} high		5.0			V
Logic Input Current, I_3	V+ = 32V	V_{IN} = 0V		–1			µA
		V_{IN} = 32V				1	µA
Input Capacitance	Pin 3				5		pF
Gate Drive, V_{GATE}	S1, S2 closed,	V^+ = 7V, I_8 = 0		13	15		V
	V_S = V+, V_{IN} = 5V	V^+ = 15V, I_8 = 100 µA		24	27		V
Zener Clamp,	S2 closed, V_{IN} = 5V	V+ = 15V, V_S = 15V		11	12.5	15	V
$V_{GATE} - V_{SOURCE}$		V^+ = 32V, V_S = 32V		11	13	16	V
Gate Turn-on Time, t_{ON} (Note 4)	V_{IN} switched from 0 to 5V; measure time for V_{GATE} to reach 20V				25	50	µs
Gate Turn-off Time, t_{OFF}	V_{IN} switched from 5 to 0V; measure time for V_{GATE} to reach 1V				4	10	µs
Threshold Bias Voltage, V_4	I_4 = 200 µA			1.7	2	2.2	V
Current Sense Trip Voltage,	S2 closed, V_{IN} = 5V,	V^+ = 7V,	S4 closed	75	105	135	mV
$V_{SENSE} - V_{SOURCE}$	Increase I_5	I_4 = 100 µA	V_S = 4.9V	70	100	130	mV
		V^+ = 15V	S4 closed	150	210	270	mV
		I_4 = 200 µA	V_S = 11.8V	140	200	260	mV
		V^+ = 32V	V_S = 0V	360	520	680	mV
		I_4 = 500 µA	V_S = 25.5V	350	500	650	mV
Peak Current Trip Voltage, $V_{SENSE} - V_{SOURCE}$	S3, S4 closed, V^+ = 15V, V_{IN} = 5V				1.6	2.1	V
Fault Output Voltage, V_{14}	V_{IN} = 0V, I_{14} = –100 µA				0.4	1	V
	V_{IN} = 5V, I_{14} = 100 µA, current sense tripped			14	14.6		V
Current Sense Inhibit, V_1	V_1 above which current sense is disabled				7.5	13	V
	Minimum possible V_1				1		V

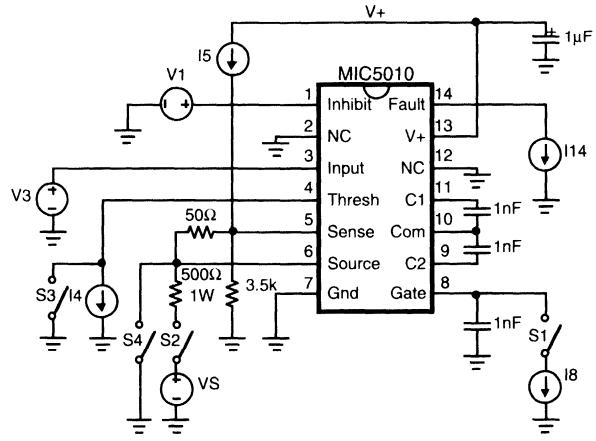
Note 1 **Absolute Maximum Ratings** indicate limits beyond which damage to the device may occur. Electrical specifications do not apply when operating the device beyond its specified **Operating Ratings**.

Note 2 The MIC5010 is ESD sensitive.

Note 3 Minimum and maximum **Electrical Characteristics** are 100% tested at T_A = 25°C and T_A = 85°C, and 100% guaranteed over the entire range. Typicals are characterized at 25°C and represent the most likely parametric norm.

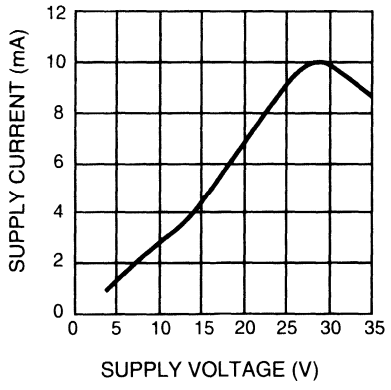
Note 4 Test conditions reflect worst case high-side driver performance. Low-side and bootstrapped topologies are significantly faster—see **Applications Information**.

Test Circuit

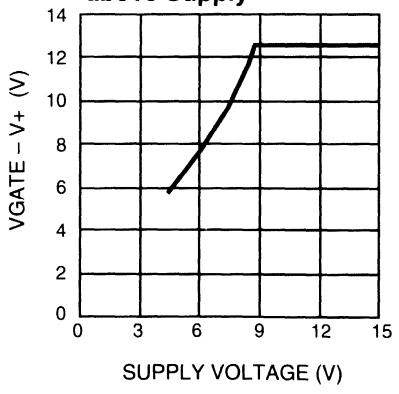


Typical Characteristics

Supply Current

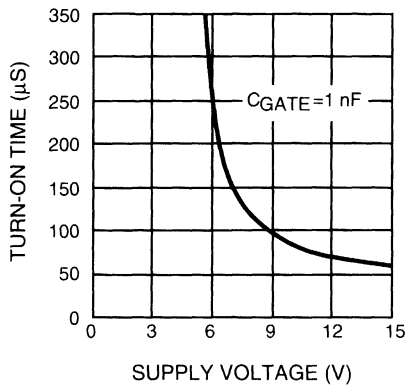


DC Gate Voltage above Supply

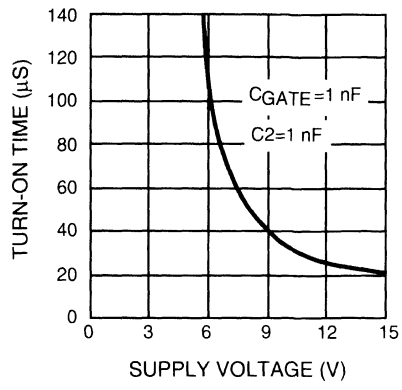


Typical Characteristics (Continued)

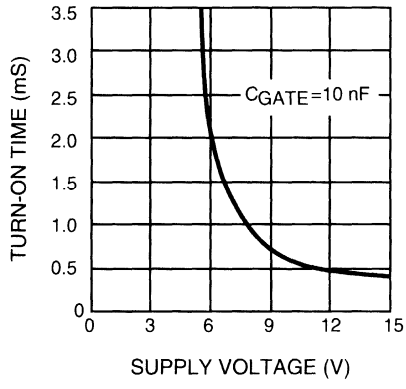
High-side Turn-on Time*



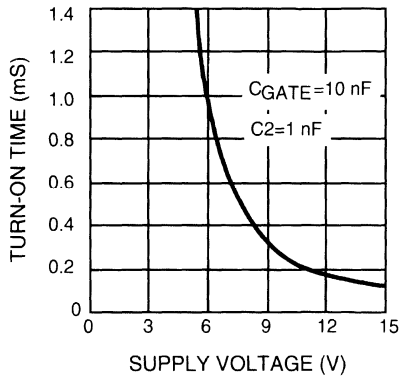
High-side Turn-on Time*



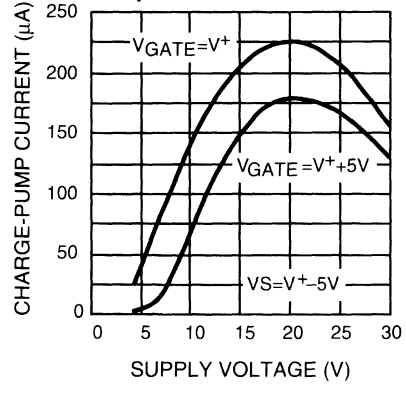
High-side Turn-on Time*



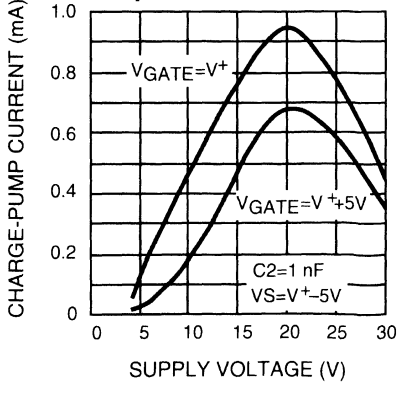
High-side Turn-on Time*



Charge Pump Output Current



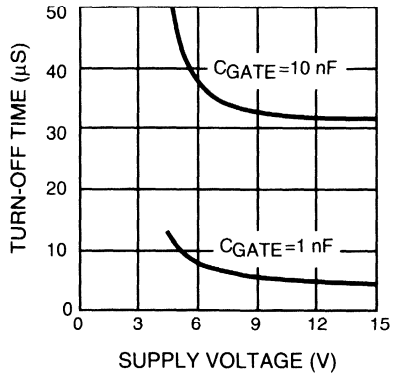
Charge Pump Output Current



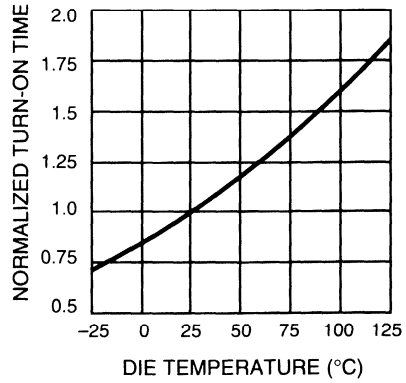
* Time for gate to reach $V^+ + 5V$ in test circuit with $VS = V^+ - 5V$ (prevents gate clamp from interfering with measurement).

Typical Characteristics (Continued)

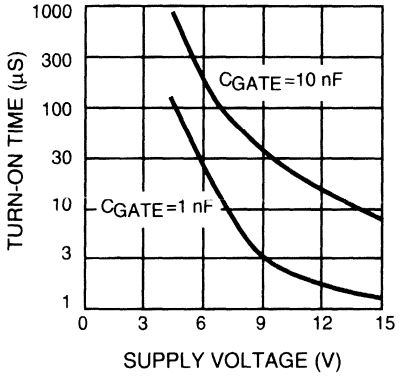
Turn-off Time



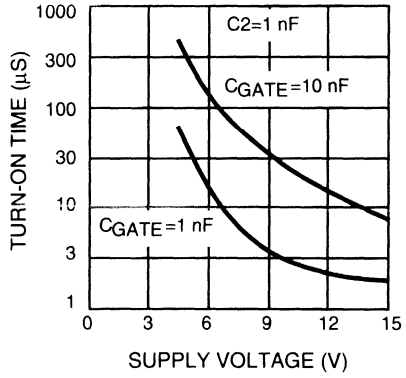
Turn-on Time



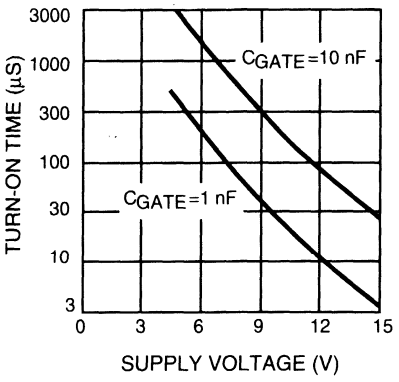
Low-side Turn-on Time for Gate = 5V



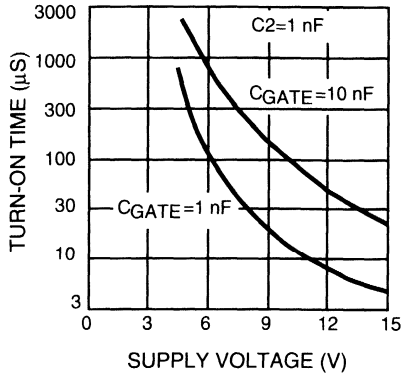
Low-side Turn-on Time for Gate = 5V



Low-side Turn-on Time for Gate = 10V



Low-side Turn-on Time for Gate = 10V



Applications Information

Functional Description (Refer to **Block Diagram**)

The various MIC5010 functions are controlled via a logic block connected to the input pin 3. When the input is low all functions are turned off for low standby current, and the gate of the power MOSFET is also held low through 500Ω to an N-channel switch. When the input is taken above the turn-on threshold (3.5V typical), the N-channel switch turns off and the charge pump is turned on to charge the gate of the power FET. A bandgap type voltage regulator is also turned on which biases the current sense circuitry.

The charge pump incorporates a 100kHz oscillator and on-chip pump capacitors capable of charging 1 nF to 5V above supply in 60μS typical. With the addition of 1nF capacitors at C1 and C2, the turn-on time is reduced to 25μS typical. The charge pump is capable of pumping thegate up to over twice the supply voltage. For this reason a zener clamp (12.5V typical) is provided between the gate pin 8 and the source pin 6 to prevent exceeding the V_{GS} rating of the MOSFET at high supplies.

The current sense operates by comparing the sense voltage at pin 5 to an offset version of the source voltage at pin 6. Current I4 flowing in threshold pin 4 is mirrored and returned to the source via a 1kΩ resistor to set the offset or trip voltage. When ($V_{SENSE} - V_{SOURCE}$) exceeds V_{TRIP}, the current sense trips and sets the current sense latch to turn off the power FET. An integrating comparator is used to reduce sensitivity to spikes on pin 5. The latch is reset to turn the FET back on by "recycling" the input pin 3 low and then high again.

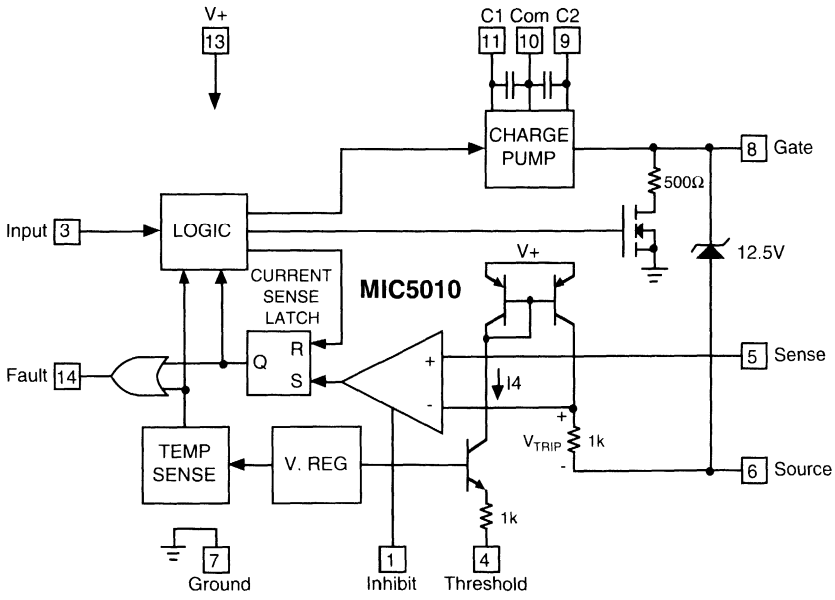
A resistor R_{TH} from pin 4 to ground sets I4, and hence V_{TRIP}. An additional capacitor C_{TH} from pin 4 to ground creates a higher trip voltage at turn-on, which is necessary to prevent high in-rush current loads such as lamps or capacitors from false-tripping the current sense.

When the current sense has tripped, the fault pin 14 will be high as long as the input pin 3 remains high. However, when the input is low the fault pin will also be low.

Construction Hints

High current pulse circuits demand equipment and assembly techniques that are more stringent than normal, low current lab practices. The following are the sources of common pitfalls encountered while prototyping:Supplies: many bench power supplies have poor transient response. Circuits that are being pulse tested, or those that operate by pulse-width modulation will produce strange results when used with a supply that has poor ripple rejection, or a peaked transient response. Monitor the power supply voltage that appears at the drain of a high-side driver (or the supply side of the load in a low-side driver) with an oscilloscope. It is not uncommon to find bench power supplies in the 1kW class that overshoot or undershoot by as much as 50% when pulse loaded. Not only will the load current and voltage measurements be affected, but it is possible to over-stress various components—especially electrolytic capacitors—with possibly catastrophic results. A 10μF supply bypass capacitor at the chip is recommended.

Block Diagram



Applications Information (Continued)

Residual Resistances: Resistances in circuit connections may also cause confusing results. For example, a circuit may employ a 50mΩ power MOSFET for low drop, but careless construction techniques could easily add 50 to 100 mΩ resistance. Do not use a socket for the MOSFET. If the MOSFET is a TO-220 type package, make high-current drain connections to the tab. Wiring losses have a profound effect on high-current circuits. A floating millivoltmeter can identify connections that are contributing excess drop under load.

Circuit Topologies

The MIC5010 is suited for use in high- or low-side driver applications with over-current protection for both current-sensing and standard MOSFETs. In addition, the MIC5010 works well in applications where, for faster switching times, the supply is bootstrapped from the MOSFET source output. Low voltage, high-side drivers (such as shown in the Test Circuit) are the slowest; their speed is reflected in the gate turn-on time specifications. The fastest drivers are the low-side and bootstrapped high-side types. Load current switching times are often much faster than the time to full gate enhancement, depending on the circuit type, the MOSFET, and the load. Turn-off times are essentially the same for all circuits (less than 10µs to V_{GS} = 1V). The choice of one topology over another is based on a combination of considerations including speed, voltage, and desired system characteristics. Each topology is described in this section. Note that I_L, as used in the design equations, is the load current that just trips the over-current comparator.

Low-Side Driver with Current Shunt (Figure 2). The over-current comparator monitors R_S and trips if $I_L \times R_S$ exceeds V_{TRIP}. R_{TH} is selected to produce the desired trip voltage. As a guideline, keep V_{TRIP} within the limits of 100mV and 500mV (R_{TH} = 3.3kΩ to 20kΩ). Thresholds at the high end offer the best noise immunity, but also compromise switch drop (especially in low voltage applications) and power dissipation.

The trip current is set higher than the maximum expected load current--typically twice that value. Trip point accuracy is a function of resistor tolerances, comparator offset (only a few millivolts), and threshold bias voltage (V_4). The values shown in Figure 2 are designed for a trip current of 20 amperes. It is important to ground pin 6 at the current shunt R_S, to eliminate the effects of ground resistance.

A key advantage of the low-side topology is that the load supply is limited only by the MOSFET BV_{DSS} rating. Clamping may be required to protect the MOSFET drain terminal from inductive switching transients. The MIC5010 supply should be limited to 15V in low-side topologies; otherwise, a large current will be forced through the gate clamp zener.

Low-side drivers constructed with the MIC501X family are also fast; the MOSFET gate is driven to near supply immediately when commanded ON. Typical circuits achieve 10V enhancement in 10µs or less on a 12 to 15V supply.

High-Side Driver with Current Shunt (Figure 3). The comparator input pins (source and sense) float with the current sensing resistor (R_S) on top of the load. R1 and R2 add a small, additional potential to V_{TRIP} to prevent false-triggering of the over-current shutdown circuit with open or inductive loads. R1 is sized for a current flow of 1mA, while R2 contributes a drop of 100mV. The shunt voltage should be 200 to 500mV at the trip point. The example of Figure 3 gives a 10A trip current when the output is near supply. The trip point is somewhat reduced when the output is at ground as the voltage drop across R1 (and therefore R2) is zero.

High-side drivers implemented with MIC501X predrivers

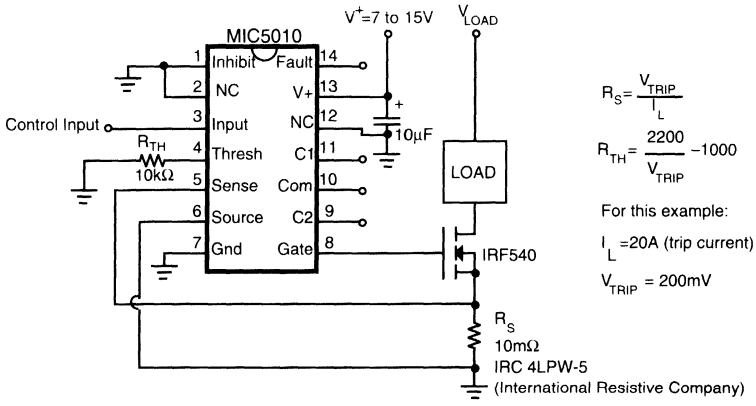


Figure 2. Low-Side Driver with Current Shunt

Applications Information (Continued)

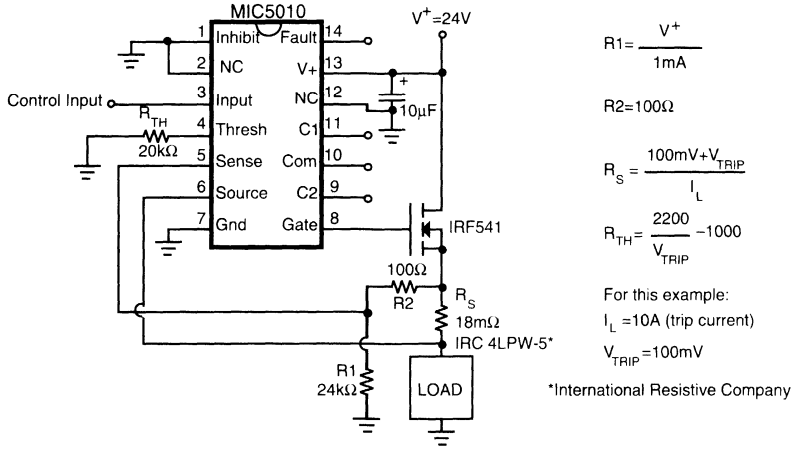


Figure 3. High-Side Driver with Current Shunt

are self-protected against inductive switching transients. During turn-off an inductive load will force the MOSFET source 5V or more below ground, while the predriver holds the gate at ground potential. The MOSFET is forced into conduction, and it dissipates the energy stored in the load inductance. The MIC5010 source and sense pins (5 and 6) are designed to withstand this negative excursion without damage. External clamp diodes are unnecessary, but may be added to reduce power dissipation in the MOSFET.

Current Shunts (R_S). Low-valued resistors are necessary for use at R_S.Values for R_S range from 5 to 50mΩ, at 2 to 10W. Worthy of special mention are Kelvin-sensed, "four-terminal" units supplied by a number of manufacturers†. Kelvin-sensed resistors eliminate errors that are caused by lead and terminal resistances, and simplify product assembly. 10% tolerance is normally adequate, and with shunt potentials of 200mV thermocouple effects are insignificant. Temperature coefficient is important; a linear, 500ppm/°C change will contribute as much as 10% shift in the over-current trip point. Most power resistors designed for current shunt service drift less than 100ppm/°C.

Low-Side Driver with Current Sensing MOSFET (Figure 4). Several manufacturers now supply power MOSFETs in which a small sampling of the total load current is diverted to a "sense" pin. One additional pin, called "Kelvin source," is included to eliminate the effects of resistance in the source bond wires. Current-sensing MOSFETs are specified with a sensing ratio "S" which describes the relationship between the on-resistance of the sense connection and the body resistance "R" of the main source pin. Current sensing MOSFETs eliminate the current shunt required by standard MOSFETs.

The design equations for a low-side driver using a current sensing MOSFET are shown in Figure 4. "S" is specified on the MOSFET's datasheet, and "R" must be measured or estimated. V_{TRIP} must be less than $R \times I_L$, or else R_S will become negative. Substituting a MOSFET with higher on-resistance, or reducing V_{TRIP} fixes this problem. V_{TRIP} = 100 to 200mV is suggested. Although the load supply is limited only by MOSFET ratings, the MIC5010 supply should be limited to 15V to prevent damage to the gate clamp zener. Output clamping is necessary for inductive loads.

"R" is the body resistance of the MOSFET, excluding bond resistances. $R_{DS(ON)}$ as specified on MOSFET data sheets includes bond resistances. A Kelvin-connected ohmmeter (using TAB and SOURCE for forcing, and SENSE and KELVIN for sensing) is the best method of evaluating "R." Alternatively, "R" can be estimated for large MOSFETs ($R_{DS(ON)} \leq 100m\Omega$) by simply halving the stated $R_{DS(ON)}$, or by subtracting 20 to 50mΩ from the stated $R_{DS(ON)}$ for smaller MOSFETs.

High-Side Driver with Current Sensing MOSFET (Figure 1). The design starts by determining the value of "S" and "R" for the MOSFET (use the guidelines described for the low-side version). Let V_{TRIP} = 100 mV, and calculate R_S for a desired trip current. Next calculate R_{TH} and R1. The trip

† Suppliers of Kelvin-sensed power resistors:
Dale Electronics, Inc., 2064 12th Ave., Columbus, NE 68601. Tel: (402) 564-3131
International Resistive Co., P.O. Box 1860, Boone, NC 28607-1860. Tel: (704) 264-8861
Kelvin, 14724 Ventura Blvd., Ste. 1003, Sherman Oaks, CA 91403-3501. Tel: (818) 990-1192
RCD Components, Inc., 520 E. Industrial Pk. Dr., Manchester, NH 03103. Tel: (603) 669-0054
Ultronix, Inc., P.O. Box 1090, Grand Junction, CO 81502. Tel: (303) 242-0810

Applications Information (Continued)

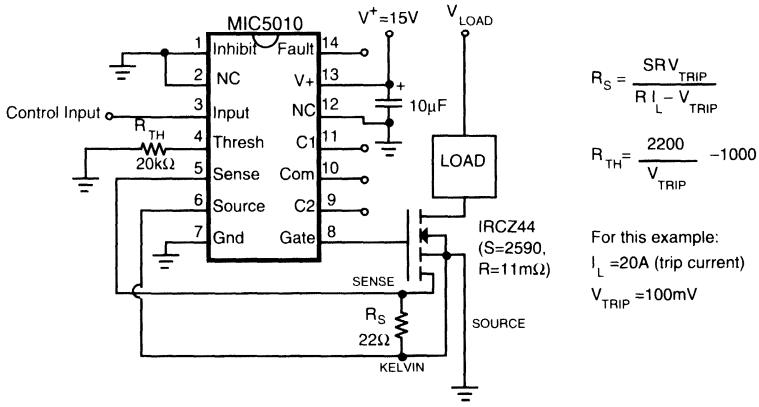


Figure 4. Low-Side Driver with Current-Sensing MOSFET

point is somewhat reduced when the output is at ground as the voltage drop across R1 is zero. No clamping is required for inductive loads.

Typical Applications

Start-up into a Dead Short. If the MIC5010 attempts to turn on a MOSFET when the load is shorted, a very high current flows. The over-current shutdown will protect the MOSFET, but only after a time delay of 5 to 10µs. The MOSFET must be capable of handling the overload; consult the device's SOA curve. If a short circuit causes the MOSFET to exceed its 10µs SOA, a small inductance in series with the source can help limit di/dt to control the peak current during the 5 to 10µs delay.

When testing short-circuit behavior, use a current probe rated for both the peak current and the high di/dt.

The over-current shutdown delay varies with comparator overdrive, owing to noise filtering in the comparator. A delay of up to 100µs can be observed at the threshold of shutdown. A 20% overdrive reduces the delay to near minimum.

Incandescent Lamps. The cold filament of an incandescent lamp exhibits less than one-tenth as much resistance as when the filament is hot. The initial turn-on current of a #6014 lamp is about 70A, tapering to 4.4A after a few hundred milliseconds. It is unwise to set the over-current trip point to 70A to accommodate such a load. A "resistive" short that draws less than 70A could destroy the MOSFET by allowing sustained, excessive dissipation. If the over-current trip point is set to less than 70A, the MIC5010 will not start a cold filament. The solution is to start the lamp with a high trip point, but reduce this to a reasonable value after the lamp is hot.

The MIC5010 over-current shutdown circuit is designed to handle this situation by varying the trip point with time (see Figure 5). R_{TH1} functions in the conventional manner, providing a current limit of approximately twice that required by the lamp. R_{TH2} acts to increase the current limit at turn-on to approximately 10 times the steady-state lamp current. The high initial trip point decays away according to a 20ms time constant contributed by C_{TH}. R_{TH2} could be eliminated with C_{TH} working against the internal 1kΩ resistor, but this results in a very high over-current threshold. As a rule of thumb design the over-current circuitry in the conventional manner, then add the R_{TH2}/C_{TH} network to allow for lamp start-up. Let $R_{TH2} = (R_{TH1} \div 10) - 1k\Omega$, and choose a capacitor that provides the desired time constant working against R_{TH2} and the internal 1kΩ resistor.

When the MIC5010 is turned off, the threshold pin (4) appears as an open circuit, and C_{TH} is discharged through R_{TH1} and R_{TH2}. This is much slower than the turn-on time

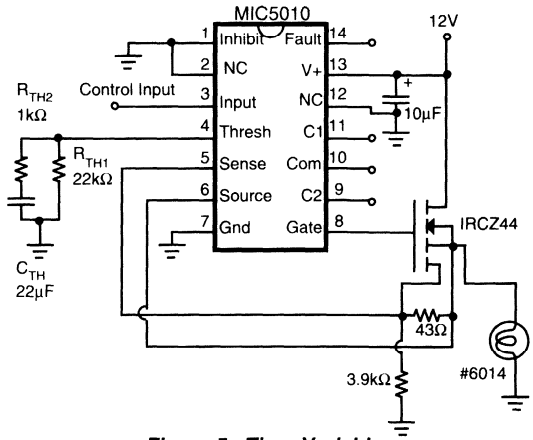


Figure 5. Time-Variable Trip Threshold

Applications Information (Continued)

constant, and it simulates the thermal response of the filament. If the lamp is pulse-width modulated, the current limit will be reduced by the residual charge left in C_{TH}.

Modifying Switching Times. Do not add external capacitors to the gate to slow down the switching time. Add a resistor (1kΩ to 51kΩ) in series with the gate of the MOSFET to achieve this result.

External capacitors can be added at C1 and C2 for faster switching times (see Block Diagram). Values of 100pF to 1nF produce useful speed increases. If component count is critical, C2 (pins 9 to 10) can be used alone with only a small loss of speed compared to using both capacitors.

Bootstrapped High-Side Driver (Figure 6). The speed of a high-side driver can be increased to better than 10µs by bootstrapping the supply off of the MOSFET source. This topology can be used where the load is pulse-width modulated (100Hz to 20kHz), or where it is energized for only a short period of time (≤25ms). If the load is left energized for a long period of time (>25ms), the bootstrap capacitor will discharge and the MIC5010 supply pin will fall to $V^+ = V_{DD} - 1.4$. Under this condition pins 5 and 6 will be held above V^+ and may false trigger the over-current circuit. A larger capacitor will lengthen the maximum "on" time; 1000µF will hold the circuit up for 2.5 seconds, but requires more charge time when the circuit is turned off. The optional Schottky barrier diode improves turn-on time on supplies of less than 10V.

Since the supply current in the "off" state is only a small leakage, the 100nF bypass capacitor tends to remain charged for several seconds after the MIC5010 is turned off. In a PWM application the chip supply is actually much higher than the system supply, which improves switching time.

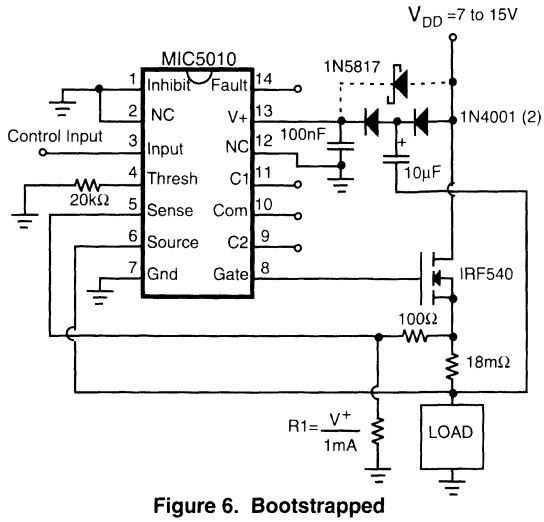


Figure 6. Bootstrapped High-Side Driver

Electronic Circuit Breaker (Figure 7). The MIC5010 forms the basis of a high-performance, fast-acting circuit breaker. By adding feedback from FAULT to INPUT the breaker can be made to automatically reset. If an over-current condition

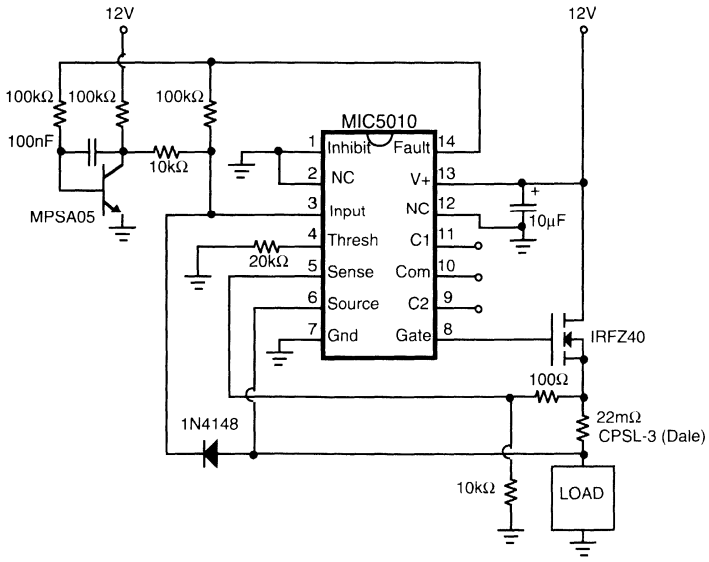


Figure 7. 10-Ampere Electronic Circuit Breaker

Applications Information (Continued)

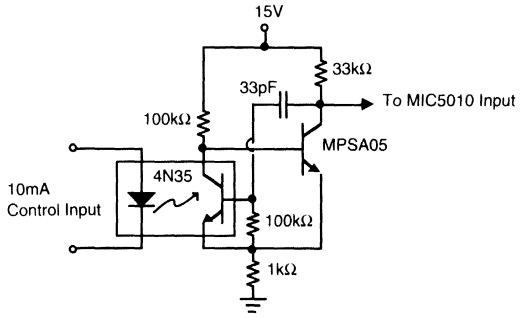


Figure 8. Improved Opto-Isolator Performance

occurs, the circuit breaker shuts off. The breaker tests the load every 18ms until the short is removed, at which time the circuit latches ON. No reset button is necessary.

Opto-Isolated Interface (Figure 8). Although the MIC5010 has no special input slew rate requirement, the lethargic transitions provided by an opto-isolator may cause oscillations on the rise and fall of the output. The circuit shown accelerates the input transitions from a 4N35 opto-isolator by adding hysteresis. Opto-isolators are used where the control circuitry cannot share a common ground with the MIC5010 and high-current power supply, or where the control circuitry is located remotely. This implementation is intrinsically safe; if the control line is severed the MIC5010 will turn OFF.

Fault-Protected Industrial Switch (Figure 9). The most common manual control for industrial loads is a push button on/off switch. The "on" button is physically arranged in a recess so that in a panic situation the "off" button, which extends out from the control box, is more easily pressed. This circuit is compatible with control boxes such as the CR2943 series (GE). The circuit is configured so that if both switches close simultaneously, the "off" button has precedence. If there is a fault condition the circuit will latch off, and it can be reset by pushing the "on" button.

This application also illustrates how two (or more) MOSFETs can be paralleled. This reduces the switch drop, and distributes the switch dissipation into multiple packages.

High-Voltage Bootstrap (Figure 10). Although the MIC5010 is limited to operation on 7 to 32V supplies, a floating bootstrap arrangement can be used to build a high-side switch that operates on much higher voltages. The MIC5010 and MOSFET are configured as a low-side driver, but the load is connected in series with ground. The high speed normally associated with low-side drivers is retained in this circuit.

Power for the MIC5010 is supplied by a charge pump. A 20kHz square wave (15Vp-p) drives the pump capacitor and delivers current to a 100µF storage capacitor. A zener diode limits the supply to 18V. When the MIC5010 is off, power is supplied by a diode connected to a 15V supply. The circuit of Figure 8 is put to good use as a barrier between low voltage control circuitry and the 90V motor supply.

Half-Bridge Motor Driver (Figure 11). Closed loop control of motor speed requires a half-bridge driver. This topology presents an extra challenge since the two output devices should not cross conduct (shoot-through) when switching. Cross conduction increases output device power dissipation and, in the case of the MIC5010, could trip the overcurrent comparator. Speed is also important, since PWM control requires the outputs to switch in the 2 to 20kHz range.

The circuit of Figure 11 utilizes fast configurations for both the top- and bottom-side drivers. Delay networks at each input provide a 2 to 3µs dead time effectively eliminating

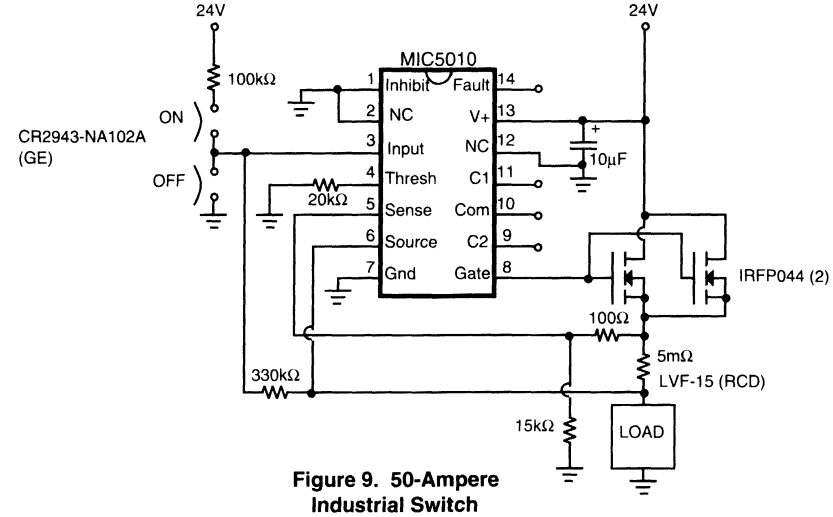


Figure 9. 50-Ampere Industrial Switch

Applications Information (Continued)

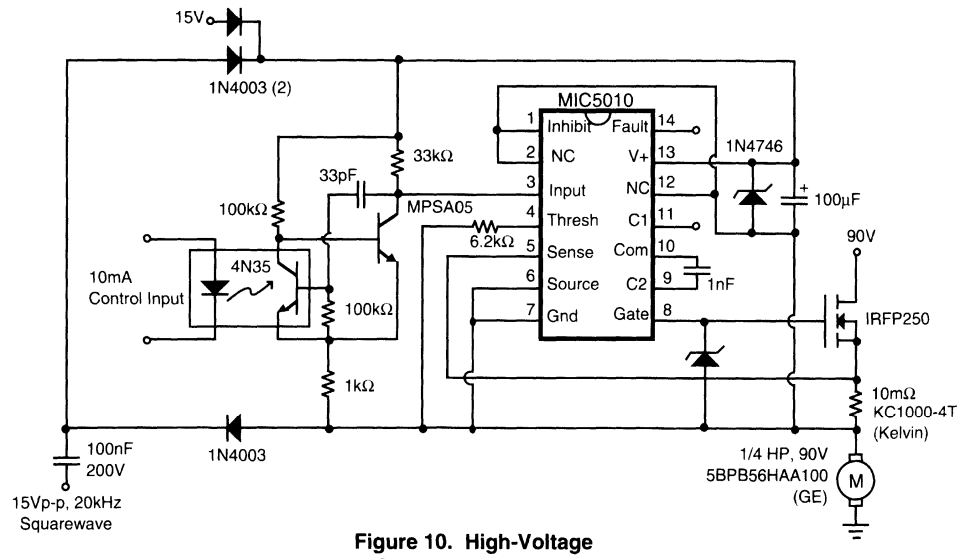


Figure 10. High-Voltage Bootstrapped Driver

cross conduction. Both the top- and bottom-side drivers are protected, so the output can be shorted to either rail without damage.

The top-side driver is based on the bootstrapped circuit of Figure 6, and cannot be switched on indefinitely. The bootstrap capacitor (1µF) relies on being pulled to ground by the bottom-side output to recharge. This limits the maximum duty cycle to slightly less than 100%.

Two of these circuits can be connected together to form an H-bridge. If the H-bridge is used for locked antiphase control, no special considerations are necessary. In the case of sign/magnitude control, the "sign" leg of the H-bridge should be held low (PWM input held low) while the other leg is driven by the magnitude signal.

If current feedback is required for torque control, it is available in chopped form at the bottom-side driver's 22mΩ current-sensing resistor.

Time-Delay Relay (Figure 12). The MIC5010 forms the basis of a simple time-delay relay. As shown, the delay commences when power is applied, but the 100kΩ/1N4148 could be independently driven from an external source such as a switch or another high-side driver to give a delay relative to some other event in the system.

Hysteresis has been added to guarantee clean switching at turn-on. Note that an over-current condition latches the relay in a safe, OFF condition. Operation is restored by either cycling power or by momentarily shorting pin 3 to ground.

Motor Driver with Stall Shutdown (Figure 13). Tachometer feedback can be used to shut down a motor driver circuit when a stall condition occurs. The control switch is a 3-way type; the "START" position is momentary and forces the driver ON. When released, the switch returns to the "RUN" position, and the tachometer's output is used to hold the MIC5010 input ON. If the motor slows down, the tach output is reduced, and the MIC5010 switches OFF. Resistor "R" sets the shutdown threshold. If the output current exceeds 30A, the MIC5010 shuts down and remains in that condition until the momentary "RESET" button is pushed. Control is then returned to the START/RUN/STOP switch.

Applications Information (Continued)

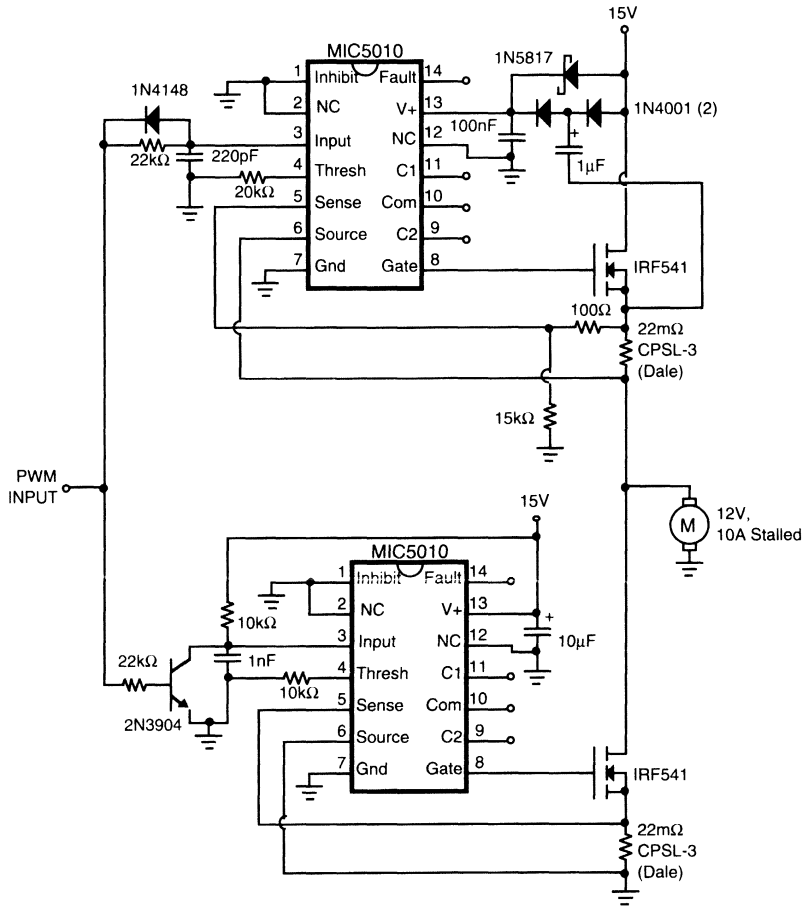


Figure 11. Half-Bridge Motor Driver

Applications Information (Continued)

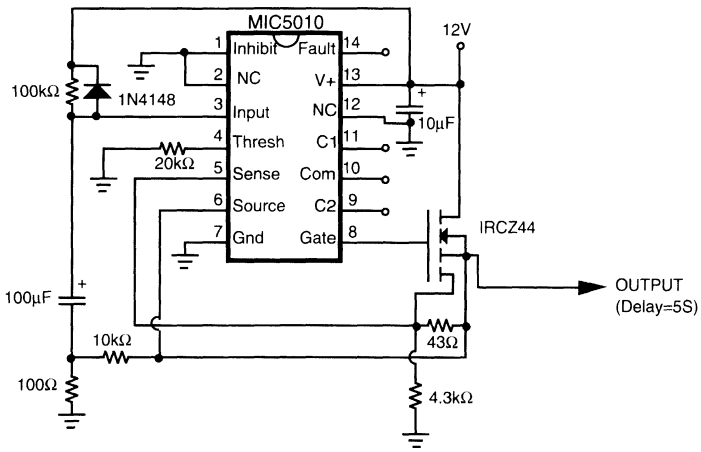


Figure 12. Time-Delay Relay with 30A Over-Current Protection

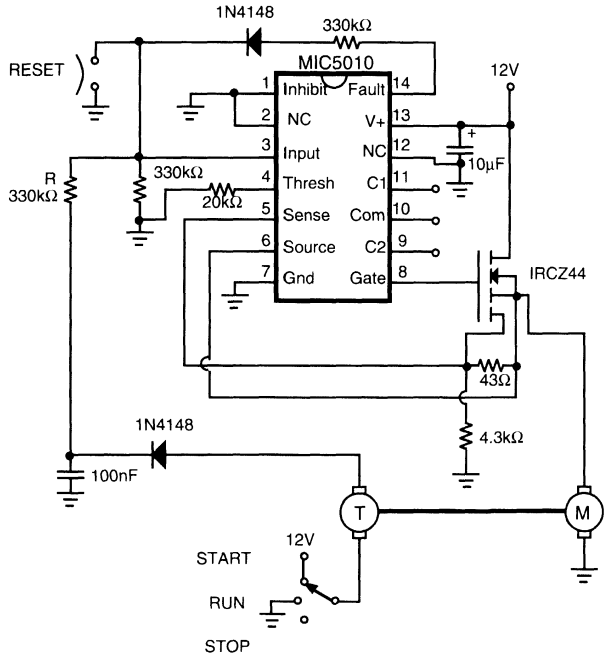


Figure 13. Motor Stall Shutdown

Applications Information (Continued)

Gate Control Circuit

When applying the MIC5010, it is helpful to understand the operation of the gate control circuitry (see Figure 14). The gate circuitry can be divided into two sections: 1) charge pump (oscillator, Q1-Q5, and the capacitors) and 2) gate turn-off switch (Q6).

When the MIC5010 is in the OFF state, the oscillator is turned off, thereby disabling the charge pump. Q5 is also turned off, and Q6 is turned on. Q6 holds the gate pin (G) at ground potential which effectively turns the external MOSFET off.

Q6 is turned off when the MIC5010 is commanded on. Q5 pulls the gate up to supply (through 2 diodes). Next, the charge pump begins supplying current to the gate. The gate accepts charge until the gate-source voltage reaches 12.5V and is clamped by the zener diode.

A 2-output, three-phase clock switches Q1-Q4, providing a quasi-tripling action. During the initial phase Q4 and Q2 are ON. C1 is discharged, and C2 is charged to supply through Q5. For the second phase Q4 turns off and Q3 turns on, pushing pin C2 above supply (charge is dumped into the gate). Q3 also charges C1. On the third phase Q2 turns off and Q1 turns on, pushing the common point of the two capacitors above supply. Some of the charge in C1 makes its way to the gate. The sequence is repeated by turning Q2 and Q4 back on, and Q1 and Q3 off.

In a low-side application operating on a 12 to 15V supply, the MOSFET is fully enhanced by the action of Q5 alone. On supplies of more than approximately 14V, current flows directly from Q5 through the zener diode to ground. To prevent excessive current flow, the MIC5010 supply should be limited to 15V in low-side applications.

The action of Q5 makes the MIC5010 operate quickly in low-side applications. In high-side applications Q5 precharges the MOSFET gate to supply, leaving the charge pump to carry the gate up to full enhancement 10V above supply. Bootstrapped high-side drivers are as fast as low-side drivers since the chip supply is boosted well above the drain at turn-on.

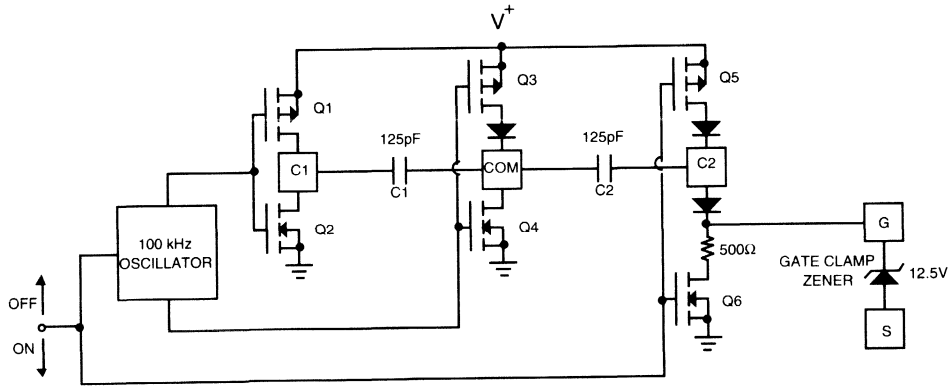


Figure 14. Gate Control Circuit Detail

MIC5011

Minimum Parts Count MOSFET Predriver

General Description

The MIC5011 is the "minimum parts count" member of the Micrel MIC501X predriver family. These ICs are designed to drive the gate of an N-channel power MOSFET above the supply rail in high-side power switch applications. The 8-pin MIC5011 is extremely easy to use, requiring only a power FET and nominal supply decoupling to implement either a high- or low-side switch.

The MIC5011 charges a 1nF load in 60µs typical with no external components. Faster switching is achieved by adding two 1nF charge pump capacitors. Operation down to 4.75V allows the MIC5011 to drive standard MOSFETs in 5V low-side applications by boosting the gate voltage above the logic supply. In addition, multiple paralleled MOSFETs can be driven by a single MIC5011 for ultra-high current applications.

Other members of the Micrel predriver family include the MIC5010 full-featured predriver, MIC5012 dual predriver, and MIC5013 protected 8-pin predriver.

Features

- 4.75V to 32V operation
- Less than 1µA standby current in the "off" state
- Internal charge pump to drive the gate of an N-channel power FET above supply
- MIL-STD-883 Method 5004/5005 version available
- Available in small outline SOIC packages
- Internal zener clamp for gate protection
- Minimum external parts count
- Can be used to boost drive to low-side power FETs operating on logic supplies
- 25µs typical turn-on time with optional external capacitors
- Implements high- or low-side drivers

Applications

- Lamp drivers
- Relay and solenoid drivers
- Heater switching
- Power bus switching

Typical Applications

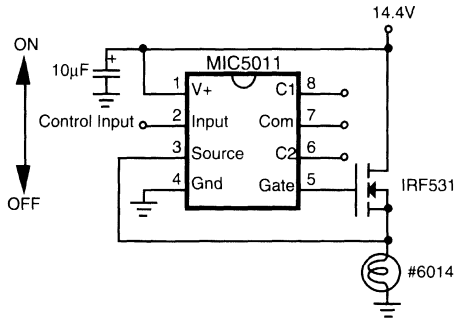


Figure 1. High Side Driver

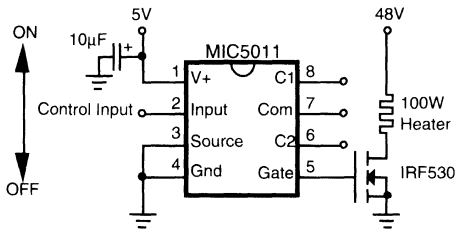


Figure 2. Low Side Driver

Ordering Information

Part Number	Temperature Range	Package
MIC5011BN	–40°C to +85°C	8-pin Plastic DIP
MIC5011BJ	–40°C to +85°C	8-pin Ceramic DIP
MIC5011BM	–40°C to +85°C	8-pin SOIC
MIC5011AJ	–55°C to +125°C	8-pin Ceramic DIP
MIC5011AJB*	–55°C to +125°C	8-pin Ceramic DIP

* AJB indicates units screened to MIL-STD 883, Method 5004, condition B, and burned-in for 1-week.

Note: The MIC5011 is ESD sensitive.

Absolute Maximum Ratings (Note 1, 2)

Supply Voltage (V^+), Pin 1	–0.5V to 36V
Input Voltage, Pin 2	–10V to V^+
Source Voltage, Pin 3	–10V to V^+
Current into Pin 3	50mA
Gate Voltage, Pin 5	–1V to 50V
Junction Temperature	150°C

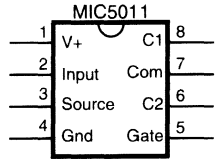
Operating Ratings (Notes 1, 2)

Power Dissipation	1.25W
θ_{JA} (Plastic DIP)	100°C/W
θ_{JA} (Ceramic DIP)	125°C/W
θ_{JA} (SOIC)	170°C/W
Ambient Temperature: B version	–40°C to +85°C
Ambient Temperature: A version	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C
Supply Voltage (V^+), Pin 1	4.75V to 32V high side 4.75V to 15V low side

Pin Description (Refer to **Typical Applications**)

Pin Number	Pin Name	Pin Function
1	V^+	Supply; must be decoupled to isolate from large transients caused by the power FET drain. 10µF is recommended close to pins 1 and 4.
2	Input	Turns on power MOSFET when taken above threshold (3.5V typical). Requires <1 µA to switch.
3	Source	Connects to source lead of power FET and is the return for the gate clamp zener. Can safely swing to –10V when turning off inductive loads.
4	Ground	
5	Gate	Drives and clamps the gate of the power FET. Will be clamped to approximately –0.7V by an internal diode when turning off inductive loads.
6, 7, 8	C2, Com, C1	Optional 1nF capacitors reduce gate turn-on time; C2 has dominant effect.

Pin Configuration



Electrical Characteristics (Note 3) Test circuit. T_A = –55°C to +125°C, V^+ = 15V, all switches open, unless otherwise specified.

Parameter	Conditions		Min	Typical	Max	Units
Supply Current, I_1	V^+ = 32V	V_{IN} = 0V, S2 closed		0.1	10	µA
		V_{IN} = V^+ = 32V		8	20	mA
	V^+ = 5V	V_{IN} = 5V, S2 closed		1.6	4	mA
Logic Input Voltage	V^+ = 4.75V	Adjust V_{IN} for V_{GATE} low			2	V
		Adjust V_{IN} for V_{GATE} high	4.5			V
	V^+ = 15V	Adjust V_{IN} for V_{GATE} high	5.0			V
Logic Input Current, I_2	V^+ = 32V	V_{IN} = 0V	–1			µA
		V_{IN} = 32V			1	µA
Input Capacitance	Pin 2			5		pF
Gate Drive, V_{GATE}	S1, S2 closed,	V^+ = 4.75V, I_{GATE} = 0, V_{IN} = 4.5V	7	10		V
	V_S = V+, V_{IN} = 5V	V^+ = 15V, I_{GATE} = 100µA, V_{IN} = 5V	24	27		V
Zener Clamp,	S2 closed, V_{IN} = 5V	V^+ = 15V, V_S = 15V	11	12.5	15	V
$V_{GATE} - V_{SOURCE}$		V^+ = 32V, V_S = 32V	11	13	16	V
Gate Turn-on Time, t_{ON} (Note 4)	V_{IN} switched from 0 to 5V; measure time for V_{GATE} to reach 20V			25	50	µs
Gate Turn-off Time, t_{OFF}	V_{IN} switched from 5 to 0V; measure time for V_{GATE} to reach 1V			4	10	µs

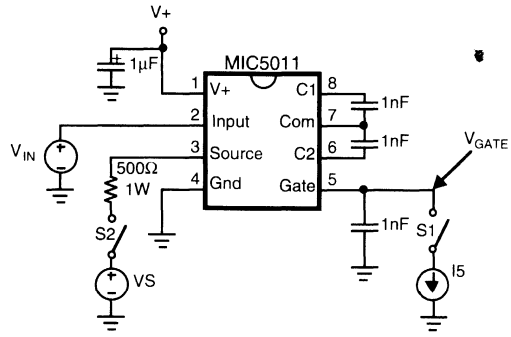
Note 1 **Absolute Maximum Ratings** indicate limits beyond which damage to the device may occur. Electrical specifications do not apply when operating the device beyond its specified **Operating Ratings**.

Note 2 The MIC5011 is ESD sensitive.

Note 3 Minimum and maximum **Electrical Characteristics** are 100% tested at T_A = 25°C and T_A = 85°C, and 100% guaranteed over the entire range. Typicals are characterized at 25°C and represent the most likely parametric norm.

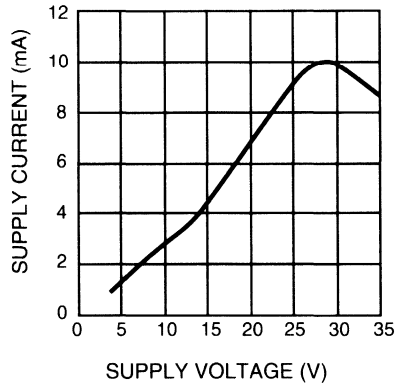
Note 4 Test conditions reflect worst case high-side driver performance. Low-side and bootstrapped topologies are significantly faster—see **Applications Information**. Maximum value of switching speed seen at 125°C, units operated at room temperature will reflect the typical values shown.

Test Circuit

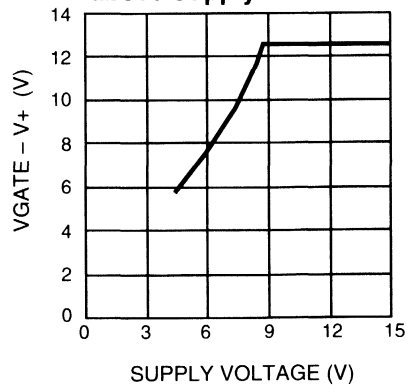


Typical Characteristics (Continued)

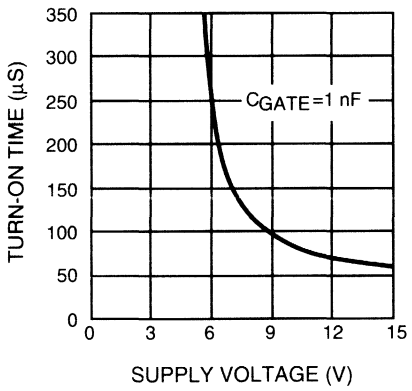
Supply Current



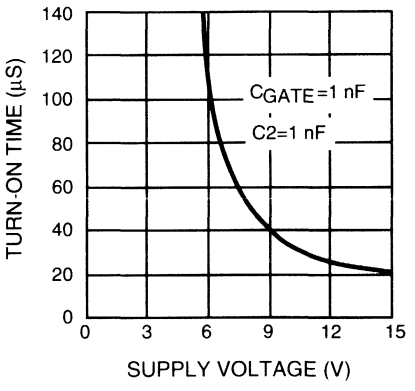
DC Gate Voltage above Supply



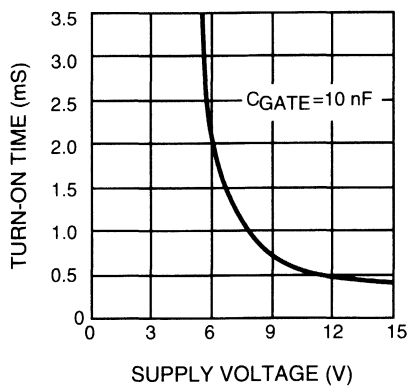
High-side Turn-on Time*



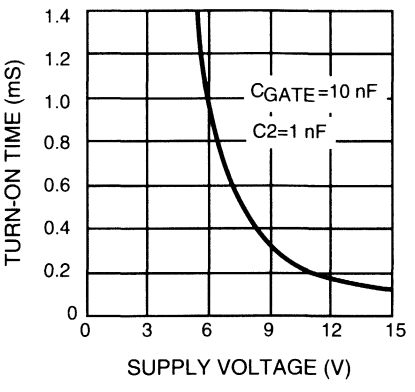
High-side Turn-on Time*



High-side Turn-on Time*



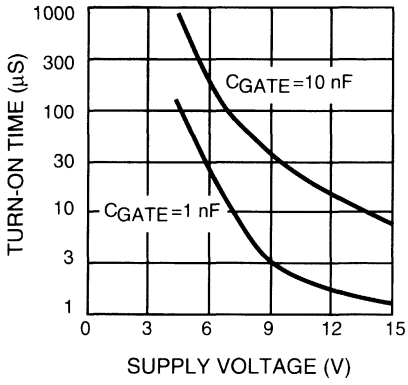
High-side Turn-on Time*



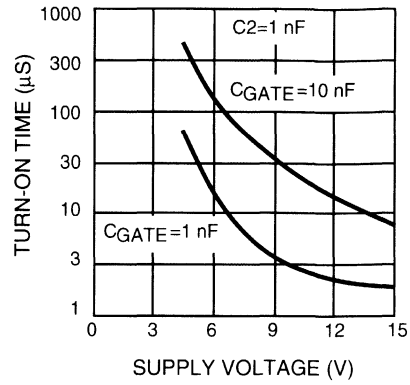
* Time for gate to reach $V^+ + 5V$ in test circuit with $VS = V^+ - 5V$.

Typical Characteristics (Continued)

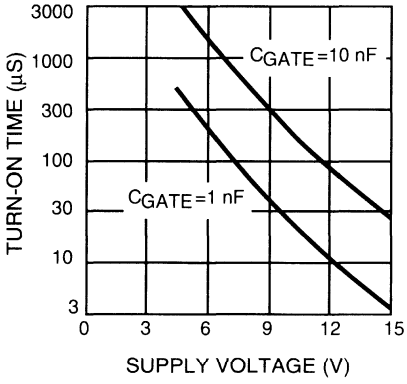
Low-side Turn-on Time for Gate = 5V



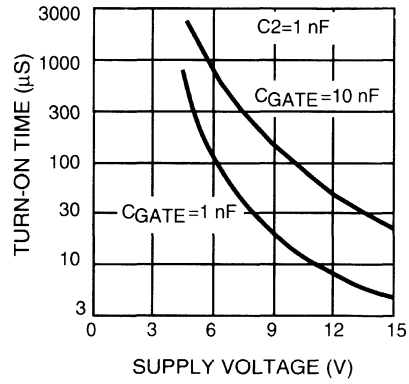
Low-side Turn-on Time for Gate = 5V



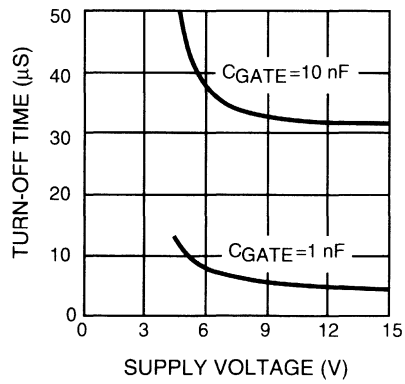
Low-side Turn-on Time for Gate = 10V



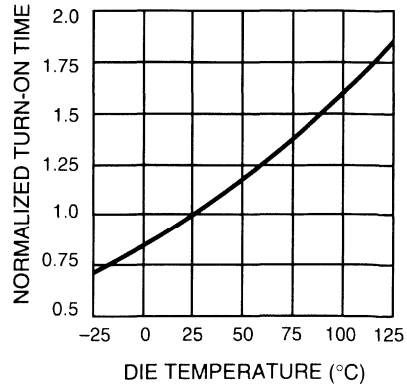
Low-side Turn-on Time for Gate = 10V

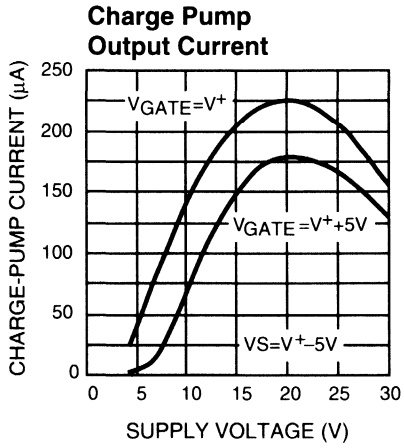


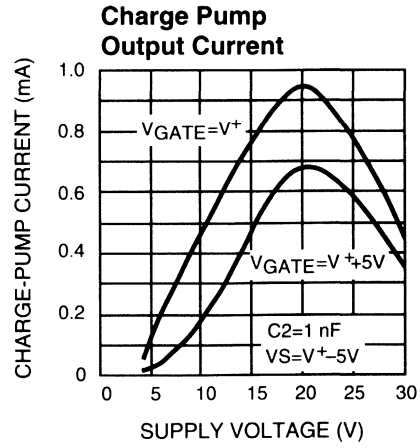
Turn-off Time



Turn-on Time

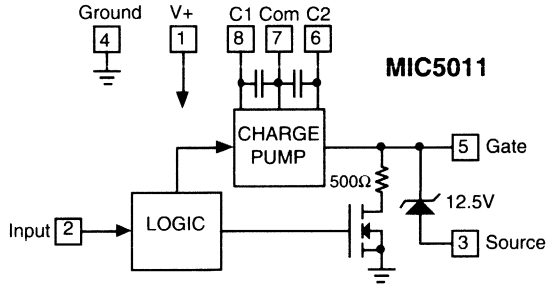






2

Block Diagram



Applications Information

Functional Description (Refer to Block Diagram)

The MIC5011 functions are controlled via a logic block connected to the input pin 2. When the input is low, all functions are turned off for low standby current and the gate of the power MOSFET is also held low through 500Ω to an N-channel switch. When the input is taken above the turn-on threshold (3.5V typical), the N-channel switch turns off and the charge pump is turned on to charge the gate of the power FET.

The charge pump incorporates a 100kHz oscillator and on-chip pump capacitors capable of charging 1nF to 5V above supply in 60µs typical. With the addition of 1nF capacitors at C1 and C2, the turn-on time is reduced to 25µs typical (see Figure 3). The charge pump is capable of pumping the gate up to over twice the supply voltage. For this reason, a zener clamp (12.5V typical) is provided between the gate pin 5 and source pin 3 to prevent exceeding the V_{GS} rating of the MOSFET at high supplies.

Applications Information (Continued)

Construction Hints

High current pulse circuits demand equipment and assembly techniques that are more stringent than normal, low current lab practices. The following are the sources of pitfalls most often encountered during prototyping. *Supplies*: many bench power supplies have poor transient response. Circuits that are being pulse tested, or those that operate by pulse-width modulation will produce strange results when used with a supply that has poor ripple rejection, or a peaked transient response. Always monitor the power supply voltage that appears at the drain of a high-side driver (or the supply side of the load in a low-side driver) with an oscilloscope. It is not uncommon to find bench power supplies in the 1 kW class that overshoot or undershoot by as much as 50% when pulse loaded. Not only will the load current and voltage measurements be affected, but it is possible to over-stress various components—especially electrolytic capacitors—with possibly catastrophic results. A 10µF supply bypass capacitor at the chip is recommended.

Residual Resistances: Resistances in circuit connections may also cause confusing results. For example, a circuit may employ a 50mΩ power MOSFET for low drop, but careless construction techniques could easily add 50 to 100mΩ resistance. Do not use a socket for the MOSFET. If the MOSFET is a TO-220 type package, make high-current drain connections to the tab. Wiring losses have a profound effect on high-current circuits. A floating millivoltmeter can identify connections that are contributing excess drop under load.

Circuit Topologies

The MIC5011 is suited for use with standard MOSFETs in high- or low-side driver applications. In addition, the MIC5011 works well in applications where, for faster switching times, the supply is bootstrapped from the MOSFET source output. Low voltage, high-side drivers (such as shown in Figure 1) are the slowest; their speed is reflected in the gate turn-on time specifications. The fastest drivers are the low-side and bootstrapped high-side types (Figures 2 and 4). Load current switching times are often much faster than the time to full gate enhancement, depending on the circuit type, the MOSFET, and the load. Turn-off times are essentially the same for all circuits (less than 10µs to V_{GS} = 1V). The choice of one topology over another is based on a combination of considerations including speed, voltage, and desired system characteristics.

High-Side Driver (Figure 1). The high-side topology works well down to V^+ = 7V with standard MOSFETs. From 4.75 to 7V supply, a logic-level MOSFET can be substituted since the MIC5011 will not reach 10V gate enhancement (10V is the maximum rating for logic-compatible MOSFETs).

High-side drivers implemented with MIC501X predrivers are self-protected against inductive switching transients. During turn-off an inductive load will force the MOSFET source 5V or more below ground, while the MIC5011 holds the gate at ground potential. The MOSFET is forced into conduction, and it dissipates the energy stored in the load inductance. The MIC5011 source pin (3) is designed to withstand this negative excursion without damage. External clamp diodes are unnecessary.

Low-Side Driver (Figure 2). A key advantage of the low-side topology is that the load supply is limited only by the MOSFET BVDSS rating. Clamping may be required to protect the MOSFET drain terminal from inductive switching transients. The MIC5011 supply should be limited to 15V in low-side topologies, otherwise a large current will be forced through the gate clamp zener.

Low-side drivers constructed with the MIC501X family are also fast; the MOSFET gate is driven to near supply immediately when commanded ON. Typical circuits achieve 10V enhancement in 10µs or less on a 12 to 15V supply.

Modifying Switching Times (Figure 3). High-side switching times can be improved by a factor of 2 or more by adding external charge pump capacitors of 1nF each. In cost-sensitive applications, omit C1 (C2 has a dominant effect on speed).

Do not add external capacitors to the MOSFET gate. Add a resistor (1kΩ to 51kΩ) in series with the gate to slow down the switching time.

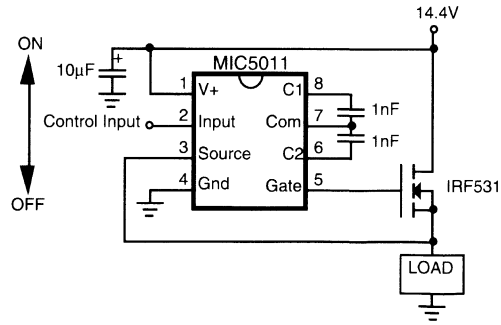


Figure 3. High Side Driver with External Charge Pump Capacitors

Bootstrapped High-Side Driver (Figure 4). The speed of a high-side driver can be increased to better than 10µs by bootstrapping the supply off of the MOSFET source. This topology can be used where the load is pulse-width modulated (100Hz to 20kHz), or where it is energized continuously. The Schottky barrier diode prevents the MIC5011 supply pin from dropping more than 200mV below the drain supply, and it also improves turn-on time on supplies of less than 10V. Since the supply current in the "off" state is only a small leakage, the 100nF bypass capacitor tends to remain charged for several seconds after the MIC5011 is turned off. In a PWM application the chip supply is sustained at a higher potential than the system supply, which improves switching time.

Applications Information (Continued)

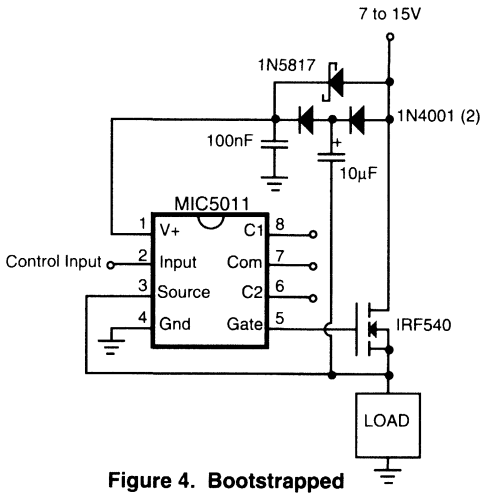


Figure 4. Bootstrapped High-Side Driver

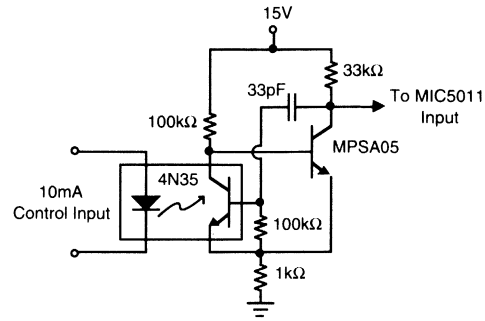


Figure 5. Improved Opto-Isolator Performance

Opto-Isolated Interface (Figure 5). Although the MIC5011 has no special input slew rate requirement, the lethargic transitions provided by an opto-isolator may cause oscillations on the rise and fall of the output. The circuit shown accelerates the input transitions from a 4N35 opto-isolator by adding hysteresis. Opto-isolators are used where the control circuitry cannot share a common ground with the MIC5011 and high-current power supply, or where the control circuitry is located remotely. This implementation is intrinsically safe; if the control line is severed the MIC5011 will turn OFF.

Industrial Switch (Figure 6). The most common manual control for industrial loads is a push button on/off switch. The "on" button is physically arranged in a recess so that in a panic situation the "off" button, which extends out from the control box, is more easily pressed. This circuit is compatible with control boxes such as the CR2943 series (GE). The circuit is configured so that if both switches close simultaneously, the "off" button has precedence.

This application also illustrates how two (or more) MOSFETs can be paralleled. This reduces the switch drop, and distributes the switch dissipation into multiple packages.

High-Voltage Bootstrap (Figure 7). Although the MIC5011 is limited to operation on 4.75 to 32V supplies, a floating bootstrap arrangement can be used to build a high-side switch that operates on much higher voltages. The MIC5011 and MOSFET are configured as a low-side driver, but the load is connected in series with ground.

Power for the MIC5011 is supplied by a charge pump. A 20kHz square wave (15Vp-p) drives the pump capacitor and delivers current to a 100µF storage capacitor. A zener

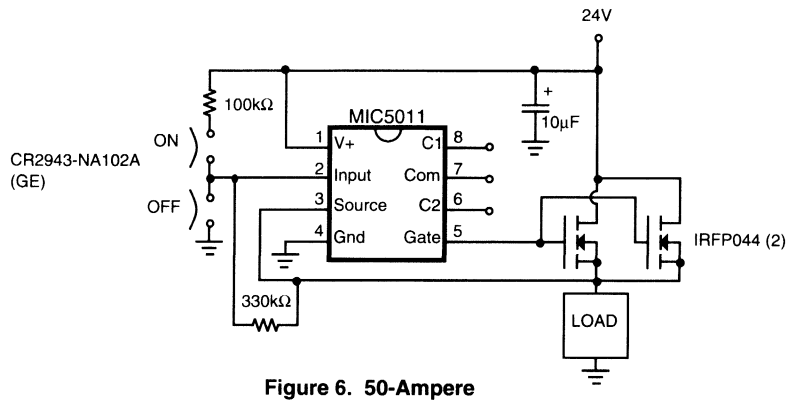


Figure 6. 50-Ampere Industrial Switch

Applications Information (Continued)

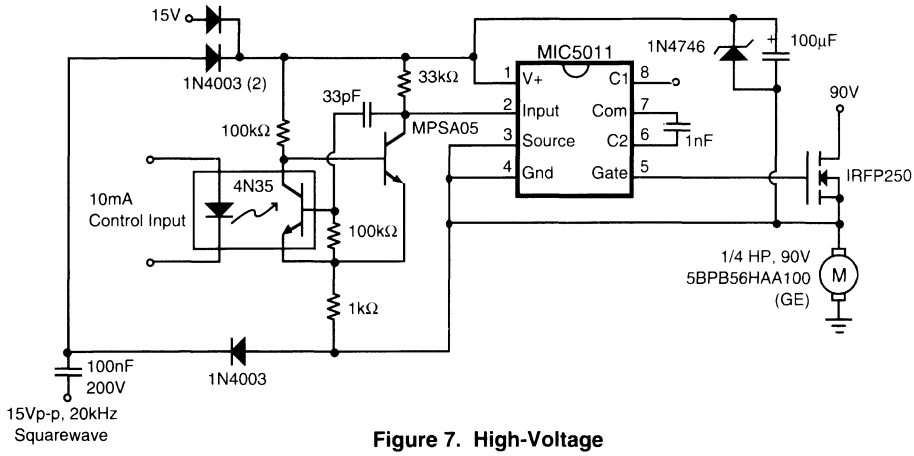


Figure 7. High-Voltage Bootstrapped Driver

diode limits the supply to 18V. When the MIC5011 is off, power is supplied by a diode connected to a 15V supply. The circuit of Figure 5 is put to good use as a barrier between low voltage control circuitry and the 90V motor supply.

Half-Bridge Motor Driver (Figure 8). Closed loop control of motor speed requires a half-bridge driver. This topology presents an extra challenge since the two output devices should not cross conduct (shoot-through) when switching. Cross conduction increases output device power dissipation. Speed is also important, since PWM control requires the outputs to switch in the 2 to 20kHz range.

The circuit of Figure 8 utilizes fast configurations for both the top- and bottom-side drivers. Delay networks at each input provide a 2 to 3µs dead time effectively eliminating cross conduction. Two of these circuits can be connected together to form an H-bridge for locked antiphase or sign/magnitude control.

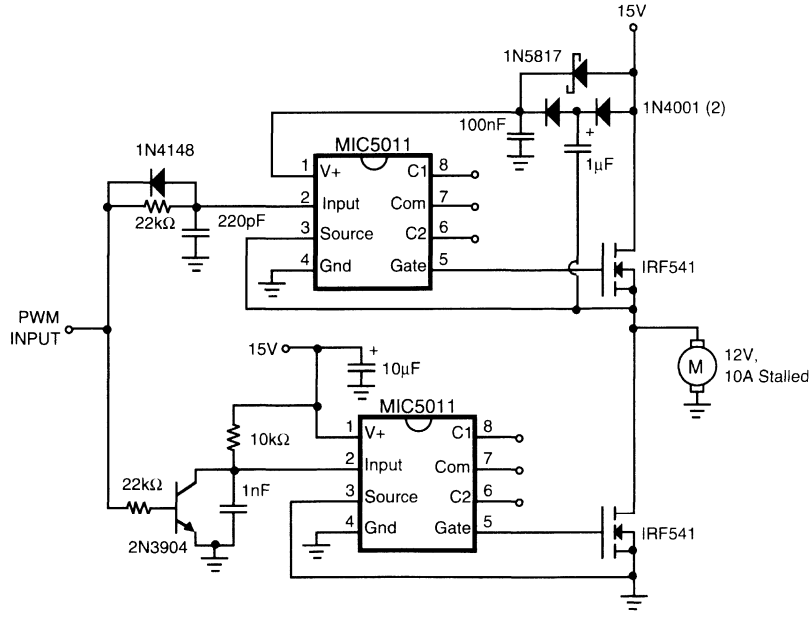


Figure 8. Half-Bridge Motor Driver

Applications Information (Continued)

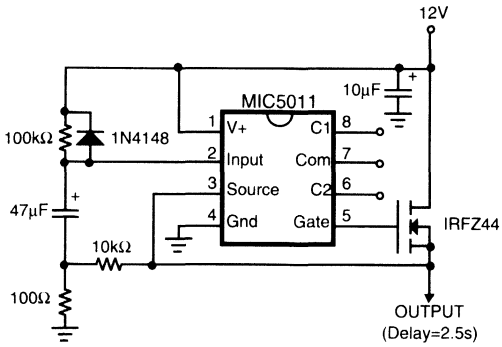


Figure 9. 30 Ampere Time-Delay Relay

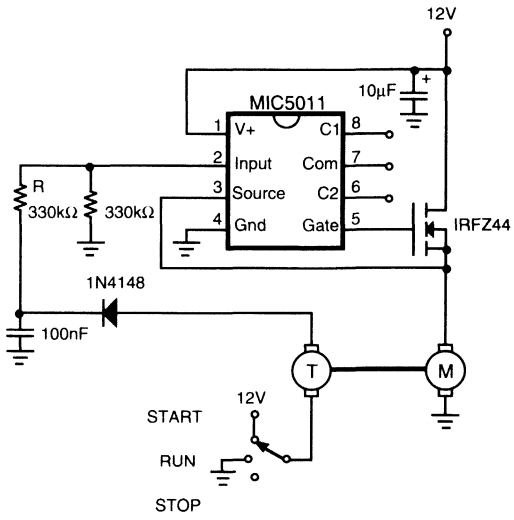


Figure 10. Motor Stall Shutdown

Time-Delay Relay (Figure 9). The MIC5011 forms the basis of a simple time-delay relay. As shown, the delay commences when power is applied, but the 100kΩ/1N4148 could be independently driven from an external source such as a switch or another high-side driver to give a delay relative to some other event in the system. Hysteresis has been added to guarantee clean switching at turn-on.

Motor Driver with Stall Shutdown (Figure 10). Tachometer feedback can be used to shut down a motor driver circuit when a stall condition occurs. The control switch is a 3-way type; the "START" position is momentary and forces the driver ON. When released, the switch returns to the "RUN" position, and the tachometer's output is used to hold the MIC5011 input ON. If the motor slows down, the tach output is reduced, and the MIC5011 switches OFF. Resistor "R" sets the shutdown threshold.

Electronic Governor (Figure 11). The output of an ac tachometer can be used to form a PWM loop to maintain the speed of a motor. The tachometer output is rectified, partially filtered, and fed back to the input of the MIC5011. When the motor is stalled there is no tachometer output, and MIC5011 input is pulled high delivering full power to the motor. If the motor spins fast enough, the tachometer output is sufficient to pull the MIC5011 input low, shutting the output off. Since the rectified waveform is only partially filtered, the input oscillates around its threshold causing the MIC5011 to switch on and off at the frequency of the tachometer signal. A PWM action results since the average dc voltage at the input decreases as the motor spins faster. The 1kΩ potentiometer is used to set the running speed of the motor. Loop gain (and speed regulation) is increased by increasing the value of the 100nF filter capacitor.

The performance of such a loop is imprecise, but stable and inexpensive. A more elaborate loop would consist of a PWM controller and a half-bridge.

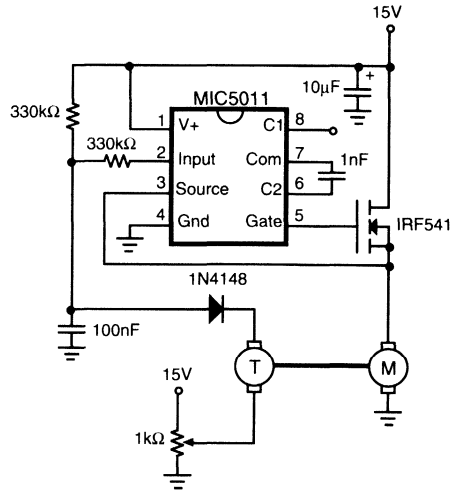


Figure 11. Electronic Governor

Applications Information (Continued)

Gate Control Circuit

When applying the MIC5011, it is helpful to understand the operation of the gate control circuitry (see Figure 12). The gate circuitry can be divided into two sections: 1) charge pump (oscillator, Q1-Q5, and the capacitors) and 2) gate turn-off switch (Q6).

When the MIC5011 is in the OFF state, the oscillator is turned off, thereby disabling the charge pump. Q5 is also turned off, and Q6 is turned on. Q6 holds the gate pin (G) at ground potential which effectively turns the external MOSFET off.

Q6 is turned off when the MIC5011 is commanded on, and Q5 pulls the gate up to supply (through 2 diodes). Next, the charge pump begins supplying current to the gate. The gate accepts charge until the gate-source voltage reaches 12.5V and is clamped by the zener diode.

A 2-output, three-phase clock switches Q1-Q4, providing a quasi-tripling action. During the initial phase Q4 and Q2 are ON. C1 is discharged, and C2 is charged to supply through Q5. For the second phase Q4 turns off and Q3 turns on, pushing pin C2 above supply (charge is dumped into the gate). Q3 also charges C1. On the third phase Q2 turns off and Q1 turns on, pushing the common point of the two capacitors above supply. Some of the charge in C1 makes its way to the gate. The sequence is repeated by turning Q2 and Q4 back on, and Q1 and Q3 off.

In a low-side application operating on a 12 to 15V supply, the MOSFET is fully enhanced by the action of Q5 alone. On supplies of more than approximately 14V, current flows directly from Q5 through the zener diode to ground. To prevent excessive current flow, the MIC5011 supply should be limited to 15V in low-side applications.

The action of Q5 makes the MIC5011 operate quickly in low-side applications. In high-side applications Q5 precharges the MOSFET gate to supply, leaving the charge pump to carry the gate up to full enhancement 10V above supply. Bootstrapped high-side drivers are as fast as low-side drivers since the chip supply is boosted well above the drain at turn-on.

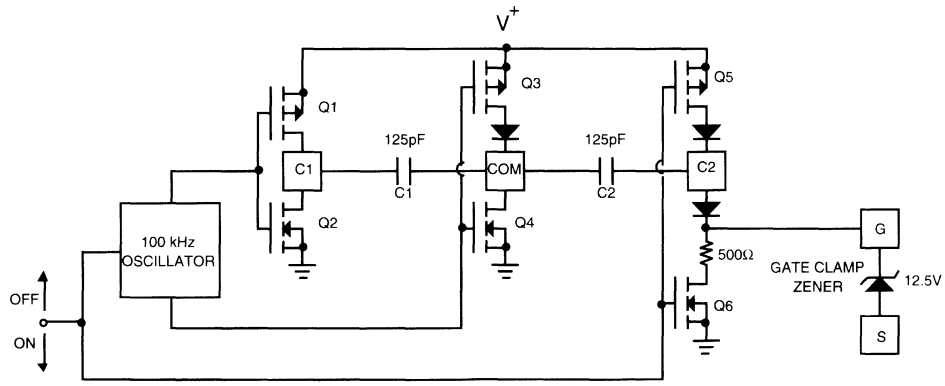


Figure 12. Gate Control Circuit Detail

MIC5012

Dual Power MOSFET Predriver

General Description

The MIC5012 is the dual member of the Micrel MIC501X predriver family. These ICs are designed to drive the gate of an N-channel power MOSFET above the supply rail in high-side power switch applications. The 14-pin MIC5012 is extremely easy to use, requiring only a power FET and nominal supply decoupling to implement either a high- or low-side switch.

The MIC5012 charges a 1nF load in 60µs typical. Operation down to 4.75V allows the MIC5012 to drive standard MOSFETs in 5V low-side applications by boosting the gate voltage above the logic supply. In addition, multiple, paralleled MOSFETs can be driven by a single MIC5012 for ultra-high current applications.

Other members of the Micrel predriver family include the MIC5010 full-featured predriver, MIC5011 minimum parts count predriver, and MIC5013 protected 8-pin predriver.

Features

- 4.75V to 32V operation
- 2 independent predrivers; implements high and low side drivers
- Less than 1µA standby current in the "off" state per channel
- MIL-STD-883 Method 5004/5005 version available
- Available in small outline SOIC packages
- Internal charge pump to drive the gate of an N-channel power FET above supply
- Internal zener clamp for gate protection
- Minimum external parts count
- Can be used to boost drive to low-side power FETs operating on logic supplies
- Independent supply pins for half-bridge applications

Applications

- Lamp drivers
- Motion Control
- Heater switching
- Power bus switching
- Half or full H-bridge drivers

Typical Applications

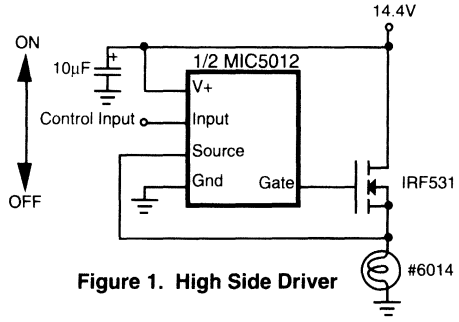


Figure 1. High Side Driver

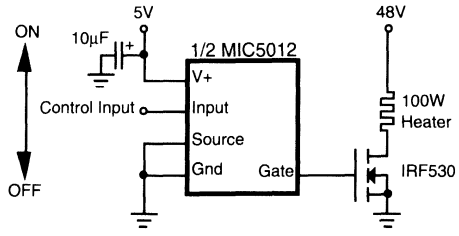


Figure 2. Low Side Driver

Ordering Information

Part Number	Temperature Range	Package
MIC5012BN	–40°C to +85°C	14-pin Plastic DIP
MIC5012BJ	–40°C to +85°C	14-pin Ceramic DIP
MIC5012BWM	–40°C to +85°C	16-pin Wide SOIC
MIC5012AJ	–55°C to +125°C	14-pin Ceramic DIP
MIC5012AJB*	–55°C to +125°C	14-pin Ceramic DIP

* AJB indicates units screened to MIL-STD 883, Method 5004, condition B, and burned-in for 1-week.

Note: The MIC5012 is ESD sensitive.

Absolute Maximum Ratings (Note 1, 2)

Supply Voltage (V^+), Pins 10, 12	–0.5V to 36V
Input Voltage, Pins 11, 14	–10V to V^+
Source Voltage, Pins 2, 5	–10V to V^+
Current into Pins 2, 5	50mA
Gate Voltage, Pins 4, 6	–1V to 50V
Junction Temperature	150°C

Operating Ratings (Notes 1, 2)

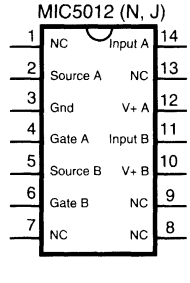
Power Dissipation	1.56W
θ_{JA} (Plastic DIP)	80 °C/W
θ_{JA} (Ceramic DIP)	105°C/W
θ_{JA} (SOIC)	105°C/W
Ambient Temperature: B version	–40°C to +85°C
Ambient Temperature: A version	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C
Supply Voltage (V^+), Pin 1	4.75V to 32V high side 4.75V to 15V low side

Pin Description (Refer to **Typical Applications**)

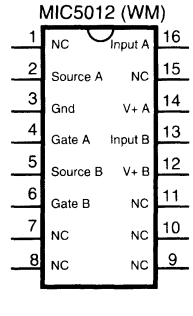
DIP Pin Number	Pin Name	Pin Function
12, 10	V^+	Supply; must be decoupled to isolate from large transients caused by the power FET drain. 10µF is recommended close to pins 1 and 4.
14, 11	Input	Turns on power MOSFET when taken above threshold (3.5V typical). Requires <1 µA to switch.
2, 5	Source	Connects to source lead of power FET and is the return for the gate clamp zener. Can safely swing to –10V when turning off inductive loads.
3	Ground	
4, 6	Gate	Drives and clamps the gate of the power FET. Clamped to approximately –0.7V by an internal diode when turning off inductive loads.

Pin Configuration

MIC5012 (N, J)



MIC5012 (WM)



Electrical Characteristics (Note 3) Test circuit. T_A = –55°C to +125°C, V^+ = 15V, all switches open, unless otherwise specified.

Parameter	Conditions		Min	Typical	Max	Units
Supply Current (per section)	V^+ = 32V	V_{IN} = 0V, S2 closed		0.1	10	µA
		V_{IN} = V_S = 32V		8	20	mA
	V^+ = 5V	V_{IN} = 5V, S2 closed		1.6	4	mA
Logic Input Voltage	V^+ = 4.75V	Adjust V_{IN} for V_{GATE} low			2	V
		Adjust V_{IN} for V_{GATE} high	4.5			V
	V^+ = 15V	Adjust V_{IN} for V_{GATE} high	5.0			V
Logic Input Current, I_2	V^+ = 32V	V_{IN} = 0V	–1			µA
		V_{IN} = 32V			1	µA
Input Capacitance	Pins 11, 14			5		pF
Gate Drive, V_{GATE}	S1, S2 closed,	V^+ = 4.75V, I_{GATE} = 0, V_{IN} = 4.5V	7	10		V
	V_S = V+, V_{IN} = 5V	V^+ = 15V, I_{GATE} = 100µA, V_{IN} = 5V	24	27		V
Zener Clamp, $V_{GATE} - V_{SOURCE}$	S2 closed, V_{IN} = 5V	V^+ = 15V, V_S = 15V	11	12.5	15	V
		V^+ = 32V, V_S = 32V	11	13	16	V
Gate Turn-on Time, t_{ON} (Note 4)	V_{IN} switched from 0 to 5V; measure time for V_{GATE} to reach 20V			60	200	µs
Gate Turn-off Time, t_{OFF}	V_{IN} switched from 5 to 0V; measure time for V_{GATE} to reach 1V			4	10	µs

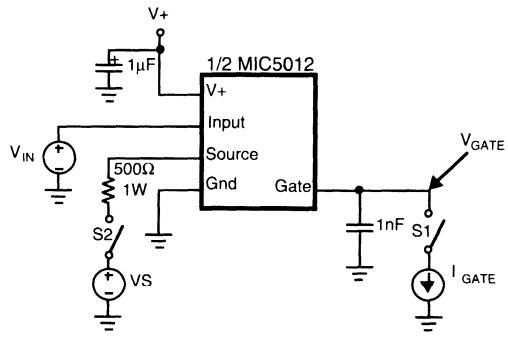
Note 1 **Absolute Maximum Ratings** indicate limits beyond which damage to the device may occur. Electrical specifications do not apply when operating the device beyond its specified **Operating Ratings**.

Note 2 The MIC5012 is ESD sensitive.

Note 3 Minimum and maximum **Electrical Characteristics** are 100% tested at T_A = 25°C and T_A = 85°C, and 100% guaranteed over the entire range. Typicals are characterized at 25°C and represent the most likely parametric norm.

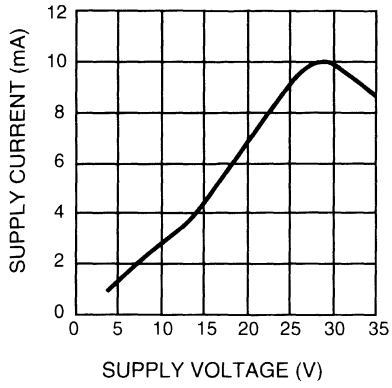
Note 4 Test conditions reflect worst case high-side driver performance. Low-side and bootstrapped topologies are significantly faster—see **Applications Information**. Maximum value of switching speed seen at 125°C, units operated at room temperature will reflect the typical values shown.

Test Circuit

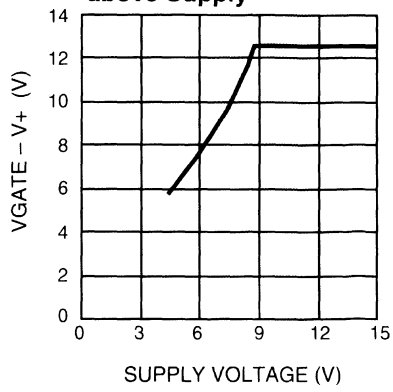


Typical Characteristics (Continued)

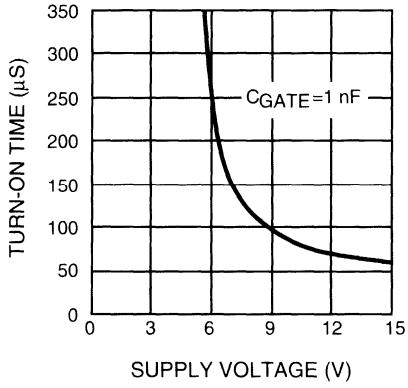
Supply Current



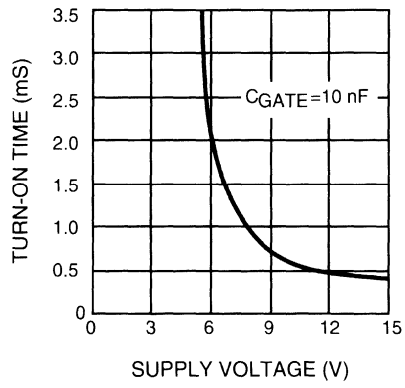
DC Gate Voltage above Supply



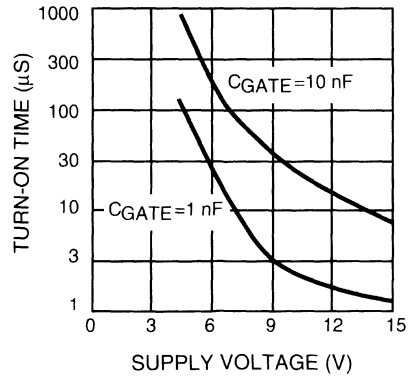
High-side Turn-on Time*



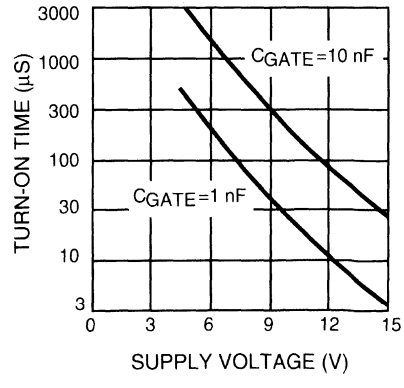
High-side Turn-on Time*



Low-side Turn-on Time for Gate = 5V



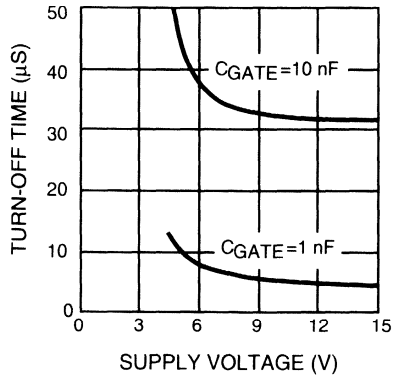
Low-side Turn-on Time for Gate = 10V



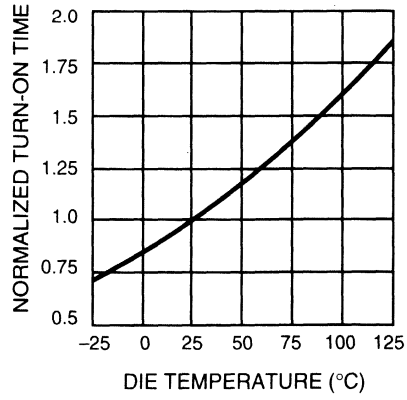
* Time for gate to reach $V^+ + 5V$ in test circuit with $VS = V^+ - 5V$.

Typical Characteristics (Continued)

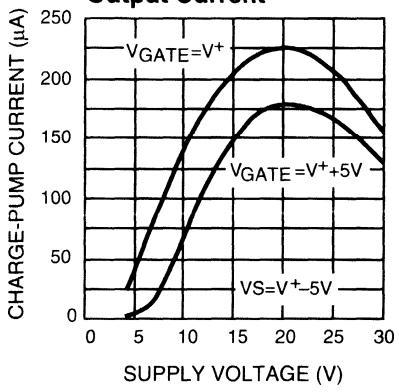
Turn-off Time



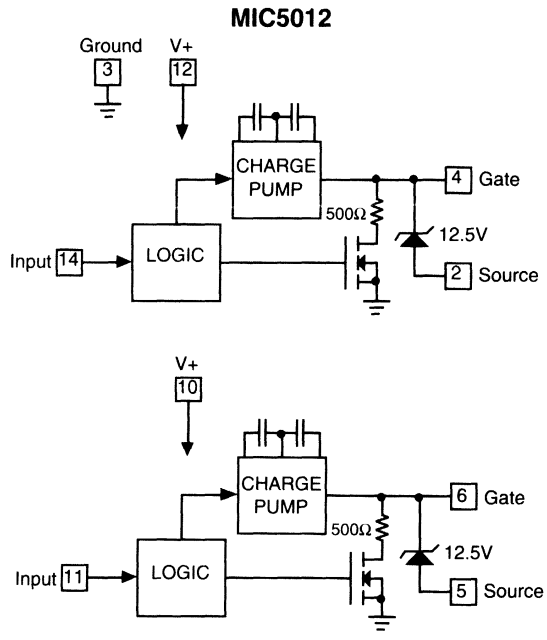
Turn-on Time



Charge Pump Output Current



Block Diagram



Applications Information

Functional Description (Refer to **Block Diagram**)

The MIC5012 consists of two independent predrivers sharing a common ground. The functions are controlled via a logic block connected to the logic input. When the input is low, all functions are turned off for low standby current and the gate of the power MOSFET is also held low through 500Ω to an N-channel switch. When the input is taken above the turn-on threshold (3.5V typical), the N-channel switch turns off and the charge pump is turned on to charge the gate of the power FET.

The charge pump incorporates a 100kHz oscillator and on-chip pump capacitors capable of charging 1nF to 5V above supply in 60µs typical. The charge pump is capable of pumping the gate up to over twice the supply voltage. For this reason, a zener clamp (12.5V typical) is provided between the gate pin and source pin to prevent exceeding the V_{GS} rating of the MOSFET at high supplies.

Since the supply pins are independent, the two predrivers contained in the MIC5012 can be operated from separate supplies of different values (see Figure 6).

Construction Hints

High current pulse circuits demand equipment and assembly techniques that are more stringent than normal, low current lab practices. The following are the sources of

Applications Information (Continued)

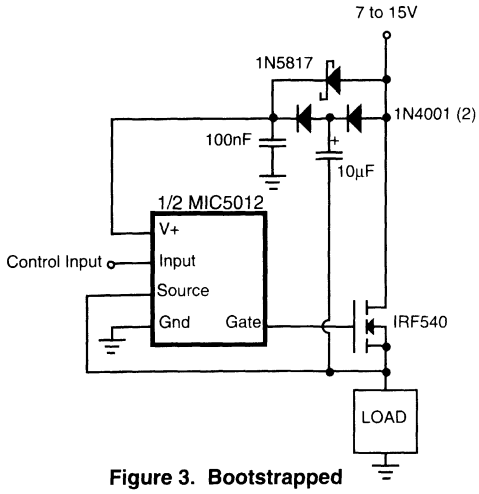


Figure 3. Bootstrapped High-Side Driver

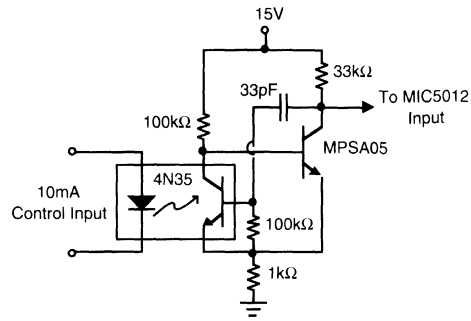


Figure 4. Improved Opto-Isolator Performance

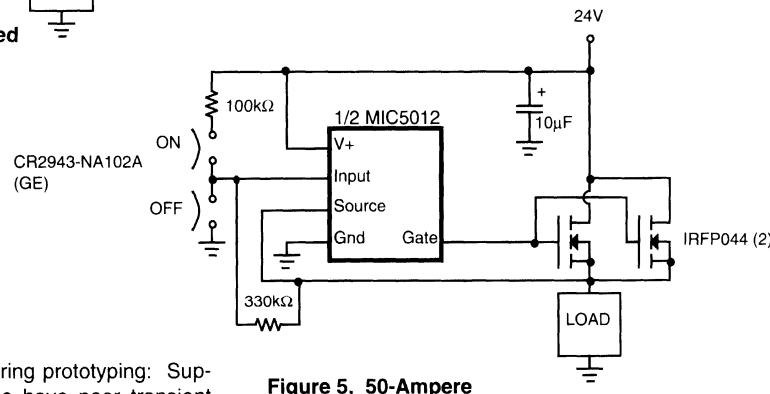


Figure 5. 50-Ampere Industrial Switch

pitfalls most often encountered during prototyping: Supplies: many bench power supplies have poor transient response. Circuits that are being pulse tested, or those that operate by pulse-width modulation will produce strange results when used with a supply that has poor ripple rejection, or a peaked transient response. Always monitor the power supply voltage that appears at the drain of a high-side driver (or the supply side of the load in a low-side driver) with an oscilloscope. It is not uncommon to find bench power supplies in the 1kW class that overshoot or undershoot by as much as 50% when pulse loaded. Not only will the load current and voltage measurements be affected, but it is possible to over-stress various components—especially electrolytic capacitors—with possibly catastrophic results. A 10µF supply bypass capacitor at the chip is recommended.

Residual Resistances: Resistances in circuit connections may also cause confusing results. For example, a circuit may employ a 50mΩ power MOSFET for low drop, but careless construction techniques could easily add 50 to 100mΩ resistance. Do not use a socket for the MOSFET. If the MOSFET is a TO-220 type package, make high-current drain connections to the tab. Wiring losses have a profound effect on high-current circuits. A floating millivoltmeter can identify connections that are contributing excess drop under load.

Circuit Topologies

The MIC5012 is suited for use with standard MOSFETs in high- or low-side driver applications. In addition, the MIC5012 works well in applications where, for faster switching times, the supply is bootstrapped from the MOSFET source output. Low voltage, high-side drivers (such as shown in Figure 1) are the slowest; their speed is reflected in the gate turn-on time specifications. The fastest drivers are the low-side and bootstrapped high-side types (Figures 2 and 4). Load current switching times are often much faster than the time to full gate enhancement, depending on the circuit type, the MOSFET, and the load. Turn-off times are essentially the same for all circuits (less than 10µs to V_{GS} = 1V). The choice of one topology over another is based on a combination of considerations including speed, voltage, and desired system characteristics.

High-Side Driver (Figure 1). The high-side topology works well down to V^+ = 7V with standard MOSFETs. From 4.75 to 7V supply, a logic-level MOSFET can be substituted since the MIC5012 will not reach 10V gate enhancement (10V is the maximum rating for logic-compatible MOSFETs).

Applications Information (Continued)

High-side drivers implemented with MIC501X predrivers are self-protected against inductive switching transients. During turn-off an inductive load will force the MOSFET source 5V or more below ground, while the MIC5012 holds the gate at ground potential. The MOSFET is forced into conduction, and it dissipates the energy stored in the load inductance. The MIC5012 source pin is designed to withstand this negative excursion without damage. External clamp diodes are unnecessary.

Low-Side Driver (Figure 2). A key advantage of the low-side topology is that the load supply is limited only by the MOSFET BV_{DSS} rating. Clamping may be required to protect the MOSFET drain terminal from inductive switching transients. The MIC5012 supply should be limited to 15V in low-side topologies; otherwise, a large current will be forced through the gate clamp zener. The switching speed to 10V enhancement is 300µs driving 1nF on a 5V supply. On a 15V supply the turn-on time is less than 2µs to 10V

Low-side drivers constructed with the MIC501X family are also fast; the MOSFET gate is driven to near supply immediately when commanded ON. Typical circuits achieve 10V enhancement in 10µs or less on a 12 to 15V supply.

Modifying Switching Times. Do not add external capacitors to the MOSFET gate. Add a resistor (1kΩ to 51kΩ) in series with the gate to slow down the switching time.

Bootstrapped High-Side Driver (Figure 3). The speed of a high-side driver can be increased to better than 10µs by bootstrapping the supply off of the MOSFET source. This topology can be used where the load is pulse-width modulated (100Hz to 20kHz), or where it is energized continuously. The Schottky barrier diode prevents the MIC5012 supply pin from dropping more than 200mV below the drain supply, and it also improves turn-on time on supplies of less than 10V. Since the supply current in the "off" state is only a small leakage, the 100nF bypass capacitor tends to remain charged for several seconds after the MIC5012 is turned off. In a PWM application the chip supply is sustained at a higher potential than the system supply, which improves switching time.

Opto-Isolated Interface (Figure 4). Although the MIC5012 has no special input slew rate requirement, the lethargic transitions provided by an opto-isolator may cause oscillations on the rise and fall of the output. The circuit shown accelerates the input transitions from a 4N35 opto-isolator by adding hysteresis. Opto-isolators are used where the control circuitry cannot share a common ground with the MIC5012 and high-current power supply, or where the control circuitry is located remotely. This implementation is intrinsically safe; if the control line is severed the MIC5012 will turn OFF.

Industrial Switch (Figure 5). The most common manual control for industrial loads is a push button on/off switch. The "on" button is physically arranged in a recess so that in a panic situation the "off" button, which extends out from the control box, is more easily pressed. This circuit is compatible with control boxes such as the CR2943 series (GE). The circuit is configured so that if both switches close simultaneously, the "off" button has precedence.

This application also illustrates how two (or more) MOSFETs

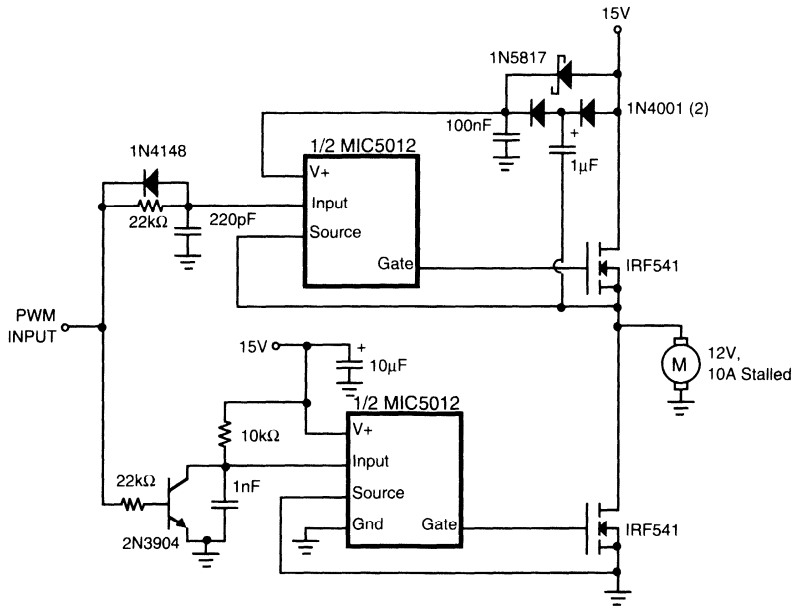


Figure 6. Half-Bridge Motor Driver

Applications Information (Continued)

can be paralleled. This reduces the switch drop, and distributes the switch dissipation into multiple packages.

Half-Bridge Motor Driver (Figure 6). Closed loop control of motor speed requires a half-bridge driver. This topology presents an extra challenge since the two output devices should not cross conduct (shoot-through) when switching. Cross conduction increases output device power dissipation. Speed is also important, since PWM control requires the outputs to switch in the 2 to 20kHz range.

The circuit of Figure 6 utilizes fast configurations for both the top- and bottom-side drivers. Delay networks at each input provide a 2 to 3µs dead time effectively eliminating cross conduction. Two of these circuits can be connected together to form an H-bridge for locked antiphase or sign/magnitude control.

Time-Delay Relay (Figure 7). The MIC5012 forms the basis of a simple time-delay relay. As shown, the delay commences when power is applied, but the 100kΩ/1N4148 could be independently driven from an external source such as a switch or another high-side driver to give a delay relative to some other event in the system. Hysteresis has been added to guarantee clean switching at turn-on.

Motor Driver with Stall Shutdown (Figure 8). Tachometer feedback can be used to shut down a motor driver circuit when a stall condition occurs. The control switch is a 3-way type; the "START" position is momentary and forces the driver ON. When released, the switch returns to the "RUN" position, and the tachometer's output is used to hold the MIC5012 input ON. If the motor slows down, the tach output is reduced, and the MIC5012 switches OFF. Resistor "R" sets the shutdown threshold.

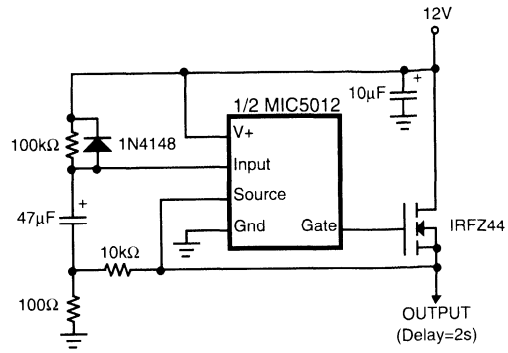


Figure 7. 30 Ampere Time-Delay Relay

Electronic Governor (Figure 9). The output of an ac tachometer can be used to form a PWM loop to maintain the speed of a motor. The tachometer output is rectified, partially filtered, and fed back to the input of the MIC5012. When the motor is stalled there is no tachometer output, and MIC5012 input is pulled high delivering full power to the motor. If the motor spins fast enough, the tachometer output is sufficient to pull the MIC5012 input low, shutting the output off. Since the rectified waveform is only partially filtered, the input oscillates around its threshold causing the MIC5012 to switch on and off at the frequency of the tachometer signal. A PWM action results since the average dc voltage at the input decreases as the motor spins faster. The 1kΩ potentiometer is used to set the running speed of the motor. Loop gain (and speed regulation) is increased by increasing the value of the 100nF filter capacitor.

The performance of such a loop is imprecise, but stable and inexpensive. A more elaborate loop would consist of a PWM controller and a half-bridge.

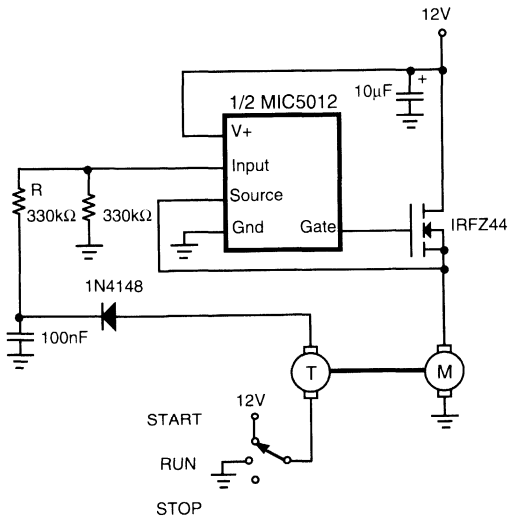


Figure 8. Motor Stall Shutdown

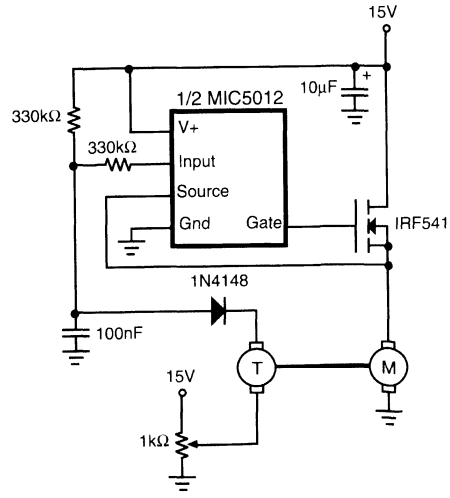


Figure 9. Electronic Governor

Applications Information (Continued)

Gate Control Circuit

When applying the MIC5012, it is helpful to understand the operation of the gate control circuitry (see Figure 12). The gate circuitry can be divided into two sections: 1) charge pump (oscillator, Q1-Q5, and the capacitors) and 2) gate turn-off switch (Q6).

When the MIC5012 is in the OFF state, the oscillator is turned off, thereby disabling the charge pump. Q5 is also turned off, and Q6 is turned on. Q6 holds the gate pin (G) at ground potential which effectively turns the external MOSFET off.

Q6 is turned off when the MIC5012 is commanded on, and Q5 pulls the gate up to supply (through 2 diodes). Next, the charge pump begins supplying current to the gate. The gate accepts charge until the gate-source voltage reaches 12.5V and is clamped by the zener diode.

A 2-output, three-phase clock switches Q1-Q4, providing a quasi-tripling action. During the initial phase Q4 and Q2 are ON. C1 is discharged, and C2 is charged to supply through Q5. For the second phase Q4 turns off and Q3 turns on, pushing C2 above supply (charge is dumped into the gate). Q3 also charges C1. On the third phase Q2 turns off and Q1 turns on, pushing the common point of the two capacitors above supply. Some of the charge in C1 makes its way to the gate. The sequence is repeated by turning Q2 and Q4 back on, and Q1 and Q3 off.

In a low-side application operating on a 12 to 15V supply, the MOSFET is fully enhanced by the action of Q5 alone. On supplies of more than approximately 14V, current flows directly from Q5 through the zener diode to ground. To prevent excessive current flow, the MIC5012 supply should be limited to 15V in low-side applications.

The action of Q5 makes the MIC5012 operate quickly in low-side applications. In high-side applications Q5 precharges the MOSFET gate to supply, leaving the charge pump to carry the gate up to full enhancement 10V above supply. Bootstrapped high-side drivers are as fast as low-side drivers since the chip supply is boosted well above the drain at turn-on.

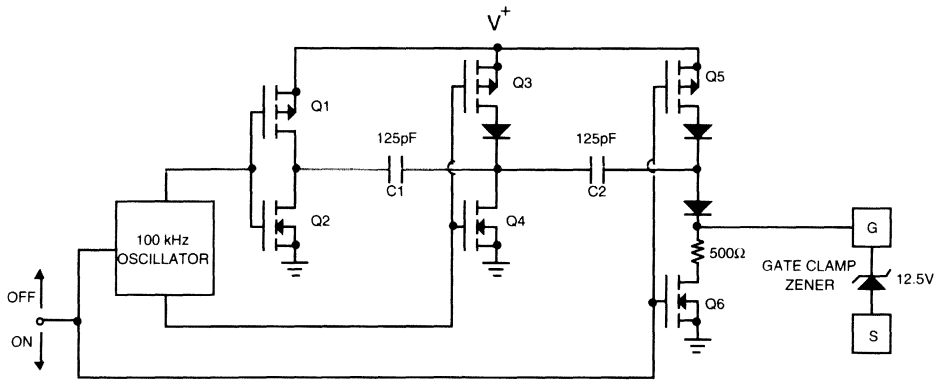


Figure 10. Gate Control Circuit Detail

MIC5013

Protected 8-pin Power MOSFET Predriver

General Description

The MIC5013 is an 8-pin MOSFET predriver with over-current shutdown and a fault flag. It is designed to drive the gate of an N-channel power MOSFET above the supply rail high-side power switch applications. The MIC5013 is compatible with standard or current-sensing power MOSFETs in both high- and low-side driver topologies.

The MIC5013 charges a 1nF load in 60µs typical and protects the MOSFET from over-current conditions. The current sense trip point is fully programmable and a dynamic threshold allows high in-rush current loads to be started. A fault pin indicates when the MIC5013 has turned off the FET due to excessive current.

Other members of the Micrel predriver family include the MIC5010 full-featured predriver, MIC5011 minimum parts count predriver, and MIC5012 dual predriver.

Features

- 7V to 32V operation
- Less than 1µA standby current in the "OFF" state
- MIL-STD-883 Method 5004/5005 version available
- Available in small outline SOIC packages
- Internal charge pump to drive the gate of an N-channel power FET above supply
- Internal zener clamp for gate protection
- 60µs typical turn-on time to 50% gate overdrive
- Programmable over-current sensing
- Dynamic current threshold for high in-rush loads
- Fault output pin indicates current faults
- Implements high- or low-side switches

Applications

- Lamp drivers
- Relay and solenoid drivers
- Heater switching
- Power bus switching
- Motion control

Typical Application

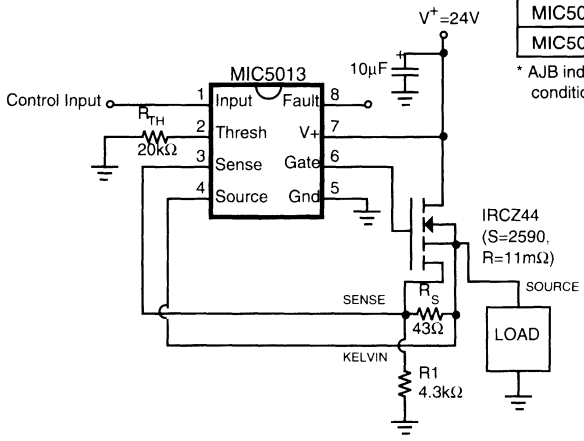


Figure 1. High-Side Driver with Current-Sensing MOSFET

Ordering Information

Part Number	Temperature Range	Package
MIC5013BN	–40°C to +85°C	8-pin Plastic DIP
MIC5013BJ	–40°C to +85°C	8-pin Ceramic DIP
MIC5013BM	–40°C to +85°C	8-pin SOIC
MIC5013AJ	–55°C to +125°C	8-pin Ceramic DIP
MIC5013AJB*	–55°C to +125°C	8-pin Ceramic DIP

* AJB indicates units screened to MIL-STD 883, Method 5004, condition B, and burned-in for 1-week.

$$R_S = \frac{SR(V_{TRIP} + 100mV)}{R\,I_L - (V_{TRIP} + 100mV)}$$

$$R1 = \frac{V^+ SRR_S}{100mV\,(SR + R_S)}$$

$$R_{TH} = \frac{2200}{V_{TRIP}} - 1000$$

For this example:

I_L =30A (trip current)

V_{TRIP}=100mV

Note: The MIC5013 is ESD sensitive.

Absolute Maximum Ratings (Note 1, 2)

Input Voltage, Pin 1	–10 to V+
Threshold Voltage, Pin 2	–0.5 to +5V
Sense Voltage, Pin 3	–10V to V+
Source Voltage, Pin 4	–10V to V+
Current into Pin 4	50mA
Gate Voltage, Pin 6	–1V to 50V
Supply Voltage (V+), Pin 7	–0.5V to 36V
Fault Output Current, Pin 8	–1mA to +1mA
Junction Temperature	150°C

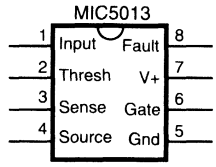
Operating Ratings (Notes 1, 2)

Power Dissipation	1.25W
θ_{JA} (Plastic DIP)	100°C/W
θ_{JA} (Ceramic DIP)	125°C/W
θ_{JA} (SOIC)	170°C/W
Ambient Temperature: B version	–40°C to +85°C
Ambient Temperature: A version	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C
Supply Voltage (V+), Pin 7	7V to 32V high side 7V to 15V low side

Pin Description (Refer to Figures 1 and 2)

Pin Number	Pin Name	Pin Function
1	Input	Resets current sense latch and turns on power MOSFET when taken above threshold (3.5V typical). Pin 1 requires <1µA to switch.
2	Threshold	Sets current sense trip voltage according to: $V_{TRIP} = \frac{2200}{R_{TH} + 1000}$ where R_{TH} to ground is 3.3k to 20kΩ. Adding capacitor C_{TH} increases the trip voltage at turn-on to 2V. Use C_{TH} =10µF for a 10ms turn-on time constant.
3	Sense	The sense pin causes the current sense to trip when V_{SENSE} is V_{TRIP} above V_{SOURCE}. Pin 3 is used in conjunction with a current shunt in the source of a 3 lead FET or a resistor R_S in the sense lead of a current sensing FET.
4	Source	Reference for the current sense voltage on pin 3 and return for the gate clamp zener. Connect to the load side of current shunt or kelvin lead of current sensing FET. Pins 3 and 4 can safely swing to –10V when turning off inductive loads.
5	Ground	
6	Gate	Drives and clamps the gate of the power FET. Pin 6 will be clamped to approximately –0.7V by an internal diode when turning off inductive loads.
7	V+	Supply pin; must be decoupled to isolate from large transients caused by the power FET drain. 10µF is recommended close to pins 7 and 5.
8	Fault	Outputs status of protection circuit when pin 1 is high. Fault low indicates normal operation; fault high indicates current sense tripped.

Pin Configuration



Electrical Characteristics (Note 3) Test circuit. T_A = –55°C to +125°C, V^+ = 15V, all switches open, unless otherwise specified.

Parameter	Conditions			Min	Typical	Max	Units
Supply Current, I_7	V^+ = 32V	V_{IN} = 0V, S4 closed			0.1	10	µA
		$V_{IN} = V_S$ = 32V			8	20	mA
Logic Input Voltage, V_{IN}	V^+ = 4.75V	Adjust V_{IN} for V_{GATE} low				2	V
		Adjust V_{IN} for V_{GATE} high		4.5			V
	V^+ =15V	Adjust V_{IN} for V_{GATE} low		5.0			V
Logic Input Current, I_1	V+ = 32V	V_{IN} = 0V		–1			µA
		V_{IN} = 32V				1	µA
Input Capacitance	Pin 1				5		pF
Gate Drive, V_{GATE}	S1, S2 closed,	V^+ = 7V, I_6 = 0		13	15		V
	V_S = V+, V_{IN} = 5V	V^+ = 15V, I_6 = 100 µA		24	27		V
Zener Clamp,	S2 closed, V_{IN} = 5V	V+ = 15V, V_S = 15V		11	12.5	15	V
$V_{GATE} - V_{SOURCE}$		V^+ = 32V, V_S = 32V		11	13	16	V
Gate Turn-on Time, t_{ON} (Note 4)	V_{IN} switched from 0 to 5V; measure time for V_{GATE} to reach 20V				60	200	µs
Gate Turn-off Time, t_{OFF}	V_{IN} switched from 5 to 0V; measure time for V_{GATE} to reach 1V				4	10	µs
Threshold Bias Voltage, V_2	I_2 = 200 µA			1.7	2	2.2	V
Current Sense Trip Voltage,	S2 closed, V_{IN} = 5V,	V^+ = 7V,	S4 closed	75	105	135	mV
$V_{SENSE} - V_{SOURCE}$	Increase I_3	I_2 = 100 µA	V_S = 4.9V	70	100	130	mV
		V^+ = 15V	S4 closed	150	210	270	mV
		I_2 = 200 µA	V_S = 11.8V	140	200	260	mV
		V^+ = 32V	V_S = 0V	360	520	680	mV
		I_2 = 500 µA	V_S = 25.5V	350	500	650	mV
Peak Current Trip Voltage, $V_{SENSE} - V_{SOURCE}$	S3, S4 closed, V^+ = 15V, V_{IN} = 5V			1.6	2.1		V
Fault Output Voltage, V_{14}	V_{IN} = 0V, I_8 = –100 µA				0.4	1	V
	V_{IN} = 5V, I_8 = 100 µA, current sense tripped			14	14.6		V

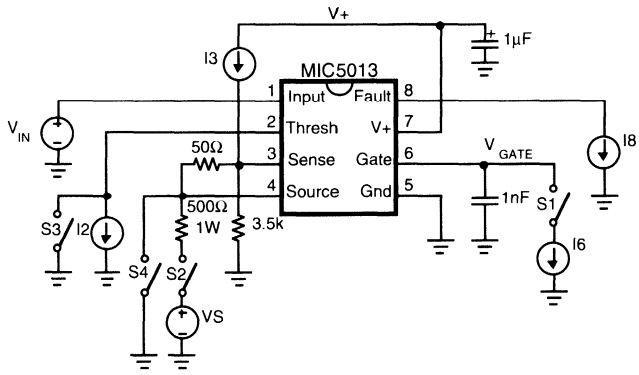
Note 1 **Absolute Maximum Ratings** indicate limits beyond which damage to the device may occur. Electrical specifications do not apply when operating the device beyond its specified **Operating Ratings**.

Note 2 The MIC5010 is ESD sensitive.

Note 3 Minimum and maximum **Electrical Characteristics** are 100% tested at T_A = 25°C and T_A = 85°C, and 100% guaranteed over the entire range. Typicals are characterized at 25°C and represent the most likely parametric norm.

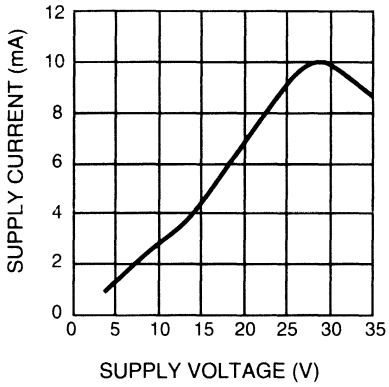
Note 4 Test conditions reflect worst case high-side driver performance. Low-side and bootstrapped topologies are significantly faster—see **Applications Information**.

Test Circuit

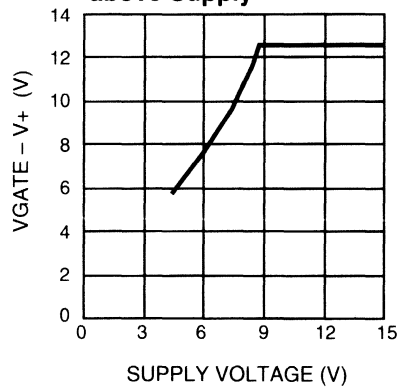


Typical Characteristics

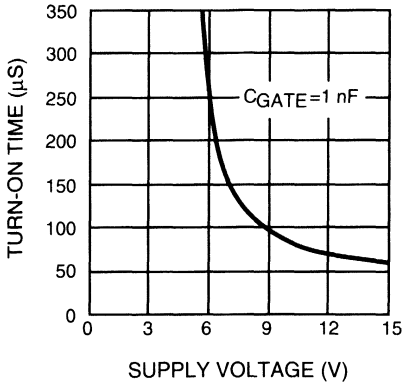
Supply Current



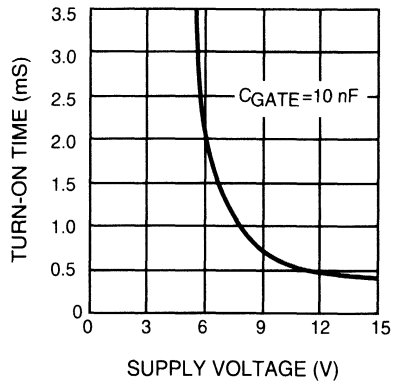
DC Gate Voltage above Supply



High-side Turn-on Time*



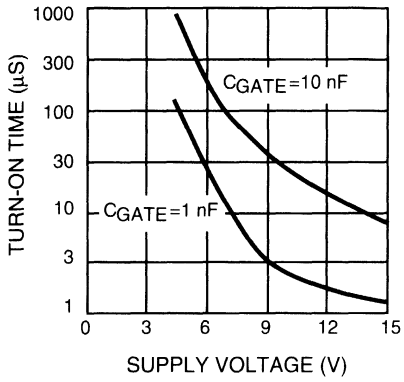
High-side Turn-on Time*



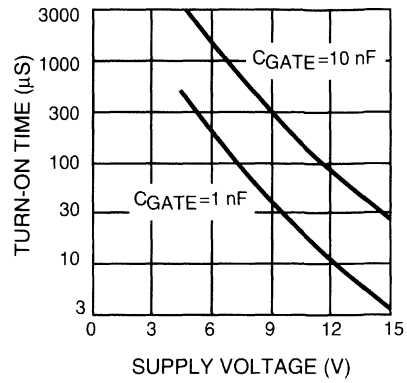
* Time for gate to reach $V^+ + 5V$ in test circuit with $VS = V^+ - 5V$ (prevents gate clamp from interfering with measurement).

Typical Characteristics (Continued)

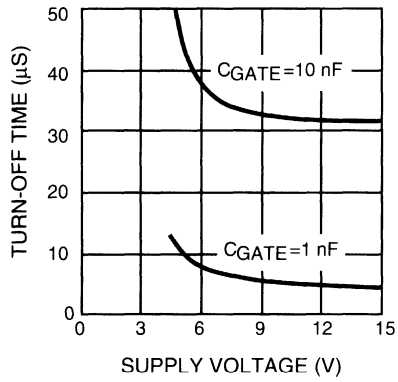
Low-side Turn-on Time for Gate = 5V



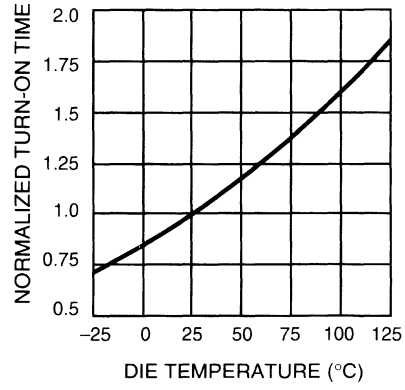
Low-side Turn-on Time for Gate = 10V



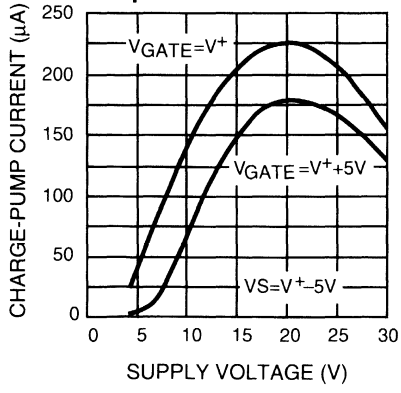
Turn-off Time



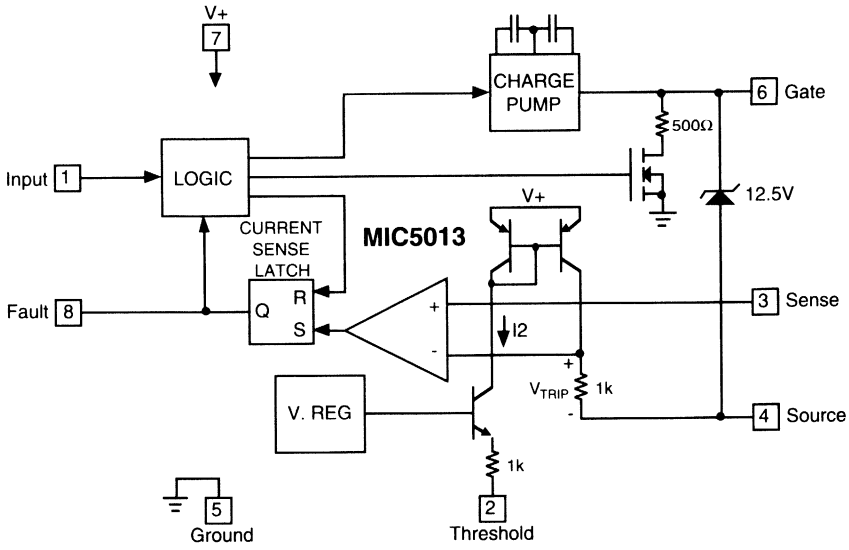
Turn-on Time



Charge Pump Output Current



Block Diagram



Applications Information

Functional Description (refer to **block diagram**)

The various MIC5013 functions are controlled via a logic block connected to the input pin 1. When the input is low, all functions are turned off for low standby current and the gate of the power MOSFET is also held low through 500Ω to an N-channel switch. When the input is taken above the turn-on threshold (3.5V typical), the N-channel switch turns off and the charge pump is turned on to charge the gate of the power FET. A bandgap type voltage regulator is also turned on which biases the current sense circuitry.

The charge pump incorporates a 100kHz oscillator and on-chip pump capacitors capable of charging 1nF to 5V above supply in 60µs typical. The charge pump is capable of pumping the gate up to over twice the supply voltage. For this reason, a zener clamp (12.5V typical) is provided between the gate pin 6 and source pin 4 to prevent exceeding the V_{GS} rating of the MOSFET at high supplies.

The current sense operates by comparing the sense voltage at pin 3 to an offset version of the source voltage at pin 4. Current I2 flowing in threshold pin 2 is mirrored and returned to the source via a 1kΩ resistor to set the offset, or trip voltage. When ($V_{SENSE} - V_{SOURCE}$) exceeds V_{TRIP}, the current sense trips and sets the current sense latch to turn off the power FET. An integrating comparator is used to reduce sensitivity to spikes on pin 3. The latch is reset to turn the FET back on by "recycling" the input pin 1 low and then high again.

A resistor R_{TH} from pin 2 to ground sets I2, and hence V_{TRIP}. An additional capacitor C_{TH} from pin 2 to ground creates a higher trip voltage at turn-on, which is necessary to prevent high in-rush current loads such as lamps or capacitors from false-tripping the current sense.

When the current sense has tripped, the fault pin 8 will be high as long as the input pin 1 remains high. However, when the input is low the fault pin will also be low.

Construction Hints

High current pulse circuits demand equipment and assembly techniques that are more stringent than normal low current lab practices. The following are the sources of pitfalls most often encountered during prototyping: Supplies: many bench power supplies have poor transient response. Circuits that are being pulse tested, or those that operate by pulse-width modulation will produce strange results when used with a supply that has poor ripple rejection, or a peaked transient response. Monitor the power supply voltage that appears at the drain of a high-side driver (or the supply side of the load in a low-side driver) with an oscilloscope. It is not uncommon to find bench power supplies in the 1kW class that overshoot or undershoot by as much as 50% when pulse loaded. Not only will the load current and voltage measurements be affected, but it is possible to over-stress various components—especially electrolytic capacitors—with possibly catastrophic results. A 10µF supply bypass capacitor at the chip is recommended.

Residual Resistances: Resistances in circuit connections may also cause confusing results. For example, a circuit may employ a 50mΩ power MOSFET for low drop, but careless construction techniques could easily add 50 to 100mΩ resistance. Do not use a socket for the MOSFET. If the MOSFET is a TO-220 type package, make high-current drain connections to the tab. Wiring losses have a profound effect on high-current circuits. A floating millivoltmeter can identify connections that are contributing excess drop under load.

Applications Information (Continued)

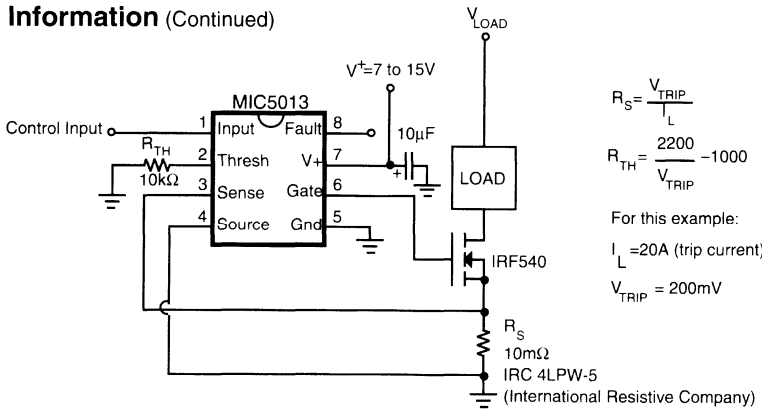


Figure 2. Low-Side Driver with Current Shunt

Circuit Topologies

The MIC5013 is suited for use in high- or low-side driver applications with over-current protection for both current-sensing and standard MOSFETs. In addition, the MIC5013 works well in applications where, for faster switching times, the supply is bootstrapped from the MOSFET source output. Low voltage, high-side drivers (such as shown in the Test Circuit) are the slowest; their speed is reflected in the gate turn-on time specifications. The fastest drivers are the low-side and bootstrapped high-side types. Load current switching times are often much faster than the time to full gate enhancement, depending on the circuit type, the MOSFET, and the load. Turn-off times are essentially the same for all circuits (less than 10µs to V_{GS} = 1V). The choice of one topology over another is based on a combination of considerations including speed, voltage, and desired system characteristics. Each topology is described in this section. Note that I_L, as used in the design equations, is the load current that just trips the over-current comparator.

Low-Side Driver with Current Shunt (Figure 2). The over-current comparator monitors RS and trips if $I_L \times R_S$ exceeds V_{TRIP}. R is selected to produce the desired trip voltage.

As a guideline, keep V_{TRIP} within the limits of 100mV and 500mV (R_{TH} = 3.3kΩ to 20kΩ). Thresholds at the high end offer the best noise immunity, but also compromise switch drop (especially in low voltage applications) and power dissipation.

The trip current is set higher than the maximum expected load current—typically twice that value. Trip point accuracy is a function of resistor tolerances, comparator offset (only a few millivolts), and threshold bias voltage (V2). The values shown in Figure 2 are designed for a trip current of 20 amperes. It is important to ground pin 4 at the current shunt R_S, to eliminate the effects of ground resistance.

A key advantage of the low-side topology is that the load supply is limited only by the MOSFET BVDSS rating. Clamping may be required to protect the MOSFET drain terminal from inductive switching transients. The MIC5013

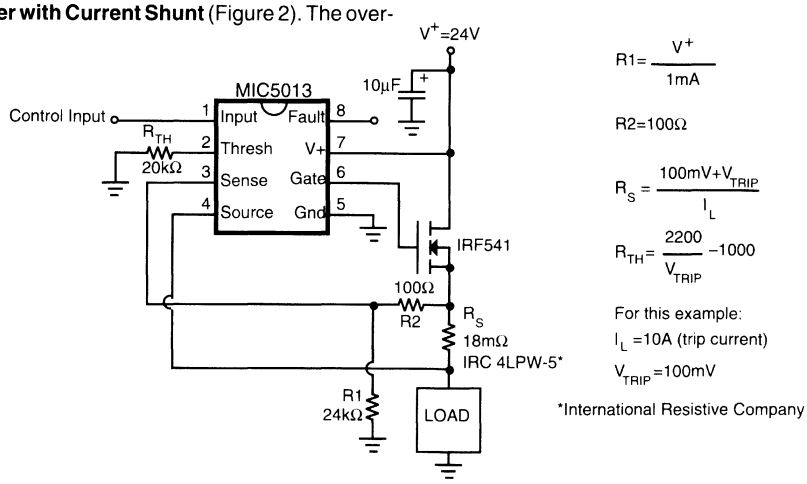


Figure 3. High-Side Driver with Current Shunt

Applications Information (Continued)

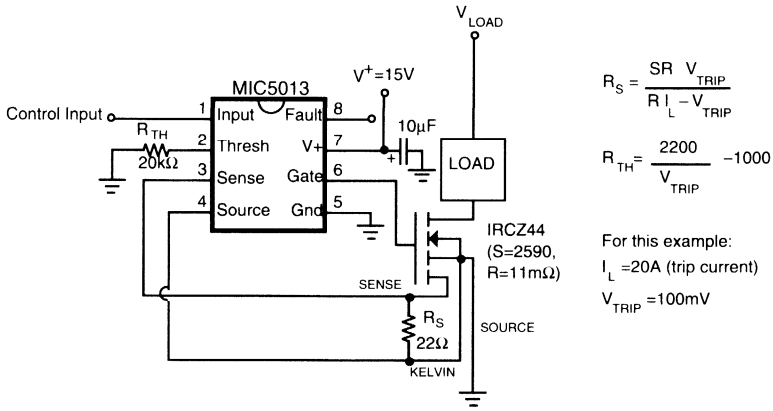


Figure 4. Low-Side Driver with Current-Sensing MOSFET

supply should be limited to 15V in low-side topologies; otherwise, a large current will be forced through the gate clamp zener.

Low-side drivers constructed with the MIC501X family are also fast; the MOSFET gate is driven to near supply immediately when commanded ON. Typical circuits achieve 10V enhancement in 10µs or less on a 12 to 15V supply.

High-Side Driver with Current Shunt (Figure 3). The comparator input pins (source and sense) float with the current sensing resistor (R_S) on top of the load. R1 and R2 add a small, additional potential to V_{TRIP} to prevent false-triggering of the over-current shutdown circuit with open or inductive loads. R1 is sized for a current flow of 1mA, while R2 contributes a drop of 100mV. The shunt voltage should be 200 to 500mV at the trip point. The example of Figure 3 gives a 10A trip current when the output is near supply. The trip point is somewhat reduced when the output is at ground as the voltage drop across R1 (and therefore R2) is zero.

High-side drivers implemented with MIC5013 predrivers are self-protected against inductive switching transients. During turn-off an inductive load will force the MOSFET source 5V or more below ground, while the predriver holds the gate at ground potential. The MOSFET is forced into conduction, and it dissipates the energy stored in the load inductance. The MIC5013 source and sense pins (3 and 4) are designed to withstand this negative excursion without damage. External clamp diodes are unnecessary.

Current Shunts (R_S). Low-valued resistors are necessary for use at R_S.Values for R_S range from 5 to 50mΩ, at 2 to 10W. Worthy of special mention are Kelvin-sensed, "four-terminal" units supplied by a number of manufacturers† (see next page). Kelvin-sensed resistors eliminate errors caused by lead and terminal resistances, and simplify product assembly. 10% tolerance is normally adequate, and with shunt potentials of 200mV thermocouple effects are insignificant. Temperature coefficient is important; a linear, 500 ppm/°C change will contribute as much as 10% shift in the over-current trip point. Most power resistors designed for current shunt service drift less than 100 ppm/°C.

Low-Side Driver with Current Sensing MOSFET (Figure 4). Several manufacturers now supply power MOSFETs in which a small sampling of the total load current is diverted to a "sense" pin. One additional pin, called "Kelvin source," is included to eliminate the effects of resistance in the source bond wires. Current-sensing MOSFETs are specified with a sensing ratio "S" which describes the relationship between the on-resistance of the sense connection and the body resistance "R" of the main source pin. Current sensing MOSFETs eliminate the current shunt required by standard MOSFETs.

The design equations for a low-side driver using a current sensing MOSFET are shown in Figure 4. "S" is specified on the MOSFET's datasheet, and "R" must be measured or estimated. V_{TRIP} must be less than $R \times I_L$, or else R_S will become negative. Substituting a MOSFET with higher on-resistance, or reducing V_{TRIP} fixes this problem. V_{TRIP} = 100 to 200mV is suggested. Although the load supply is limited only by MOSFET ratings, the MIC5013 supply should be limited to 15V to prevent damage to the gate clamp zener. Output clamping is necessary for inductive loads.

"R" is the body resistance of the MOSFET, excluding bond resistances. $R_{DS(ON)}$ as specified on MOSFET data sheets

† Suppliers of Kelvin-sensed power resistors:
Dale Electronics, Inc., 2064 12th Ave., Columbus, NE 68601. Tel: (402) 564-3131
International Resistive Co., P.O. Box 1860, Boone, NC 28607-1860. Tel: (704) 264-8861
Kelvin, 14724 Ventura Blvd., Ste. 1003, Sherman Oaks, CA 91403-3501. Tel: (818) 990-1192
RCD Components, Inc., 520 E. Industrial Pk. Dr., Manchester, NH 03103. Tel: (603) 669-0054
Ultronix, Inc., P.O. Box 1090, Grand Junction, CO 81502. Tel: (303) 242-0810

Applications Information (Continued)

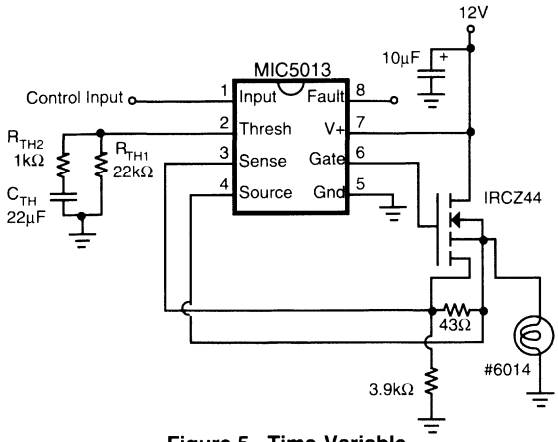


Figure 5. Time-Variable Trip Threshold

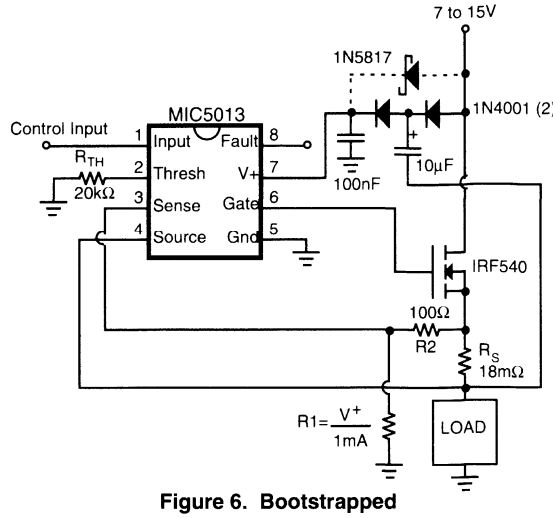


Figure 6. Bootstrapped High-Side Driver

includes bond resistances. A Kelvin-connected ohmmeter (using TAB and SOURCE for forcing, and SENSE and KELVIN for sensing) is the best method of evaluating "R." Alternatively, "R" can be estimated for large MOSFETs ($R_{DS(ON)} \leq 100m\Omega$) by simply halving the stated $R_{DS(ON)}$, or by subtracting 20 to 50mΩ from the stated $R_{DS(ON)}$ for smaller MOSFETs.

High-Side Driver with Current Sensing MOSFET (Figure 5). The design starts by determining the value of "S" and "R" for the MOSFET (use the guidelines described for the low-side version). Let V_{TRIP} = 100mV, and calculate R_S for a desired trip current. Next calculate R_{TH} and R1. The trip point is somewhat reduced when the output is at ground as the voltage drop across R1 is zero. No clamping is required for inductive loads, but may be added to reduce power dissipation in the MOSFET.

Typical Applications

Start-up into a Dead Short. If the MIC5013 attempts to turn on a MOSFET when the load is shorted, a very high current flows. The over-current shutdown will protect the MOSFET, but only after a time delay of 5 to 10µs. The MOSFET must be capable of handling the overload; consult the device's SOA curve. If a short circuit causes the MOSFET to exceed its 10µs SOA, a small inductance in series with the source can help limit di/dt to control the peak current during the 5 to 10µs delay.

When testing short-circuit behavior, use a current probe rated for both the peak current and the high di/dt.

The over-current shutdown delay varies with comparator overdrive, owing to noise filtering in the comparator. A delay of up to 100µs can be observed at the threshold of shutdown. A 20% overdrive reduces the delay to near minimum.

Incandescent Lamps. The cold filament of an incandescent lamp exhibits less than one-tenth as much resistance as when the filament is hot. The initial turn-on current of a #6014 lamp is about 70A, tapering to 4.4A after a few hundred milliseconds. It is unwise to set the over-current trip point to 70A to accommodate such a load. A "resistive" short that draws less than 70A could destroy the MOSFET by allowing sustained, excessive dissipation. If the over-current trip point is set to less than 70A, the MIC5013 will not start a cold filament. The solution is to start the lamp with a high trip point, but reduce this to a reasonable value after the lamp is hot.

The MIC5013 over-current shutdown circuit is designed to handle this situation by varying the trip point with time (see Figure 5). R_{TH1} functions in the conventional manner, providing a current limit of approximately twice that required by the lamp. R_{TH2} acts to increase the current limit at turn-on to approximately 10 times the steady-state lamp current. The high initial trip point decays away according to a 20ms time constant contributed by C_{TH}. R_{TH2} could be eliminated with C_{TH} working against the internal 1kΩ resistor, but this results in a very high over-current threshold. As a rule of thumb design the over-current circuitry in the conventional manner, then add the R_{TH2}/C_{TH} network to allow for lamp start-up. Let $R_{TH2} = (R_{TH1} \div 10) - 1k\Omega$, and choose a capacitor that provides the desired time constant working against R_{TH2} and the internal 1kΩ resistor.

When the MIC5013 is turned off, the threshold pin (2) appears as an open circuit, and C_{TH} is discharged through R_{TH1} and R_{TH2}. This is much slower than the turn-on time constant, and it simulates the thermal response of the filament. If the lamp is pulse-width modulated, the current limit will be reduced by the residual charge left in C_{TH}.

Modifying Switching Times. Do not add external capacitors to the gate to slow down the switching time. Add a resistor (1kΩ to 51kΩ) in series with the gate of the MOSFET to achieve this result.

Bootstrapped High-Side Driver (Figure 6). The speed of a high-side driver can be increased to better than 10µs by bootstrapping the supply off of the MOSFET source. This topology can be used where the load is pulse-width modu-

Applications Information (Continued)

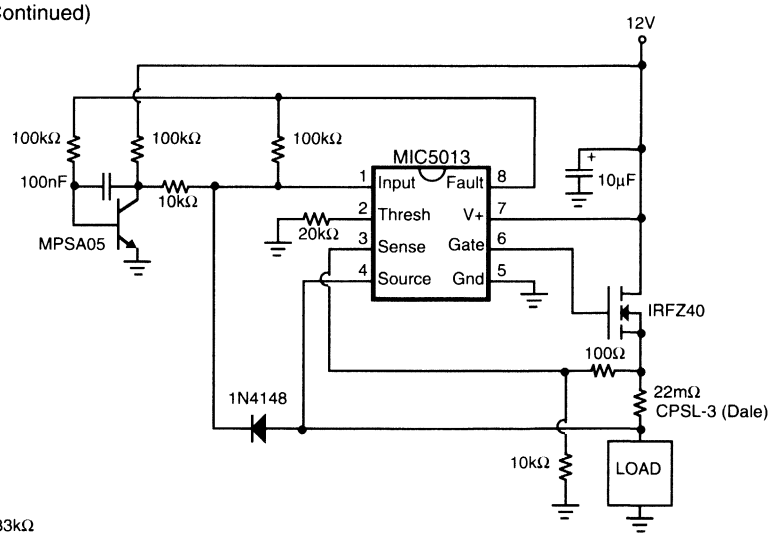


Figure 7. 10-Ampere Electronic Circuit Breaker

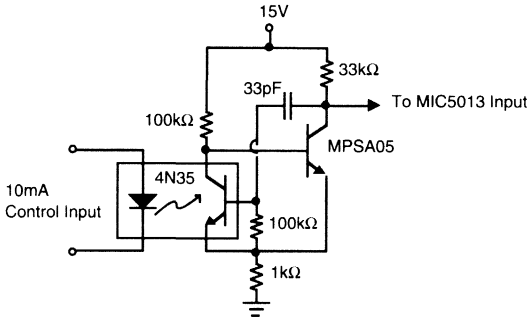


Figure 8. Improved Opto-Isolator Performance

lated (100Hz to 20kHz), or where it is energized for only a short period of time (≤25ms). If the load is left energized for a long period of time (>25ms), the bootstrap capacitor will discharge and the MIC5013 supply pin will fall to V+ = V_{DD} −1.4. Under this condition pins 3 and 4 will be held above V+ and may false trigger the over-current circuit. A larger capacitor will lengthen the maximum "on" time; 1000µF will hold the circuit up for 2.5 seconds, but requires more charge time when the circuit is turned off. The optional Schottky barrier diode improves turn-on time on supplies of less than 10V.

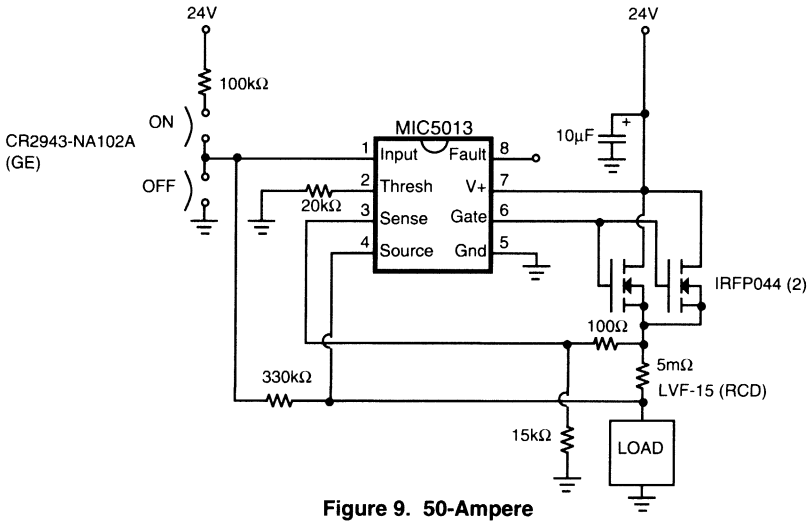


Figure 9. 50-Ampere Industrial Switch

Applications Information (Continued)

Since the supply current in the "OFF" state is only a small leakage, the 100nF bypass capacitor tends to remain charged for several seconds after the MIC5013 is turned off. In a PWM application the chip supply is actually much higher than the system supply, which improves switching time.

Electronic Circuit Breaker (Figure 7). The MIC5013 forms the basis of a high-performance, fast-acting circuit breaker. By adding feedback from FAULT to INPUT the breaker can be made to automatically reset. If an over-current condition occurs, the circuit breaker shuts off. The breaker tests the load every 18ms until the short is removed, at which time the circuit latches ON. No reset button is necessary.

Opto-Isolated Interface (Figure 8). Although the MIC5013 has no special input slew rate requirement, the lethargic transitions provided by an opto-isolator may cause oscillations on the rise and fall of the output. The circuit shown accelerates the input transitions from a 4N35 opto-isolator by adding hysteresis. Opto-isolators are used where the control circuitry cannot share a common ground with the MIC5013 and high-current power supply, or where the control circuitry is located remotely. This implementation is intrinsically safe; if the control line is severed the MIC5013 will turn OFF.

Fault-Protected Industrial Switch (Figure 9). The most common manual control for industrial loads is a push button on/off switch. The "on" button is physically arranged in a recess so that in a panic situation the "off" button, which extends out from the control box, is more easily pressed. This circuit is compatible with control boxes such as the CR2943 series (GE). The circuit is configured so that if both switches close simultaneously, the "off" button has precedence. If there is a fault condition the circuit will latch off, and it can be reset by pushing the "ON" button.

This application also illustrates how two (or more) MOSFETs can be paralleled. This reduces the switch drop, and distributes the switch dissipation into multiple packages.

High-Voltage Bootstrap (Figure 10). Although the MIC5013 is limited to operation on 7 to 32V supplies, a floating bootstrap arrangement can be used to build a high-side switch that operates on much higher voltages. The MIC5013 and MOSFET are configured as a low-side driver, but the load is connected in series with ground. The high speed normally associated with low-side drivers is retained in this circuit.

Power for the MIC5013 is supplied by a charge pump. A 20kHz square wave (15Vp-p) drives the pump capacitor and delivers current to a 100µF storage capacitor. A zener diode limits the supply to 18V. When the MIC5013 is off, power is supplied by a diode connected to a 15V supply. The circuit of Figure 8 is put to good use as a barrier between low voltage control circuitry and the 90V motor supply.

Half-Bridge Motor Driver (Figure 11). Closed loop control of motor speed requires a half-bridge driver. This topology presents an extra challenge since the two output devices should not cross conduct (shoot-through) when switching. Cross conduction increases output device power dissipation and, in the case of the MIC5013, could trip the over-current comparator. Speed is also important, since PWM control requires the outputs to switch in the 2 to 20kHz range.

The circuit of Figure 11 utilizes fast configurations for both the top- and bottom-side drivers. Delay networks at each input provide a 2 to 3µs dead time effectively eliminating cross conduction. Both the top- and bottom-side drivers are protected, so the output can be shorted to either rail without damage.

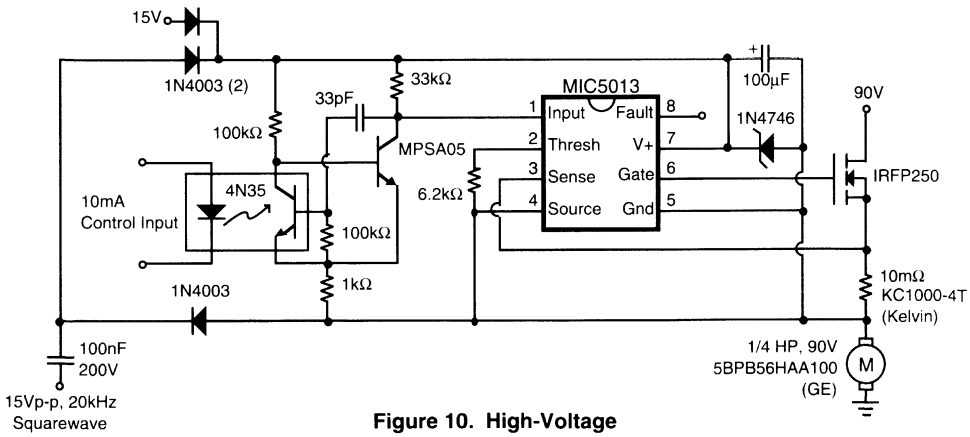


Figure 10. High-Voltage Bootstrapped Driver

Applications Information (Continued)

The top-side driver is based on the bootstrapped circuit of Figure 6, and cannot be switched on indefinitely. The bootstrap capacitor (1µF) relies on being pulled to ground by the bottom-side output to recharge. This limits the maximum duty cycle to slightly less than 100%.

Two of these circuits can be connected together to form an H-bridge. If the H-bridge is used for locked antiphase control, no special considerations are necessary. In the case of sign/magnitude control, the "sign" leg of the H-bridge should be held low (PWM input held low) while the other leg is driven by the magnitude signal.

If current feedback is required for torque control, it is available in chopped form at the bottom-side driver's 22 mΩ current-sensing resistor.

Time-Delay Relay (Figure 12). The MIC5013 forms the basis of a simple time-delay relay. As shown, the delay commences when power is applied, but the 100 kΩ/1N4148 could be independently driven from an external source such as a switch or another high-side driver to give a delay relative to some other event in the system.

Hysteresis has been added to guarantee clean switching at turn-on. Note that an over-current condition latches the relay in a safe, OFF condition. Operation is restored by either cycling power or by momentarily shorting pin 1 to ground.

Motor Driver with Stall Shutdown (Figure 13). Tachometer feedback can be used to shut down a motor driver circuit when a stall condition occurs. The control switch is a 3-way type; the "START" position is momentary and forces the driver ON. When released, the switch returns to the "RUN" position, and the tachometer's output is used to hold the MIC5013 input ON. If the motor slows down, the tach output is reduced, and the MIC5013 switches OFF. Resistor "R" sets the shutdown threshold. If the output current exceeds 30A, the MIC5013 shuts down and remains in that condition until the momentary "RESET" button is pushed. Control is then returned to the START/RUN/STOP switch.

2

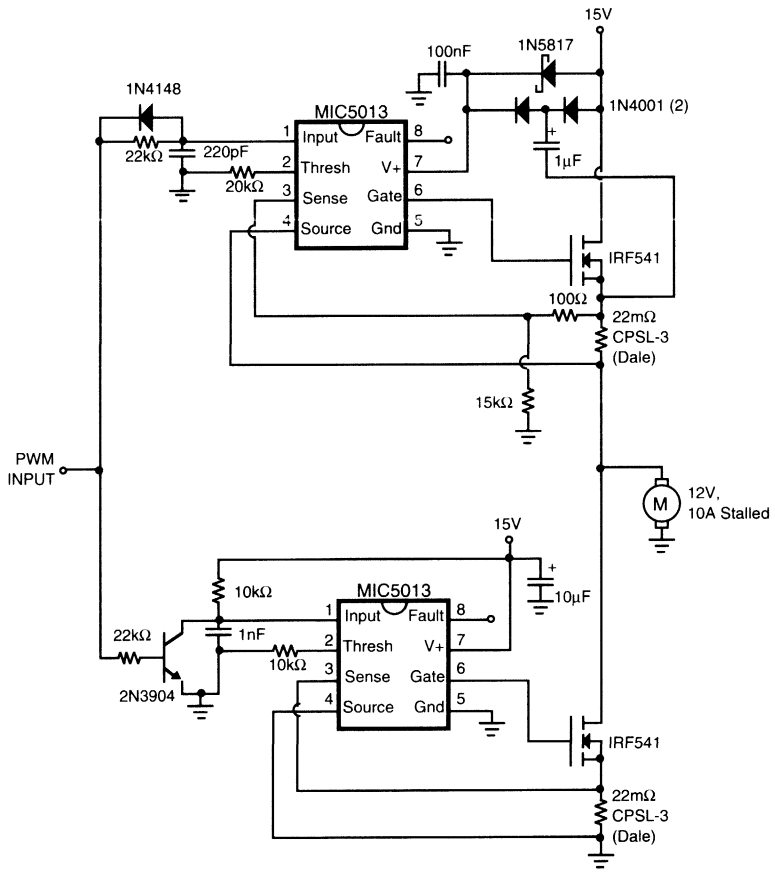


Figure 11. Half-Bridge Motor Driver

Applications Information (Continued)

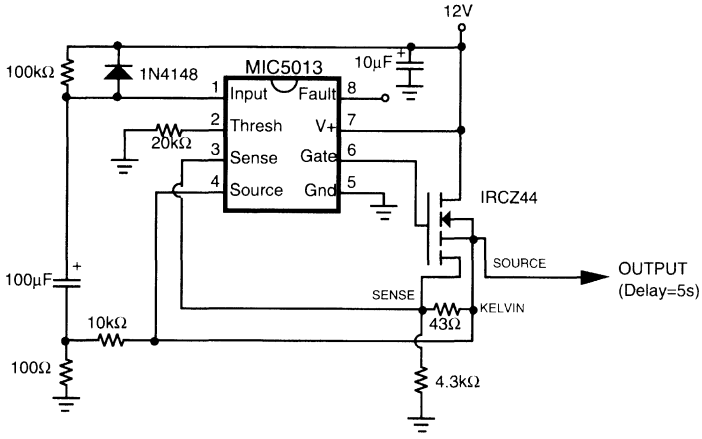


Figure 12. Time-Delay Relay with 30A Over-Current Protection

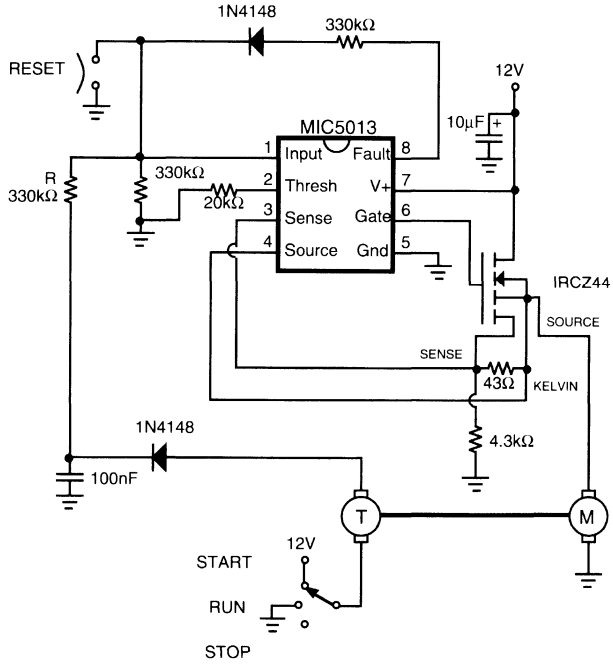


Figure 13. Motor Stall Shutdown

Applications Information (Continued)

Gate Control Circuit

When applying the MIC5010, it is helpful to understand the operation of the gate control circuitry (see Figure 14). The gate circuitry can be divided into two sections: 1) charge pump (oscillator, Q1-Q5, and the capacitors) and 2) gate turn-off switch (Q6).

When the MIC5010 is in the OFF state, the oscillator is turned off, thereby disabling the charge pump. Q5 is also turned off, and Q6 is turned on. Q6 holds the gate pin (G) at ground potential which effectively turns the external MOSFET off.

Q6 is turned off when the MIC5010 is commanded on. Q5 pulls the gate up to supply (through 2 diodes). Next, the charge pump begins supplying current to the gate. The gate accepts charge until the gate-source voltage reaches 12.5V and is clamped by the zener diode.

A 2-output, three-phase clock switches Q1-Q4, providing a quasi-tripling action. During the initial phase Q4 and Q2 are ON. C1 is discharged, and C2 is charged to supply through Q5. For the second phase Q4 turns off and Q3 turns on, pushing pin C2 above supply (charge is dumped into the gate). Q3 also charges C1. On the third phase Q2 turns off and Q1 turns on, pushing the common point of the two capacitors above supply. Some of the charge in C1 makes its way to the gate. The sequence is repeated by turning Q2 and Q4 back on, and Q1 and Q3 off.

In a low-side application operating on a 12 to 15V supply, the MOSFET is fully enhanced by the action of Q5 alone. On supplies of more than approximately 14V, current flows directly from Q5 through the zener diode to ground. To prevent excessive current flow, the MIC5010 supply should be limited to 15V in low-side applications.

The action of Q5 makes the MIC5010 operate quickly in low-side applications. In high-side applications Q5 precharges the MOSFET gate to supply, leaving the charge pump to carry the gate up to full enhancement 10V above supply. Bootstrapped high-side drivers are as fast as low-side drivers since the chip supply is boosted well above the drain at turn-on.

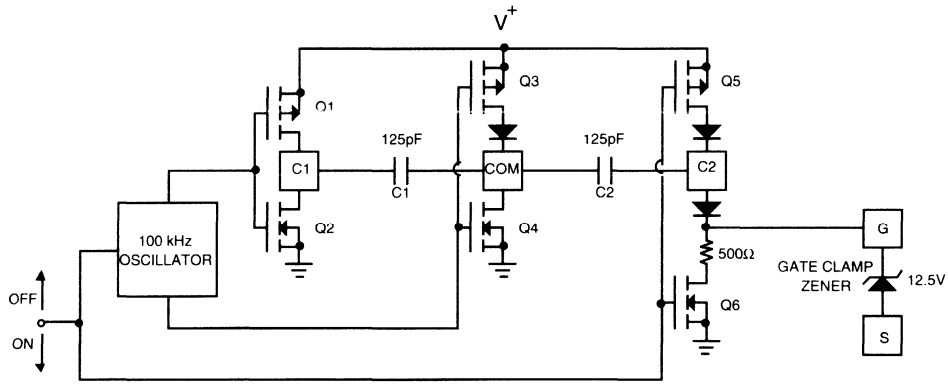


Figure 14. Gate Control Circuit Detail

MIC5014/5015

Low Cost MOSFET Predrivers

General Description

The MIC5014/5015 MOSFET predrivers are members of the MIC501x family. These versatile drivers are designed to provide gate enhancement above the positive supply for an N-channel FET used in high or low side switching applications.

The MIC5014/5015 devices have many improvements in addition to the ease of use and versatility of the earlier members of the MIC5010 family. Operation down to 2.75V allows the MIC5014/5015 to drive standard or logic level FETs in 2.75 to 5V low side applications by boosting the gate voltage above the positive supply. This feature makes these devices ideally suited for laptop/notebook computer applications.

The MIC5014/5015 devices are considerably more rugged than their predecessors, having both "load dump" and "reverse battery" capability. They can handle an output swing of up to 20V below ground, which can occur when driving an inductive load. An overvoltage shutdown at 35V prevents damage due to supply excursions. These features make the MIC5014/5015 ideal for use in automotive applications.

As in the MIC5011, an internal zener clamp is provided to protect the gate of the external FET. The value of this zener clamp has been increased from 12.5V to 15V to allow more flexibility in design, and it has been upgraded to provide voltage regulation. The MIC5014 is pin to pin compatible with the MIC5011except for the optional speed-up capacitor pins, which are not connected in the MIC5014. The MIC5015 is an inverting version of the MIC5014.

Features

- 2.75V to 30V operation
- 100µA maximum supply current at V_{DD} = 5V
- 15µA typical standby current in the "off" state
- Internal charge pump to drive the gate of an N-channel power FET above supply
- Internal 15V zener clamp for gate protection
- Minimum external parts count
- Can be used to boost drive to low-side power or logic level FETs
- Implements high or low-side drivers
- Can withstand a 60V voltage transient (load dump).
- Designed to withstand having an input or output driven to 20V below the negative rail (inductive load).
- Reverse battery protected to –20V
- 1µA pull-off on the control input
- Available in inverting (MIC5015) and noninverting (MIC5014) forms.
- Overvoltage shutdown at 35V
- TTL compatible input

Applications

- Automotive motor/lamp/solenoid drive
- "Sleep-mode" battery saver switch for notebook/laptop computers
- Solenoid/solenoid–valve drive
- Heater switching
- Motion control
- Power bus switching
- Incandescent or halogen lamp driver

Typical Application

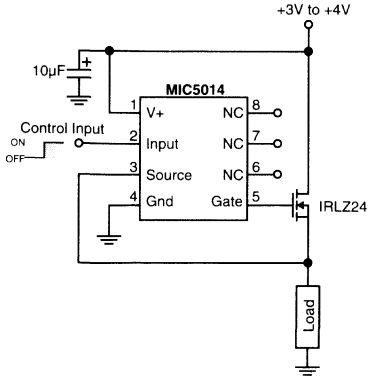


Figure 1. 3V "Sleep Mode" Switch with a Logic Level FET

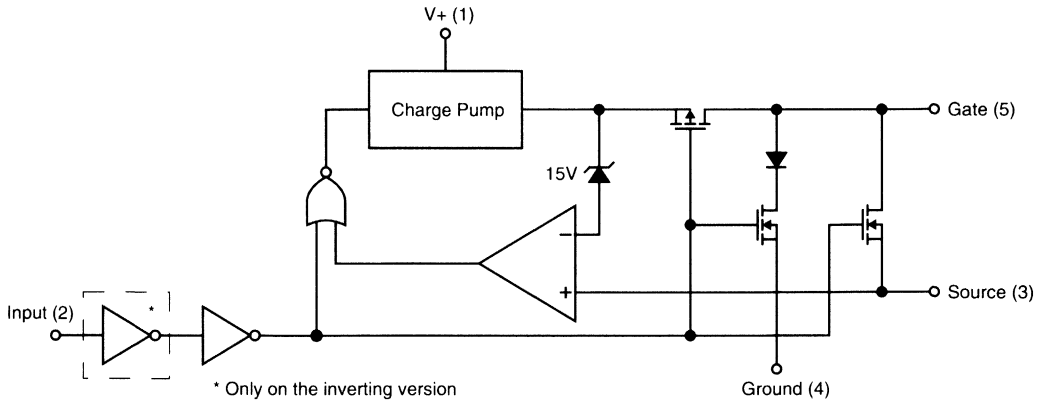
Ordering Information

Part Number*	Temperature Range	Package
MIC5014AJ	–55°C to +125°C	8-Pin CERDIP
MIC5014AJB†	–55°C to +125°C	8-Pin CERDIP
MIC5014BM	–40°C to +85°C	8-Pin SOIC
MIC5014BN	–40°C to +85°C	8-Pin Plastic DIP
MIC5015AJ	–55°C to +125°C	8-Pin CERDIP
MIC5015AJB†	–55°C to +125°C	8-Pin CERDIP
MIC5015BM	–40°C to +85°C	8-Pin SOIC
MIC5015BN	–40°C to +85°C	8-Pin Plastic DIP

* Note: MIC5014 Non-Inverting Predrivers
MIC5015 Inverting Predrivers

† AJB indicates units screened to MIL-STD 883, Method 5004, condition B, and burned-in for 1-week.

Block Diagram



Pin Description

Pin Number	Pin Name	Pin Function
1	V+	Supply pin; must be decoupled to isolate from large transients caused by the power FET drain. 10 µF is recommended close to pins 1 and 4.
2	Input	Turns on power MOSFET when taken above (or below) threshold (1.0V typical). Pin 2 requires ~ 1 µA to switch.
3	Source	Connects to source lead of power FET and is the return for the gate clamp zener. Pin 3 can safely swing to –20V when turning off inductive loads.
4	Ground	
5	Gate	Drives and clamps the gate of the power FET.
6, 7, 8	NC	No internal connection.

Absolute Maximum Ratings (Notes 1,2)

Supply Voltage (V^+), DIP pin 1	–20V to 60V
Input Voltage, DIP pins 14, 11	–20V to V^+
Source Voltage, DIP pins 2, 5	–20V to V^+
Source Current, DIP pins 2, 5	50mA
Gate Voltage, DIP pins 4, 6	–20V to 50V
Junction Temperature	150°C

Operating Ratings (Notes 1,2)

θ_{JA} (Plastic DIP)	160°C/W
θ_{JA} (Ceramic DIP)	125°C/W
θ_{JA} (SOIC)	170°C/W
Ambient Temperature: B version	–40°C to +85°C
Ambient Temperature: A version	+55°C to +125°C
Storage Temperature	–65°C to +150°C
Lead Temperature (max soldering time: 10 seconds)	260°C
Supply Voltage (V^+)	2.75V to 30V

Electrical Characteristics (Note 3) T_A = –55°C to +125°C unless otherwise specified

Parameter	Conditions		Min	Typ	Max	Units
Supply Current	V^+ = 30V	V_{IN} De-Asserted (Note 5)		10	15	µA
		V_{IN} Asserted (Note 5)		5.0	8.5	mA
	V^+ = 5V	V_{IN} De-Asserted		0.1	1	µA
		V_{IN} Asserted		60	100	
	V^+ = 3V	V_{IN} De-Asserted		0.1	1	µA
		V_{IN} Asserted		25	35	
Logic Input Voltage Threshold V_{IN}	3.0V ≤ V^+ ≤ 30V T_A = 25°C	Digital Low Level			0.8	V
		Digital High Level	2.0			
Logic Input Current MIC5014 (non-inverting)	3.0V ≤ V^+ ≤ 30V	V_{IN} Low	–2.0	0		µA
		V_{IN} High		1.0	2.0	
Logic Input Current MIC5015 (inverting)	3.0V ≤ V^+ ≤ 30V	V_{IN} Low	–2.0	–1.0		µA
		V_{IN} High		–1.0	2.0	
Input Capacitance				5.0		pF
Gate Enhancement $V_{GATE} - V_{SUPPLY}$	3.0V ≤ V^+ ≤ 30V	V_{IN} Asserted	4.0		17	V
Zener Clamp $V_{GATE} - V_{SOURCE}$	8.0V ≤ V^+ ≤ 30V	V_{IN} Asserted	13	15	17	V
Gate Turn-on Time, t_{ON} (Note 4)	V^+ = 4.5V C_L = 1000pF	V_{IN} switched on, measure time for V_{GATE} to reach V^+ + 4V		2.5	8.0	ms
	V^+ = 12V C_L = 1000pF	As above, measure time for V_{GATE} to reach V^+ + 4V		90	140	µs
Gate Turn-off Time, t_{OFF} (Note 4)	V^+ = 4.5V C_L = 1000pF	V_{IN} switched off, measure time for V_{GATE} to reach 1V		6.0	30	µs
	V^+ = 12V C_L = 1000pF	As above, measure time for V_{GATE} to reach 1V		6.0	30	µs
Overvoltage Shutdown Threshold			35	37	41	V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Electrical specifications do not apply when operating the device beyond its specified **Operating Ratings**.

Note 2: The MIC5014/5015 is ESD sensitive.

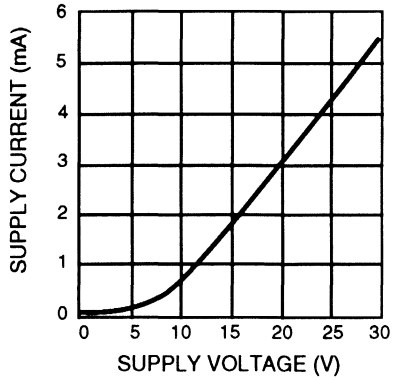
Note 3: Minimum and maximum **Electrical Characteristics** are 100% tested at T_A = 25°C and T_A = 85°C, and 100% guaranteed over the entire operating temperature range. Typicals are characterized at 25°C and represent the most likely parametric norm.

Note 4: Test conditions reflect worst case high-side driver performance. Low-side and bootstrapped topologies are significantly faster—see Applications Information. Maximum value of switching time seen at 125°C, unit operated at room temperature will reflect the typical value shown.

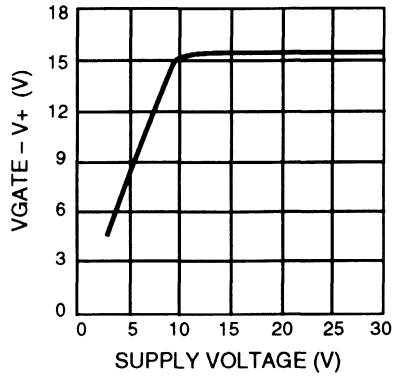
Note 5: "Asserted" refers to a logic high on the MIC5014 and a logic low on the MIC5015.

Typical Characteristics: (Note: All data was taken using a FET probe to eliminate inaccuracy due to resistive loading.)

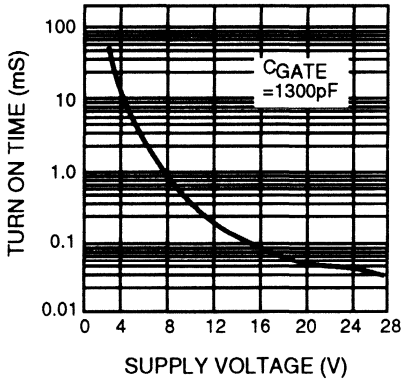
Supply Current (ON state)



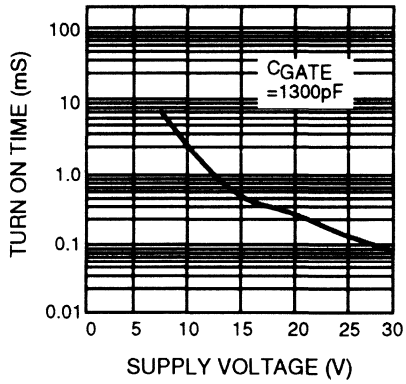
DC Gate Voltage above Supply



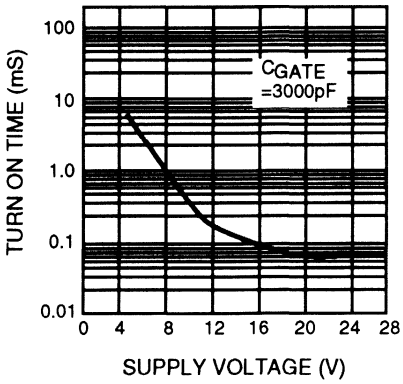
High Side Turn-on Time for Gate = 4V + Supply



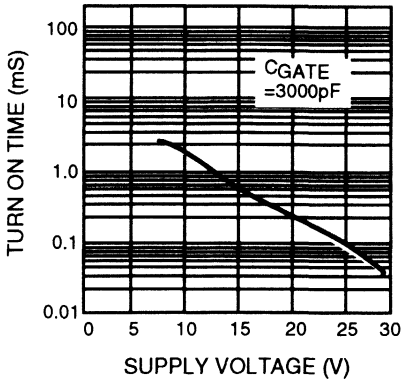
High Side Turn-on Time for Gate = 10 V + Supply



High Side Turn-on Time for Gate = 4V + Supply

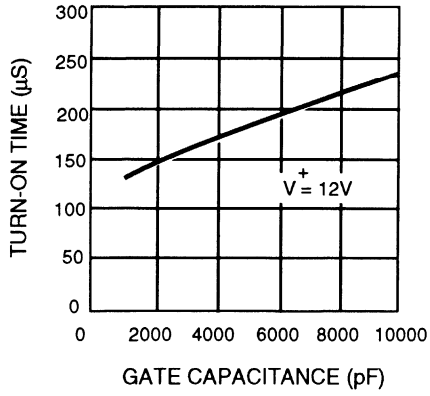


High Side Turn-on Time for Gate = 10 V + Supply

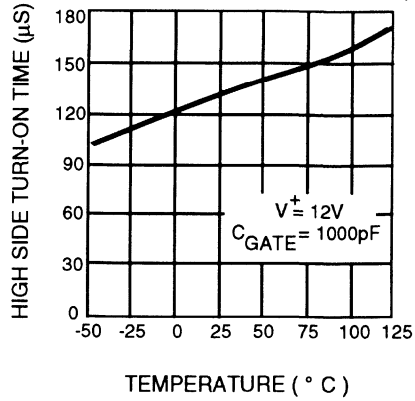


Typical Characteristics (Continued)

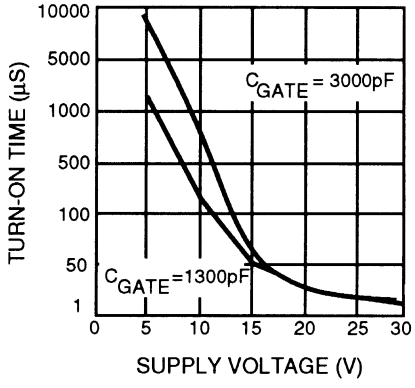
High Side Turn-on Time vs. Gate Capacitance



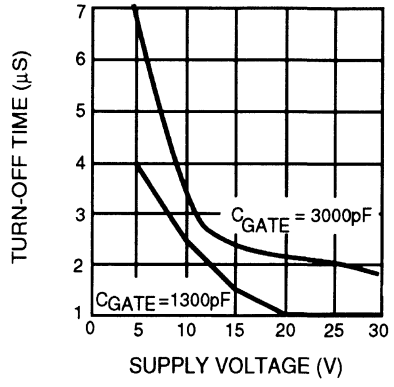
High Side Turn-on Time vs. Temperature (Ambient)



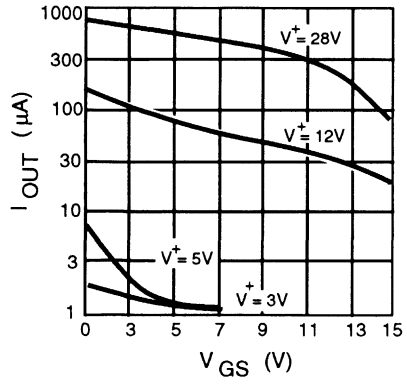
Low-side Turn-on Time for Gate = 4V



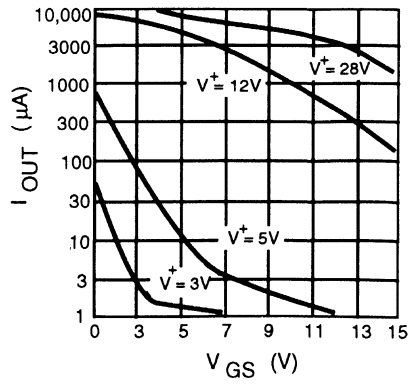
High Side Turn-off Time (Time to V_{GS} = 1V)



Charge Pump Output Current, $V_S = V^+$



Charge Pump Output Current, V_S = Ground



Applications Information

Functional Description

The MIC5014 is functionally and pin for pin compatible with the MIC5011, except for the omission of the optional speed-up capacitor pins, which are available on the MIC5011. The MIC5015 is an inverting configuration of the MIC5014.

The internal functions of these devices are controlled via a logic block (refer to block diagram) connected to the control input (pin 2). When the input is off (low for the MIC5014, and high for the MIC5015), all functions are turned off, and the gate of the external power MOSFET is held low via two N-channel switches. This results in a very low standby current; 15μA typical, which is necessary to power an internal bandgap. When the input is driven to the "ON" state, the N-channel switches are turned off, the charge pump is turned on, and the P-channel switch between the charge pump and the gate turns on, allowing the gate of the power FET to be charged. The op amp and internal zener form an active regulator which shuts off the charge pump when the gate voltage is high enough. This is a feature not found on the MIC5011.

The charge pump incorporates a 100kHz oscillator and on-chip pump capacitors capable of charging a 1,000pF load in 90μs typical. In addition to providing active regulation, the internal 15V zener is included to prevent exceeding the V_{GS} rating of the power MOSFET at high supply voltages.

The MIC5014/15 devices have been improved for greater ruggedness and durability. All pins can withstand being pulled 20V below ground without sustaining damage, and the supply pin can withstand an overvoltage transient of 60V for 1s. An overvoltage shutdown has also been included, which turns off the device when the supply exceeds 35V.

Construction Hints

High current pulse circuits demand equipment and assembly techniques that are more stringent than normal, low current lab practices. The following are the sources of pitfalls most often encountered during prototyping: *Supplies*: Many bench power supplies have poor transient response. Circuits that are being pulse tested, or those that operate by pulse-width modulation will produce strange results when used with a supply that has poor ripple rejection, or a peaked transient response. Always monitor the power supply voltage that appears at the drain of a high side driver (or the supply side of the load for a low side driver) with an oscilloscope. It is not uncommon to find bench power supplies in the 1kW class that overshoot or undershoot by as much as 50% when pulse loaded. Not only will the load current and voltage measurements be affected, but it is possible to overstress various components, especially electrolytic capacitors, with possibly catastrophic results. A 10μF supply bypass capacitor *at the chip is* recommended. *Residual resistances*: Resistances in circuit connections may also cause confusing results. For example, a circuit may employ a 50mΩ power MOSFET for low voltage drop, but unless careful construction techniques are used, one could easily add 50 to 100mΩ resistance. Do not use a socket for the MOSFET. If the MOSFET is a TO-220 type package, make high current connections to the drain tab. Wiring losses have a profound effect on high-current circuits. A floating milliohmeter can identify connections that are contributing excess drop under load.

Low Voltage Testing

As the MIC5014/MIC5015 have relatively high output impedances, a normal oscilloscope probe will load the device. This is especially pronounced at low voltage operation. It is recommended that a FET probe or unity gain buffer be used for all testing.

Circuit Topologies

The MIC5014 and MIC5015 are well suited for use with standard power MOSFETs in both low and high side driver configurations. In addition, the lowered supply voltage requirements of these devices make them ideal for use with logic level FETs in high side applications with a supply voltage of 3 to 4V. (If higher supply voltages [>4V] are used with logic level FETs, an external zener clamp must be supplied to ensure that the maximum V_{GS} rating of the logic FET [10V] is not exceeded.) In addition, a standard IGBT can be driven using these devices.

Choice of one topology over another is usually based on speed vs. safety. The fastest topology is the low side driver, however, it is not usually considered as safe as high side driving as it is easier to accidentally short a load to ground than to V_{CC}. The slowest, but safest topology is the high side driver; with speed being inversely proportional to supply voltage. It is the preferred topology for most military and automotive applications. Speed can be improved considerably by bootstrapping from the supply.

All topologies implemented using these devices are well suited to driving inductive loads, as either the gate or the source pin can be pulled 20V below ground with no effect. External clamp diodes are unnecessary, except for the case in which a transient may exceed the overvoltage trip point.

High Side Driver (Figure 1) The high side topology shown here is an implementation of a "sleep-mode" switch for a laptop or notebook computer which uses a logic level FET. A standard power FET can easily be substituted when supply voltages above 4V are required.

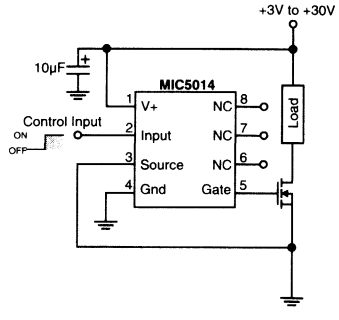


Figure 2. Low Side Driver

Low Side Driver (Figure 2) A key advantage of this topology, as previously mentioned, is speed. The MOSFET gate is driven to near supply immediately when the MIC5014/15 is turned on. Typical circuits reach full enhancement in 50µs or less with a 15V supply.

Bootstrapped High Side Driver (Figure 3) The turn-on time of a high side driver can be improved to faster than 40µs by bootstrapping the supply with the MOSFET source. The Schottky barrier diode prevents the supply pin from dropping more than 200mV below the drain supply and improves turn-on time. Since the supply current in the "off" state is only a small leakage, the 100nF bypass capacitor tends to remain charged for several seconds after the MIC5014/15 is turned off. Faster speeds can be obtained at the expense of supply voltage (the overvoltage shutdown will turn the part off when the bootstrapping action pulls the supply pin above 35V) by using a larger capacitor at the junction of the two 1N4001 diodes. In a PWM application (this circuit can be used for either PWM'ed or continuously energized loads), the chip supply is sustained at a higher potential than the system supply, which improves switching time.

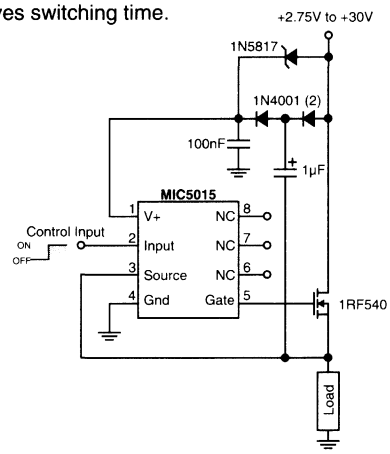


Figure 3. Bootstrapped Hgh-Side Driver

High Side Driver With Current Sense (Figure 4) Although no current sense function is included on the MIC5014/15 devices, a simple current sense function can be realized via the addition of one more active component; an LM301A op amp used as a comparator. The positive rail of the op amp is tied to V^+, and the negative rail is tied to ground. This op amp was chosen as it can withstand having input transients that swing below the negative rail, and has common mode range almost to the positive rail.

The inverting side of this comparator is tied to a voltage divider which sets the voltage to $V^+ - V_{TRIP}$. The non inverting side is tied to the node between the drain of the FET and the sense resistor. If the overcurrent trip point is not exceeded, this node will always be pulled above $V^+ - V_{TRIP}$, and the output of the comparator will be high which feeds the control input of the MIC5014 (polarities should be reversed if the MIC5015 is used). One the overcurrent trip point has been reached, the comparator will go low, which shuts off the MIC5014. When the the short is removed, feedback to the input pin insures that the MIC5014 will turn back on. This output can also be level shifted and sent to an I/O port of a microcontroller for intelligent control.

Current Shunts (R_S). Low valued resistors are necessary for use at R_S. Resistors are available with values ranging from 1 to 50mΩ, at 2 to 10W. If a precise overcurrent trip point is not necessary, then a nonprecision resistor or even a measured PCB trace can serve as R_S. The major cause of drift in resistor values with such resistors is temperature coefficient; the designer should be aware that a linear, 500 ppm/°C change will contribute as much as 10% shift in the overcurrent trip point. If this is not acceptable, a power resistor designed for current shunt service (drifts less than 100 ppm/°C), or a Kelvin-sensed resistor may be used.†

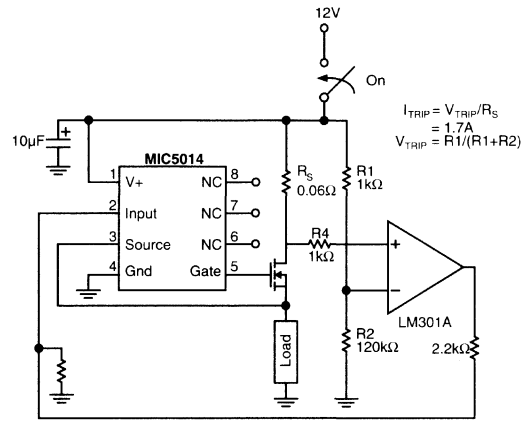


Figure 4. High Side Driver with Overcurrent Shutdown

† Suppliers of Precision Power Resistors:
Dale Electronics, Inc., 2064 12th Ave., Columbus, NE 68601. (402) 565-3131
International Resistive Co., P.O. Box 1860, Boone,NC 28607-1860. (704) 264-8861
Isotek Corp., 566 Wilbur Ave. Swansea, MA 02777. (508) 673-2900
Kelvin, 14724 Ventura Blvd., Ste. 1003, Sherman Oaks, CA 91403-3501. (818) 990-1192
RCD Components, Inc., 520 E. Industrial Pk. Dr., Manchester, NH 03103. (603) 669-0054
Ultronix, Inc., P.O. Box 1090, Grand Junction, CO 81502 (303) 242-0810

High Side Driver With Delayed Current Sense (Figure 5) Delay of the overcurrent detection to accomodate high inrush loads such as incandescent or halogen lamps can be accomplished by adding an LM3905 timer as a one shot to provide an open collector pulldown for the comparator output such that the control input of the MIC5015 stays low for a preset amount of time without interference from the current sense circuitry. Note that an MIC5015 must be used in this application (figure 5), as an inverting control input is necessary. The delay time is set by the RC time constant of the external components on pins 3 and 4 of the timer; in this case, 6ms was chosen.

An LM3905 timer was used instead of a 555 as it provides a clean transition, and is almost impossible to make oscillate. Good bypassing and noise immunity is essential in this circuit to prevent spurious op amp oscillations.

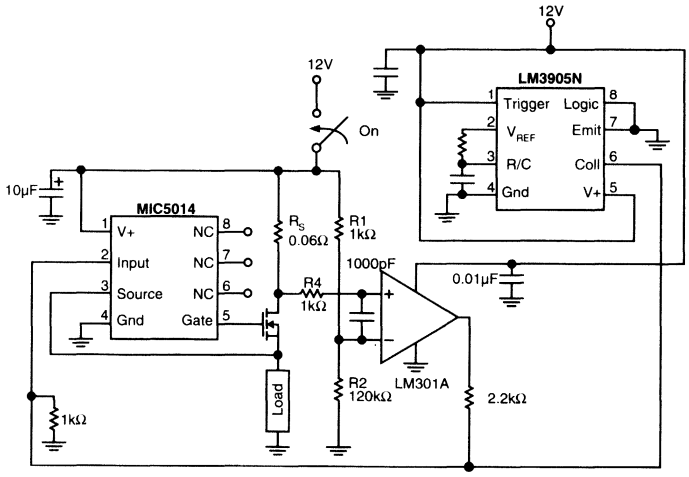


Figure 5. High Side Driver with Delayed Overcurrent Shutdown

Typical Applications

Variable Supply Low Side Driver for Motor Speed Control (Figure 6) The internal regulation in the MIC5014/15 allows a steady gate enhancement to be supplied while the MIC5014/15 supply varies from 5V to 30V, without damaging the internal gate to source zener clamp. This allows the speed of the DC motor shown to be varied by varying the supply voltage.

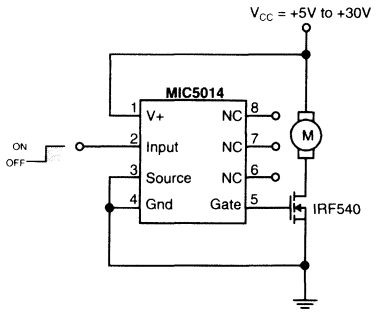


Figure 6: DC Motor Speed Control/Driver

Solenoid Valve Driver (Figure 7) High power solenoid valves are used in many industrial applications requiring the timed dispensing of chemicals or gases. When the solenoid is activated, the valve opens (or closes), releasing (or stopping) fluid flow. A solenoid valve, like all inductive loads, has a considerable "kickback" voltage when turned off, as current cannot change instantaneously through an inductor. In most applications, it is acceptable to allow this voltage to momentarily turn the MOSFET back on as a way of dissipating the inductor's current. However, if this occurs when driving a solenoid valve with a fast switching speed, chemicals or gases may be inadvertantly be dispensed at the wrong time with possibly disasterous consequences. Also, too large of a kickback voltage (as is found in larger solenoids) can damage the MIC5014 or the power FET by forcing the Source node below ground (the MIC5014 can be driven up to 20V below ground before this happens). A catch diode has been included in this design to provide an alternate route for the inductive kickback current to flow. The 5kΩ resistor in series with this diode has been included to set the recovery time of the solenoid valve.

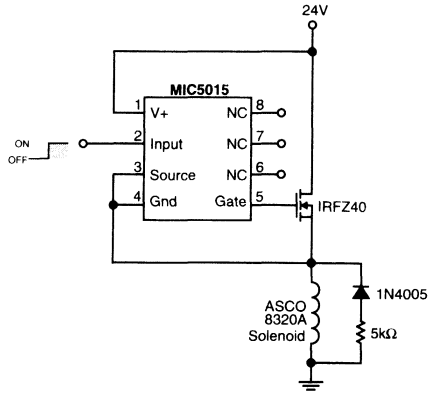


Figure 7: Solenoid Valve Driver

Incandescent/Halogen Lamp Driver (Figure 8) The combination of an MIC5014/5015 and a power FET makes an effective driver for a standard incandescent or halogen lamp load. Such loads often have high inrush currents, as the resistance of a cold filament is less than one-tenth as much as when it is hot. Power MOSFETs are well suited to this application as they have wider safe operating areas than do power bipolar transistors. It is important to check the SOA curve on the data sheet of the power FET to be used against the estimated or measured inrush current of the lamp in question prior to prototyping to prevent "explosive" results.

If overcurrent sense is to be used, first measure the duration of the inrush, then use the topology of Figure 5 with the RC of the timer chosen to accomodate the duration with suitable guardbanding.

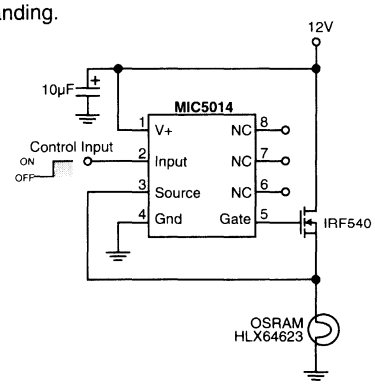


Figure 8. Halogen Lamp Driver

Relay Driver (Figure 9) Some power relay applications require the use of a separate switch or drive control, such as in the case of microprocessor control of banks of relays where a logic level control signal is used, or for drive of relays with high power requirements. The combination of an MIC5014/5015 and a power FET also provides an elegant solution to power relay drive.

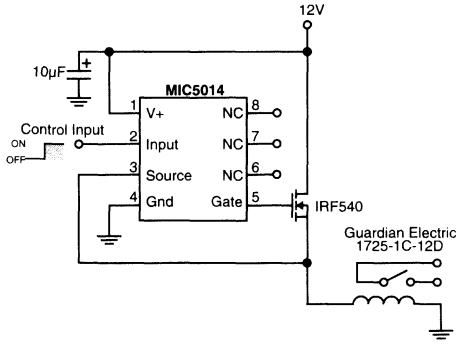


Figure 9: Relay Driver

Motor Driver With Stall Shutdown (Figure 10) Tachometer feedback can be used to shut down a motor driver circuit when a stall condition occurs. The control switch is a 3-way type; the "START" position is momentary and forces the driver ON. When released, the switch returns to the "RUN" position, and the tachometer's output is used to hold the MIC5014 input ON. If the motor slows down, the tach output is reduced, and the MIC5014 switches OFF. Resistor "R" sets the shutdown threshold.

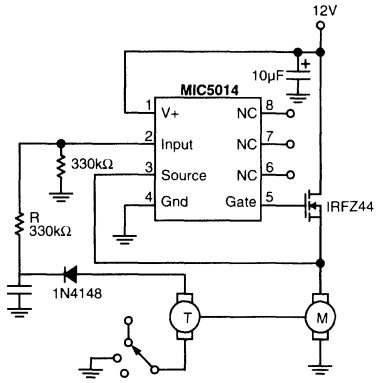


Figure 10. Motor Stall Shutdowm

Simple DC-DC Converter (Figure 11) The simplest application for the MIC5014 is as a basic one-chip DC-DC converter. As the output (Gate) pin has a relatively high impedance, the output voltage shown will vary significantly with applied load.

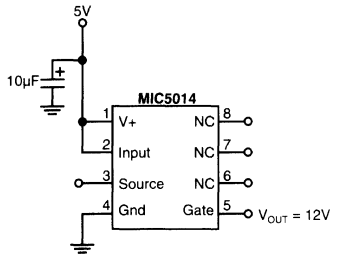


Figure 11. DC - DC Converter

High Side Driver With Load Protection (Figure 12) Although the MIC5014/15 devices are reverse battery protected, the load and power FET are not, in a typical high side configuration. In the event of a reverse battery condition, the internal body diode of the power FET will be forward biased. This allows the reversed supply access to the load.

The addition of a Schottky diode between the supply and the FET eliminates this problem. The MBR2035CT was chosen as it can withstand 20A continuous and 150A peak, and should survive the rigors of an automotive environment. The two diodes are paralleled to reduce switch loss (forward voltage drop).

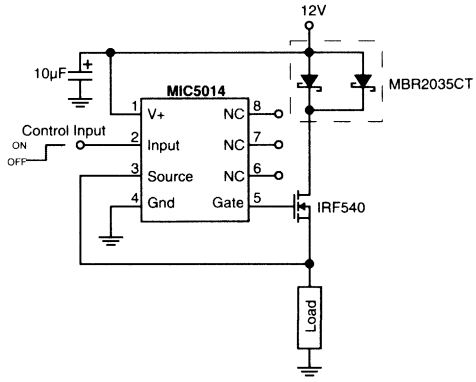


Figure 12: High Side Driver With Load Protection

Push-Pull Driver With No Cross-Conduction (Figure 13) As the turn-off time of the MIC5014/15 devices is much faster than the turn-on time, a simple push-pull driver with no cross conduction can be made using one MIC5014 and one MIC5015. The same control signal is applied to both inputs; the MIC5014 turns on with the positive signal, and the MIC5015 turns on when it swings low.

This scheme works with no additional components as the relative time difference between the rise and fall times of the MIC5014 is large. However, this does mean that there is considerable deadtime (time when neither driver is turned on). If this circuit is used to drive an inductive load, catch diodes must be used on each half to provide an alternate path for the kickback current that will flow during this deadtime.

This circuit is also a simple half H-bridge which can be driven with a PWM signal on the input for SMPS or motor drive applications in which high switching frequencies are not desired.

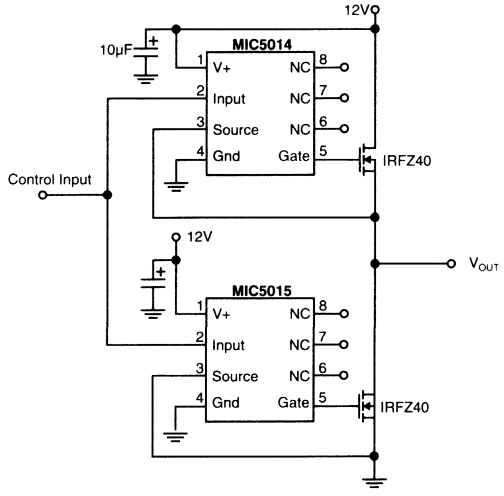


Figure 13: Push-Pull Driver

MIC5016/5017

Low Cost Dual MOSFET Predrivers

General Description

The MIC5016/5017 MOSFET dual predrivers are members of the MIC501X family and are pin compatible with the MIC5012. These versatile drivers are designed to provide gate enhancement above the positive supply for an N-channel FET used in high or low side switching applications.

The MIC5016/5017 devices have many improvements in addition to the ease of use and versatility of the earlier members of the MIC5010 family. Operation down to 2.75V allows the MIC5016/5017 to drive standard or logic level FETs in 2.75 to 5V low side applications by boosting the gate voltage above the positive supply. This feature makes these devices ideally suited for laptop/notebook computer applications.

The MIC5016/5017s are considerably more rugged than their predecessors, having both "load dump" and "reverse battery" capability. They can handle an output swing of up to 20V below ground, which can occur when driving an inductive load. An overvoltage shutdown at 35V prevents damage due to supply excursions. These features make the MIC5016/5017 ideal for use in automotive applications.

As in the MIC5011, an internal zener clamp is provided to protect the gate of the external FET. The value of this zener clamp has been increased from 12.5V to 15V to allow more flexibility in design, and it has been upgraded to provide voltage regulation. The MIC5017 is an inverting version of the MIC5016.

Typical Application

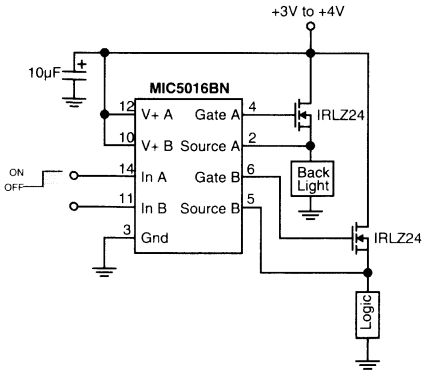


Figure 1: 3-Volt "Sleep-Mode" Switches with Logic Level FETs

Features

- 2.75V to 30V operation
- 100µA maximum supply current/channel at V_{DD} = 5V
- 15µA typical standby current/channel in the "off" state
- Internal charge pump to drive the gate of an N-channel power FET above supply
- Internal 15V zener clamp for gate protection
- Minimum external parts count
- Can be used to boost drive to low-side power or logic level FETs
- Implements high or low-side drivers
- Can withstand a 60V voltage transient (load dump).
- Designed to withstand having an input or output driven to 20V below the negative rail (inductive load).
- Reverse battery protected to –20V.
- 1µA pull-off on the control input.
- Available in inverting (MIC5017) and noninverting (MIC5016) forms.
- Overvoltage shutdown at 35V
- TTL compatible inputs

Applications

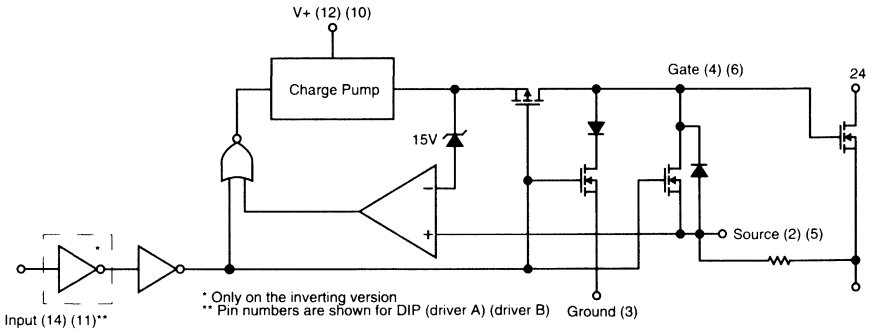
- Automotive motor/lamp/solenoid drive
- "Sleep-mode" battery saver switch for notebook/laptop computers
- Solenoid/solenoid – valve drive
- Heater switching
- Motion control
- Power bus switching
- Incandescent or halogen lamp drive

Ordering Information

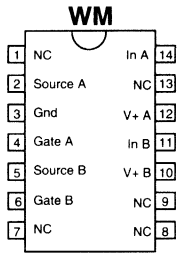
Part Number*	Temperature Range	Package
MIC5016AJ	–55°C to +125°C	14-Pin CERDIP
MIC5016AJB	–55°C to +125°C	14-Pin CERDIP
MIC5016BWM	–40°C to +85°C	16-Pin SOIC
MIC5016BN	–40°C to +85°C	14-Pin Plastic DIP
MIC5017AJ	–55°C to +125°C	14-Pin CERDIP
MIC5017AJB	–55°C to +125°C	14-Pin CERDIP
MIC5017BWM	–40°C to +85°C	16-Pin SOIC
MIC5017BN	–40°C to +85°C	14-Pin Plastic DIP

* Note: MIC5016 Dual Non-Inverting Predrivers
MIC5017 Dual Inverting Predrivers

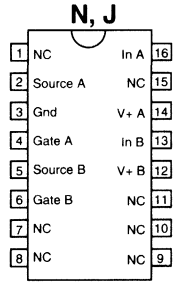
Block Diagram



Connection Diagram



14-pin DIP



14-pin DIP

Pin Description

Pin Name	DIP (14-pin)	SOIC (16-pin)	Pin Function
V^+A	12	14	Supply Pin A. Must be decoupled to isolate large transients caused by power FET drain. 10µF is recommended close to pins 12 and/or 10 and ground. V^+A and V^+B may be connected to separate supplies.
V^+B	10	12	Supply Pin B. See V^+A.
Input A	14	16	Turns on power MOSFET A when asserted. Requires approximately 1µA to switch.
Input B	11	13	Turns on power MOSFET B. See Input A.
Gate A	4	4	Drives and clamps the gate of power MOSFET A
Gate B	6	6	Drives and clamps the gate of power MOSFET B
Source A	2	2	Connects the source lead of MOSFET A
Source B	5	5	Connects the source lead of MOSFET B
Gnd	3	3	Ground

Absolute Maximum Ratings (Notes 1,2)

Supply Voltage (V^+), DIP pins 10, 12	–20V to 60V
Input Voltage, DIP pins 14, 11	–20V to V^+
Source Voltage, DIP pins 2, 5	–20V to V^+
Source Current, DIP pins 2, 5	50mA
Gate Voltage, DIP pins 4, 6	–20V to 50V
Junction Temperature	150°C

Operating Ratings (Notes 1,2)

θ_{JA} (Plastic DIP)	140°C/W
θ_{JA} (Ceramic DIP)	105°C/W
θ_{JA} (SOIC)	110°C/W
Ambient Temperature: B version	–40°C to +85°C
Ambient Temperature: A version	+55°C to +125°C
Storage Temperature	–65°C to +150°C
Lead Temperature (max soldering time: 10 seconds)	260°C
Supply Voltage (V^+)	2.75V to 30V

Electrical Characteristics (Note 3) T_A = –55°C to +125°C unless otherwise specified

Parameter	Conditions		Min	Typ	Max	Units
Supply Current (Each Driver Channel)	V^+ = 30V	V_{IN} De-Asserted (Note 5)		10	25	µA
		V_{IN} Asserted (Note 5)		5.0	8.5	mA
	V^+ = 5V	V_{IN} De-Asserted		0.1	1	µA
		V_{IN} Asserted		60	100	
	V^+ = 3V	V_{IN} De-Asserted		0.1	1	µA
		V_{IN} Asserted		25	35	
Logic Input Voltage Threshold V_{IN}	3.0V ≤ V^+ ≤ 30V T_A = 25°C	Digital Low Level			0.8	V
		Digital High Level	2.0			
Logic Input Current MIC5016 (non-inverting)	3.0V ≤ V^+ ≤ 30V	V_{IN} Low	–2.0	0		µA
		V_{IN} High		1.0	2.0	
Logic Input Current MIC5017 (inverting)	3.0V ≤ V^+ ≤ 30V	V_{IN} Low	–2.0	–1.0		µA
		V_{IN} High		–1.0	2.0	
Input Capacitance				5.0		pF
Gate Enhancement V_{GATE} - V_{SUPPLY}	3.0V ≤ V^+ ≤ 30V	V_{IN} Asserted	4.0		17	V
Zener Clamp V_{GATE} - V_{SOURCE}	8.0V ≤ V^+ ≤ 30V	V_{IN} Asserted	13	15	17	V
Gate Turn-on Time, t_{ON} (Note 4)	V^+ = 4.5V C_L = 1000pF	V_{IN} switched on, measure time for V_{GATE} to reach V^+ + 4V		2.5	8.0	ms
	V^+ = 12V C_L = 1000pF	As above, measure time for V_{GATE} to reach V^+ + 4V		90	140	µs
Gate Turn-off Time, t_{OFF} (Note 4)	V^+ = 4.5V C_L = 1000pF	V_{IN} switched off, measure time for V_{GATE} to reach 1V		6.0	30	µs
	V^+ = 12V C_L = 1000pF	As above, measure time for V_{GATE} to reach 1V		6.0	30	µs
Overvoltage Shutdown Threshold			35	37	41	V

Note 1: **Absolute Maximum Ratings** indicate limits beyond which damage to the device may occur. Electrical specifications do not apply when operating the device beyond its specified **Operating Ratings**.

Note 2: The MIC5016/5017 is ESD sensitive.

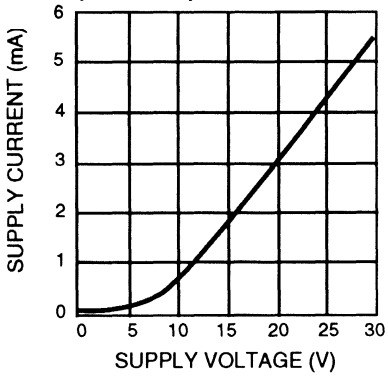
Note 3: Minimum and maximum **Electrical Characteristics** are 100% tested at T_A = 25°C and T_A = 85°C, and 100% guaranteed over the entire operating temperature range. Typicals are characterized at 25°C and represent the most likely parametric norm.

Note 4: Test conditions reflect worst case high-side driver performance. Low-side and bootstrapped topologies are significantly faster—see Applications Information. Maximum value of switching time seen at 125°C, unit operated at room temperature will reflect the typical value shown.

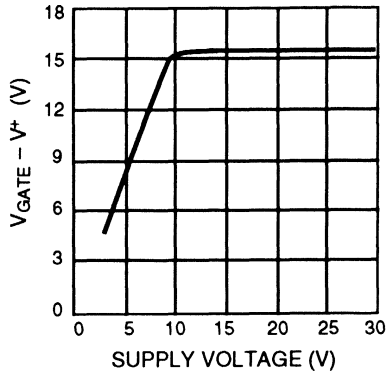
Note 5: "Asserted" refers to a logic high on the MIC5016 and a logic low on the MIC5017.

Typical Characteristics : (Note: All data was taken using a FET probe to eliminate inaccuracies due to loading)

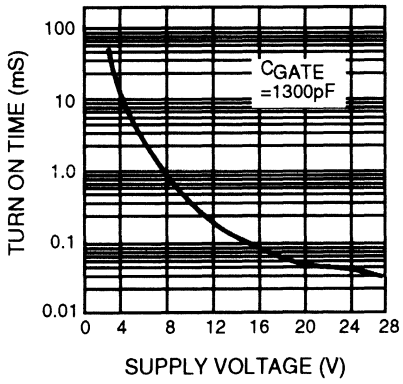
Supply Current/Channel (ON state)



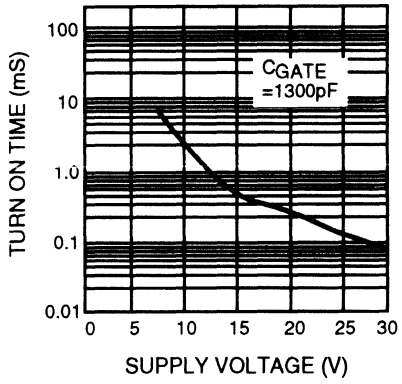
DC Gate Voltage above Supply



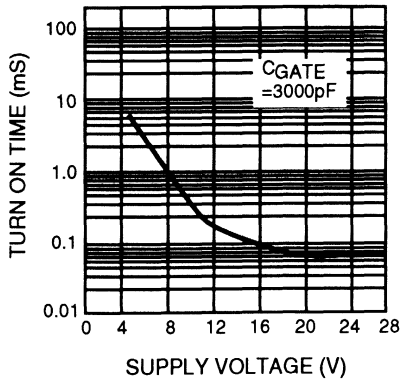
High Side Turn-on Time for Gate = 4V + Supply



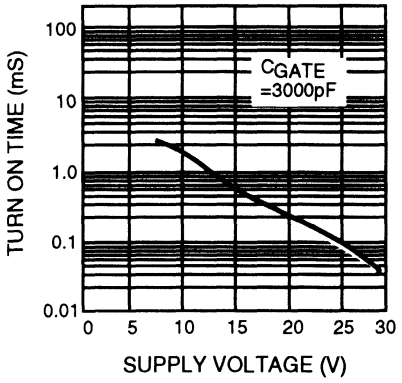
High Side Turn-on Time for Gate = 10V + Supply



High Side Turn-on Time for Gate = 4V + Supply



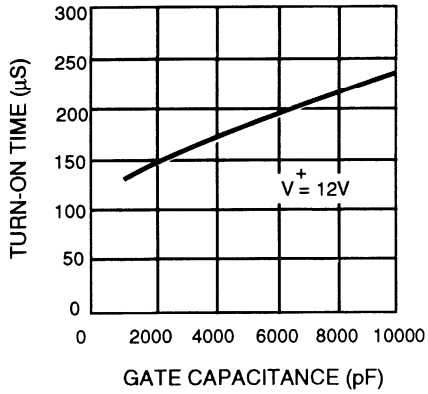
High Side Turn-on Time for Gate = 10V + Supply



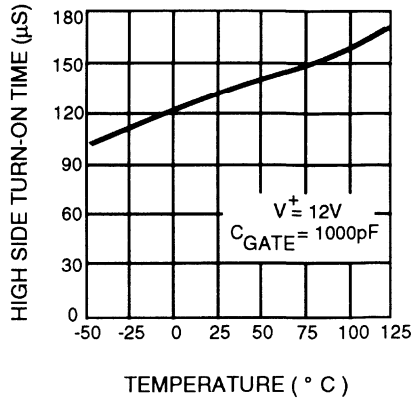
2

Typical Characteristics (Continued)

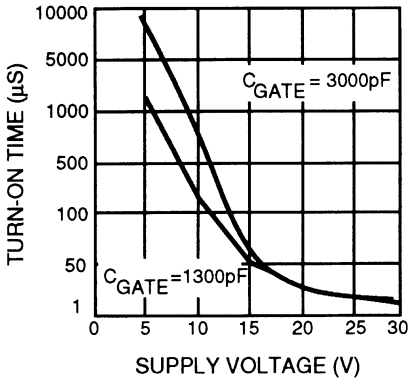
High Side Turn-on Time vs. Gate Capacitance



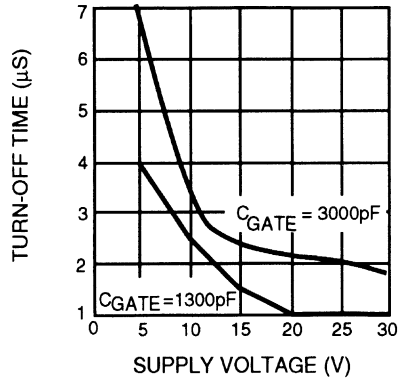
High Side Turn-on Time vs. Temperature (Ambient)



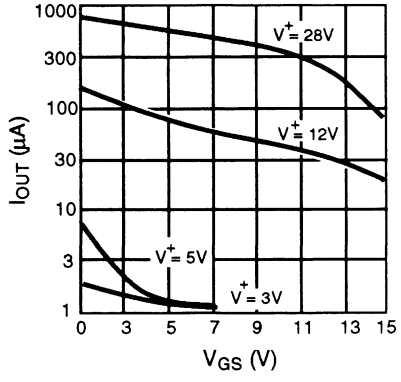
Low-side Turn-on Time for Gate = 4V



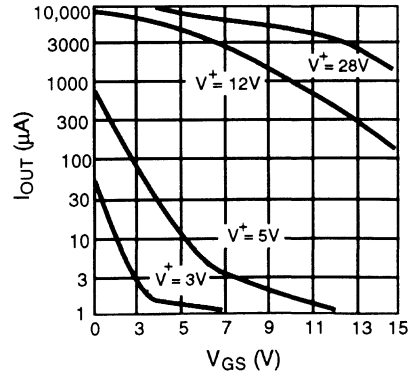
High Side Turn-off Time (Time to 1V)



Charge Pump Output Current, $V_S = V^+$



Charge Pump Output Current, V_S = Ground



Applications Information

Functional Description

The MIC5016 is functionally compatible with the MIC5012, and the MIC5017 is an inverting configuration of the MIC5016.

The internal functions of these devices are controlled via a logic block (refer to block diagram) connected to the control input (pin 14). When the input is off (low for the MIC5016, and high for the MIC5017), all functions are turned off, and the gate of the external power MOSFET is held low via two N-channel switches. This results in a very low standby current; 15μA typical, which is necessary to power an internal bandgap. When the input is driven to the "ON" state, the N-channel switches are turned off, the charge pump is turned on, and the P-channel switch between the charge pump and the gate turns on, allowing the gate of the power FET to be charged. The op amp and internal zener form an active regulator which shuts off the charge pump when the gate voltage is high enough. This is a feature not found on the MIC5012.

The charge pump incorporates a 100kHz oscillator and on-chip pump capacitors capable of charging a 1,000pF load in 90μs typical. In addition to providing active regulation, the internal 15V zener is included to prevent exceeding the V_{GS} rating of the power MOSFET at high supply voltages.

The MIC5016/17 devices have been improved for greater ruggedness and durability. All pins can withstand being pulled 20 V below ground without sustaining damage, and the supply pin can withstand an overvoltage transient of 60V for 1s. An overvoltage shutdown has also been included, which turns off the device when the supply reaches 35V.

Construction Hints

High current pulse circuits demand equipment and assembly techniques that are more stringent than normal, low current lab practices. The following are the sources of pitfalls most often encountered during prototyping: *Supplies*: Many bench power supplies have poor transient response. Circuits that are being pulse tested, or those that operate by pulse-width modulation will produce strange results when used with a supply that has poor ripple rejection, or a peaked transient response. Always monitor the power supply voltage that appears at the drain of a high side driver (or the supply side of the load for a low side driver) with an oscilloscope. It is not uncommon to find bench power supplies in the 1kW class that overshoot or undershoot by as much as 50% when pulse loaded. Not only will the load current and voltage measurements be affected, but it is possible to overstress various components, especially electrolytic capacitors, with possibly catastrophic results. A 10μF supply bypass capacitor *at the chip is* recommended. *Residual resistances*: Resistances in circuit connections may also cause confusing results. For example, a circuit may employ a 50mΩ power MOSFET for low voltage drop, but unless careful construction techniques are used, one could easily add 50 to 100mΩ resistance. Do not use a socket for the MOSFET. If the MOSFET is a TO-220 type package, make high current connections to the drain tab. Wiring losses have a profound effect on high-current circuits. A floating milliohmeter can identify connections that are contributing excess drop under load.

Low Voltage Testing As the MIC5016/5017 have relatively high output impedances, a normal oscilloscope probe will load the device. This is especially pronounced at low voltage operation. It is recommended that a FET probe or unity gain buffer be used for all testing.

Circuit Topologies

The MIC5016 and MIC5017 are well suited for use with standard power MOSFETs in both low and high side driver configurations. In addition, the lowered supply voltage requirements of these devices make them ideal for use with logic level FETs in high side applications with a supply voltage of 3V to 4V. (If higher supply voltages [>4V] are used with logic level FETs, an external zener clamp must be supplied to ensure that the maximum V_{GS} rating of the logic FET [10V] is not exceeded). In addition, a standard IGBT can be driven using these devices.

Choice of one topology over another is usually based on speed vs. safety. The fastest topology is the low side driver, however, it is not usually considered as safe as high side driving as it is easier to accidentally short a load to ground than to V_{CC} The slowest, but safest topology is the high side driver; with speed being inversely proportional to supply voltage. It is the preferred topology for most military and automotive applications. Speed can be improved considerably by bootstrapping the supply.

All topologies implemented using these devices are well suited to driving inductive loads, as either the gate or the source pin can be pulled 20V below ground with no effect. External clamp diodes are unnecessary, except for the case in which a transient may exceed the overvoltage trip point.

High Side Driver (Figure 1) The high side topology shown here is an implementation of a "sleep-mode" switch for a laptop or notebook computer which uses a logic level FET. A standard power FET can easily be substituted when supply voltages above 4V are required.

Low Side Driver (Figure 2) A key advantage of this topology, as previously mentioned, is speed. The MOSFET gate is

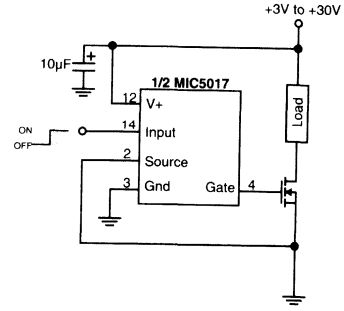


Figure 2. Low Side Driver

driven to near supply immediately when the MIC5016/17 is turned on. Typical circuits reach full enhancement in 50µs or less with a 15V supply.

Bootstrapped High Side Driver (Figure 3) The turn-on time of a high side driver can be improved to faster than 40µs by bootstrapping the supply with the MOSFET source. The Schottky barrier diode prevents the supply pin from dropping more than 200mV below the drain supply, and improves turn-on time. Since the supply current in the "OFF" state is only a small leakage, the 100nF bypass capacitor tends to remain charged for several seconds after the MIC5016/17 is turned off. Faster switching speeds can be obtained at the expense of supply voltage (the overvoltage shutdown will turn the part off when the bootstrapping action pulls the supply pin above 35V) by using a larger capacitor at the junction of the two 1N4001 diodes. In a PWM application (this circuit can be used for either PWM'ed or continuously energized loads), the chip supply is sustained at a higher potential than the system supply, which improves switching time.

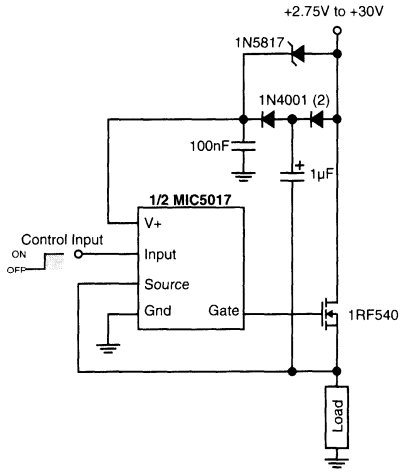


Figure 3. Bootstrapped High-Side Driver

High Side Driver With Current Sense (Figure 4) Although no current sense function is included on the MIC5016/17 devices, a simple current sense function can be realized via the addition of one more active component; an LM301A op amp used as a comparator. The positive rail of the op amp is tied to V^+, and the negative rail is tied to ground. This op amp was chosen as it can withstand having input transients that swing below the negative rail, and has common mode range almost to the positive rail.

The inverting side of this comparator is tied to a voltage divider which sets the voltage to $V^+ - V_{TRIP}$. The noninverting side is tied to the node between the drain of the FET and the sense resistor. If the overcurrent trip point is not exceeded, this node will always be above $V^+ - V_{TRIP}$, and the output of the comparator will be high which feeds the control input of the MIC5016 (polarities should be reversed if the MIC5017 is used). Once the overcurrent trip point has been reached, the comparator will go low, which shuts off the MIC5016. When the short is removed, feedback to the input pin insures that the MIC5016 will turn back on. This output can also be level shifted and sent to an I/O port of a microcontroller for intelligent control.

Current Shunts (R_S). Low valued resistors are necessary for use at R_S. Resistors are available with values ranging from 1 to 50mΩ, at 2 to10W. If a precise overcurrent trip point is not necessary, then a nonprecision resistor or even a measured PCB trace can serve as R_S. The major cause of drift in resistor values with such resistors is temperature coefficient; the designer should be aware that a linear, 500ppm/°C change will contribute as much as 10% shift in the overcurrent trip point.

If this is not acceptable, a power resistor designed for current shunt service (drifts less than 100ppm/°C), or a Kelvin-sensed resistor may be used.†

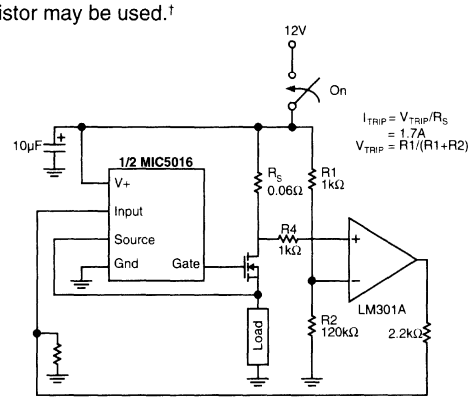


Figure 4. High Side Driver with Overcurrent Shutdown

† Suppliers of Precision Power Resistors:
Dale Electronics, Inc., 2064 12th Ave., Columbus, NE 68601. (402) 565-3131
International Resistive Co., P.O. Box 1860, Boone,NC 28607-1860. (704) 264-8861
Isotek Corp., 566 Wilbur Ave. Swansea, MA 02777. (508) 673-2900
Kelvin, 14724 Ventura Blvd., Ste. 1003, Sherman Oaks, CA 91403-3501. (818) 990-1192
RCD Components, Inc., 520 E. Industrial Pk. Dr., Manchester, NH 03103. (603) 669-0054
Ultronix, Inc., P.O. Box 1090, Grand Junction, CO 81502 (303) 242-0810

High Side Driver With Delayed Current Sense (Figure 5) Delay of the overcurrent detection to accomodate high inrush loads such as incandescent or halogen lamps can be accomplished by adding an LM3905 timer as a one shot to provide an open collector pulldown for the comparator output such that the control input of the MIC5017 stays low for a preset amount of time without interference from the current sense circuitry. Note that an MIC5017 must be used in this application (figure 5), as an inverting control input is necessary. The delay time is set by the RC time constant of the external components on pins 3 and 4 of the timer; in this case, 6ms was chosen.

An LM3905 timer was used instead of a 555 as it provides a clean transition, and is almost impossible to make oscillate. Good bypassing and noise immunity is essential in this circuit to prevent spurious op amp oscillations.

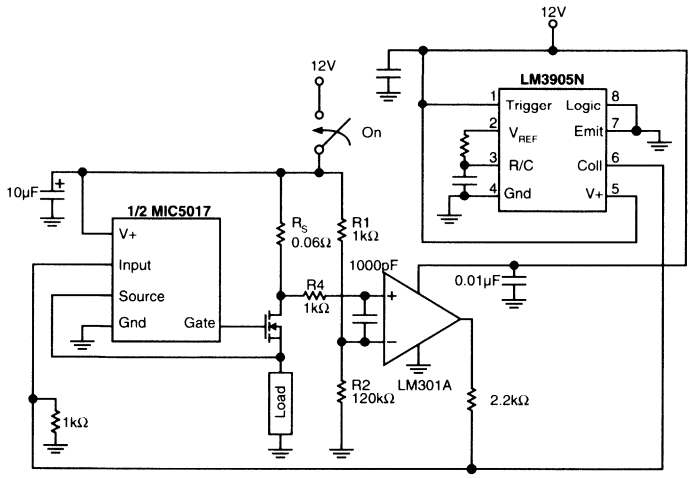


Figure 5. High Side Driver with Delayed Overcurrent Shutdown

Typical Applications

Variable Supply Low Side Driver for Motor Speed Control (Figure 6) The internal regulation in the MIC5016/17 allows a steady gate enhancement to be supplied while the MIC5016/17 supply varies from 5V to 30V, without damaging the internal gate to source zener clamp. This allows the speed of the DC motor shown to be varied by varying the supply voltage.

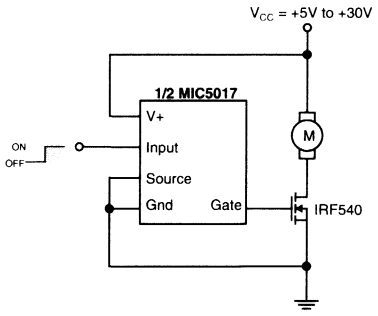


Figure 6: DC Motor Speed Control/Driver

Solenoid Valve Driver (Figure 7) High power solenoid valves are used in many industrial applications requiring the timed dispensing of chemicals or gases. When the solenoid is activated, the valve opens (or closes), releasing (or stopping) fluid flow. A solenoid valve, like all inductive loads, has a considerable "kickback" voltage when turned off, as current cannot change instantaneously through an inductor. In most applications, it is acceptable to allow this voltage to momentarily turn the MOSFET back on as a way of dissipating the inductor's current. However, if this occurs when driving a solenoid valve with a fast switching speed, chemicals or gases may inadvertantly be dispensed at the wrong time with possibly disasterous consequences. Also, too large of a kickback voltage (as is found in larger solenoids) can damage the MIC5016 or the power FET by forcing the Source node below ground (the MIC5016 can be driven up to 20V below ground before this happens). A catch diode has been included in this design to provide an alternate route for the inductive kickback current to flow. The 5kΩ resistor in series with this diode has been included to set the recovery time of the solenoid valve.

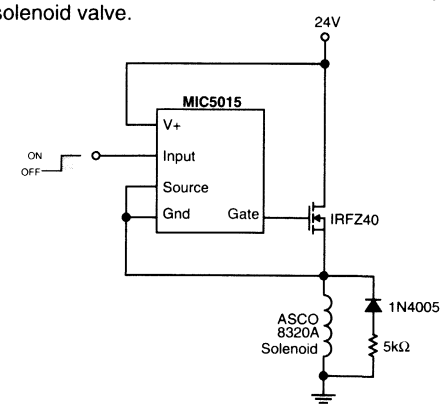


Figure 7: Solenoid Valve Driver

Incandescent/Halogen Lamp Driver (Figure 8) The combination of an MIC5016/5017 and a power FET makes an effective driver for a standard incandescent or halogen lamp load. Such loads often have high inrush currents, as the resistance of a cold filament is less than one-tenth as much as when it is hot. Power MOSFETs are well suited to this application as they have wider safe operating areas than do power bipolar transistors. It is important to check the SOA curve on the data sheet of the power FET to be used against the estimated or measured inrush current of the lamp in question prior to prototyping to prevent "explosive" results.

If overcurrent sense is to be used, first measure the duration of the inrush, then use the topology of Figure 5 with the RC of the timer chosen to accomodate the duration with suitable guardbanding.

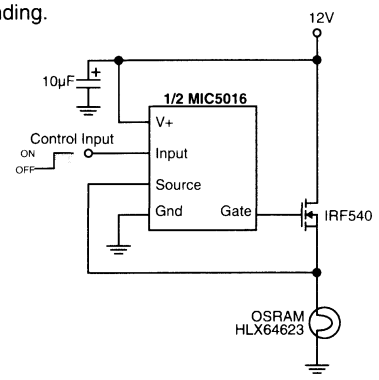


Figure 8: Halogen Lamp Driver

Relay Driver (Figure 9) Some power relay applications require the use of a separate switch or drive control, such as in the case of microprocessor control of banks of relays where a logic level control signal is used, or for drive of relays with high power requirements. The combination of an MIC5016/5017 and a power FET also provides an elegant solution to power relay drive.

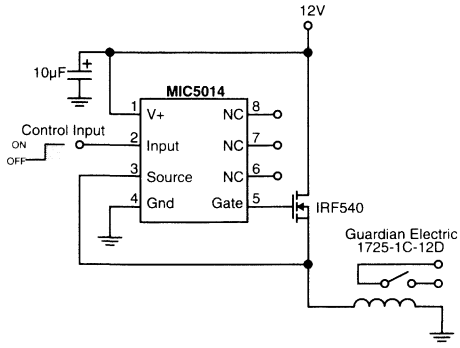


Figure 9: Relay Driver

Motor Driver With Stall Shutdown (Figure 10) Tachometer feedback can be used to shut down a motor driver circuit when a stall condition occurs. The control switch is a 3-way type; the "START" position is momentary and forces the driver ON. When released, the switch returns to the "RUN" position, and the tachometer's output is used to hold the MIC5016 input ON. If the motor slows down, the tach output is reduced, and the MIC5016 switches OFF. Resistor "R" sets the shutdown threshold.

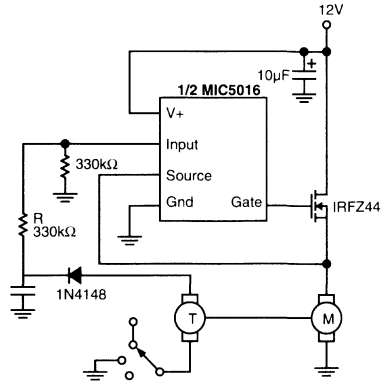


Figure 10. Motor Stall Shutdown

Simple DC-DC Converter (Figure 11) The simplest application for the MIC5016 is as a basic one-chip DC-DC converter. As the output (Gate) pin has a relatively high impedance, the output voltage shown will vary significantly with applied load.

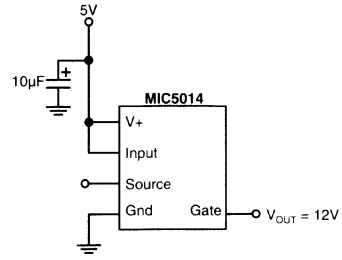


Figure 11. DC - DC Converter

High Side Driver With Load Protection (Figure 12) Although the MIC5016/17 devices are reverse battery protected, the load and power FET are not in a typical high side configuration. In the event of a reverse battery condition, the internal body diode of the power FET will be forward biased. This allows the reversed supply to drive the load.

An MBR2035CT dual Schottky diode was used to eliminate this problem. This particular diode can handle 20A continuous current and 150A peak current; therefore it should survive the rigors of an automotive environment. The diodes are paralleled to reduce the switch loss (forward voltage drop).

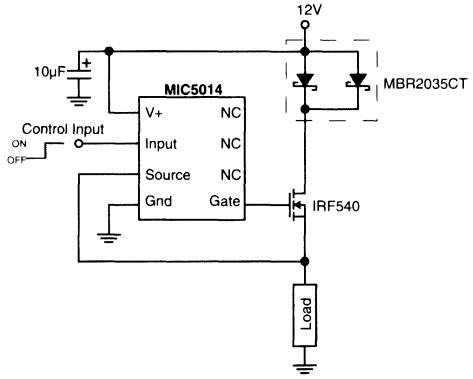


Figure 12: High Side Driver With Load Protection

Push-Pull Driver With No Cross-Conduction (Figure 13) As the turn-off time of the MIC5016/17 devices is much faster than the turn-on time, a simple dual push-pull driver with no cross conduction can be made using one MIC5016 and one MIC5017. The same control signal is applied to both inputs; the MIC5016 turns on with the positive signal, and the MIC5017 turns on when it swings low.

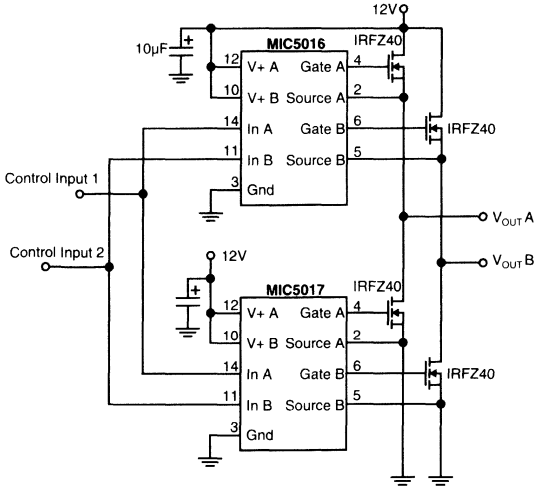


Figure 13: Push-Pull Driver

This scheme works with no additional components as the relative time difference between the rise and fall times of the MIC5014 is large. However, this does mean that there is considerable deadtime (time when neither driver is turned on). If this circuit is used to drive an inductive load, catch diodes must be used on each half to provide an alternate path for the kickback current that will flow during this deadtime.

This circuit is also a simple H-bridge which can be driven with a PWM signal on the input for SMPS or motor drive applications in which high switching frequencies are not desired.

Synchronous Rectifier (Figure 14) In applications where efficiency in terms of low forward voltage drops and low diode reverse-recovery losses is critical, power FETs are used to achieve rectification instead of a conventional diode bridge. Here, the power FETs are used in the third quadrant of the IV characteristic curve (FETs are installed essentially "backwards"). The two FETs are connected such that the top FET turns on with the positive going AC cycle, and turns off when it swings negative. The bottom FET operates opposite to the top FET.

In the first quadrant of operation, the limitation of the device is determined by breakdown voltage. Here, we are limited by the turn-on of a parasitic p-n body drain diode. If it is allowed to conduct, its reverse recovery time will crowbar the other power FET and possibly destroy it. The way to prevent this is to keep the IR drop across the device below the cut-in voltage of this diode; this is accomplished here by using a fast comparator to sense this voltage and feed the appropriate signal to the control inputs of the MIC5016 device. Obviously, it is very important to use a comparator with a fast slew rate such as the LM393, and fast recovery diodes. 3mV of positive feedback is used on the comparator to prevent oscillations.

At 3A, with an R_{DS} (ON) of 0.077Ω, our forward voltage drop per FET is ~ 0.2 V as opposed to the 0.7 to 0.8 V drop that a normal diode would have. Even greater savings can be had by using FETs with lower R_{DS}(ON)s, but care must be taken that the peak currents and voltages do not exceed the SOA of the chosen FET.

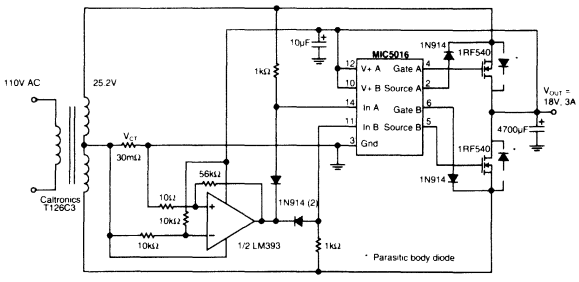


Figure 14: High Efficiency 60 Hz Synchronous Rectifier

MIC5020

Current-Sensing Low-Side MOSFET Driver

Preliminary Information

General Description

The MIC5020 low-side MOSFET driver is designed to operate at frequencies greater than 100kHz and is an ideal choice for high-speed applications such as motor control, SMPS (switch mode power supplies), and applications using IGBTS. The MIC5020 can also operate as a circuit breaker with or without automatic retry. The MIC5020's maximum supply voltage lends itself to control applications using up to 50V. The MIC5020 can control MOSFETs that switch voltages greater than 50V.

A rising or falling edge on the input results in a current source or sink pulse on the gate output. This output current pulse can turn on or off a 2000pF MOSFET in approximately 175ns. The MIC5020 then supplies a limited current (< 2mA), if necessary, to maintain the output state.

An overcurrent comparator with a trip voltage of 50mV makes the MIC5020 ideal for use with a current sensing MOSFET. An external low value resistor may be used instead of a sensing MOSFET for more precise overcurrent control. An optional external capacitor connected to the C_T pin may be used to control the current shutdown duty cycle from 20% to < 1%. A duty cycle from 20% to about 75% is possible with an optional pull-up resistor from C_T to V_{DD}. An open collector output provides a fault indication when the sense inputs are tripped.

The MIC5020 is available in 8-pin SOIC, plastic DIP, and CerDIP packages.

Other members of the MIC502x series include the MIC5021 high-side driver and the MIC5022 half-bridge driver with a cross-conduction interlock.

Features

- 11V to 50V operation
- 175ns rise/fall time driving 2000pF
- TTL compatible input with internal pull-down resistor
- Overcurrent limit
- Fault output indication
- Gate to source protection
- Compatible with current sensing MOSFETs

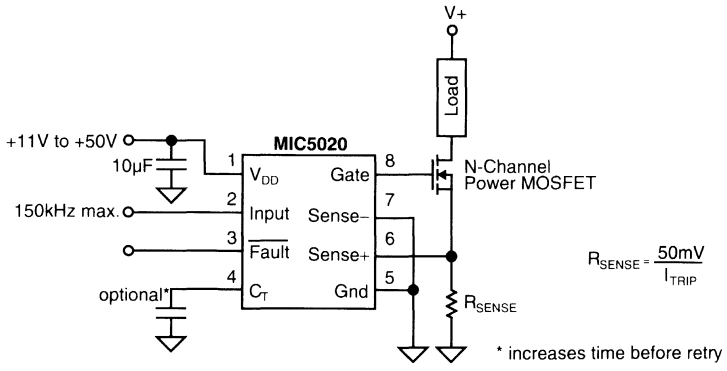
Applications

- Lamp control
- Heater control
- Motor control
- Solenoid switching
- Switch-mode power supplies
- Circuit breaker

Ordering Information

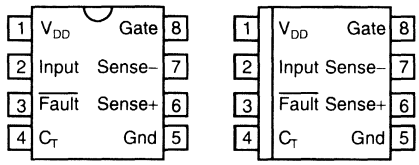
Part Number	Temperature Range	Package
MIC5020AJ	–55°C to +125°C	8-pin CerDIP
MIC5020BM	–40°C to +85°C	8-pin SOIC
MIC5020BN	–40°C to +85°C	8-pin Plastic DIP

Typical Application



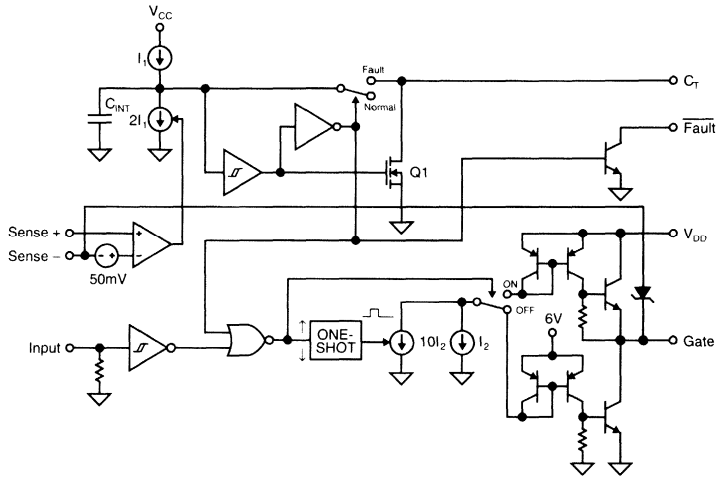
Low-Side Driver with Overcurrent Trip and Retry

Pin Configuration



DIP Packages (N, J) **SOIC Package (M)**

Block Diagram



Pin Description

Pin Number	Pin Name	Pin Function
1	V_{DD}	Supply: +11V to +50V. Decouple with ≥ 10µF capacitor.
2	Input	TTL Compatible Input: Logic high turns the external MOSFET on. An internal pull-down returns an open pin to logic low.
3	$\overline{Fault}$	Overcurrent Fault Indicator: When the sense voltage exceeds threshold, open collector output is open circuit for 5µs ($t_{G(ON)}$), then pulled low for $t_{G(OFF)}$. $t_{G(OFF)}$ is adjustable from C_T.
4	C_T	Retry Timing Capacitor: Controls the off time ($t_{G(OFF)}$) of the overcurrent retry cycle. (Duty cycle adjustment.) • Open = 20% duty cycle. • Capacitor to Ground = approx. 20% to <1% duty cycle. • Pull-Up resistor = approx. 20% to approx. 75% duty cycle. • Ground = maintained shutdown upon overcurrent condition.
5	Gnd	Circuit Ground
6	Sense +	Current Sense Comparator (+) Input: Connect to high side of sense resistor or current sensing MOSFET sense lead. A built-in offset in conjunction with R_{SENSE} sets the load overcurrent trip point.
7	Sense –	Current Sense Comparator (–) Input: Connect to the low side of the sense resistor (usually power ground).
8	Gate	Gate Drive: Drives the gate of an external power MOSFET. Also limits V_{GS} to 15V max. to prevent Gate to Source damage. Will sink and source current.

Absolute Maximum Ratings

Supply Voltage (V_{DD}) ..... +50V
Input Voltage ..... –0.5V to +15V
Sense Differential Voltage ..... ±6.5V
Sense + or Sense – to Gnd ..... –0.5V to +50V
Fault Voltage ..... +50V
Current into $\overline{Fault}$ 50mA
Timer Voltage (C_T) ..... +5.5V

Operating Ratings

Supply Voltage (V_{DD}) ..... +11V to +50V
Temperature Range
CerDIP ..... –55°C to +125°C
SOIC ..... –40°C to +85°C
Plastic DIP ..... –40°C to +85°C

Electrical Characteristics

T_A = 25°C, Gnd = 0V, V_{DD} = 12V, Sense +,– = 0V, Fault = Open, C_T = Open, Gate C_L = 1500pF unless otherwise specificed

Symbol	Parameter	Condition	Min	Typ	Max	Units
	D.C. Supply Current	V_{DD} = 12V, Input = 0V		0.8	2	mA
		V_{DD} = 50V, Input = 0V		2	10	mA
		V_{DD} = 12V, Input = 5V		0.8	2	mA
		V_{DD} = 50V, Input = 5V		4	25	mA
	Input Threshold		0.8	1.4	2.0	V
	Input Hysteresis			0.1		V
	Input Pull-Down Current	Input = 5V	10	20	40	µA
	Fault Output Saturation Voltage	Fault Current = 1.6mA **Note 1**		0.15	0.4	V
	Fault Output Leakage	Fault = 50V	–1	0.01	+1	µA
	Current Limit Threshold	**Note 2**	30	50	70	mV
	Gate On Voltage	V_{DD} = 12V	10	11		V
		V_{DD} = 50V	14	15	18	V
$t_{G(ON)}$	Gate On Time, Fixed	Sense Differential > 70mV	2	5	10	µs
$t_{G(OFF)}$	Gate Off Time, Adjustable	Sense Differential > 70mV, C_T = 0pF	10	20	50	µs
t_{DLH}	Gate Turn-On Delay	**Note 3**		400	800	ns
t_R	Gate Rise Time	**Note 4**		700	1500	ns
t_{DLH}	Gate Turn-Off Delay	**Note 5**		900	1500	ns
t_F	Gate Fall Time	**Note 6**		500	1500	ns
f_{max}	Maximum Operating Frequency	**Note 7**	100	150		kHz

Note 1 Voltage remains low for time affected by C_T.

Note 2 When using sense MOSFETs, it is recommended that R_{SENSE} < 50Ω. Higher values may affect the sense MOSFET's current transfer ratio.

Note 3 Input switched from 0.8V (TTL low) to 2.0V (TTL high), time for Gate transition from 0V to 2V.

Note 4 Input switched from 0.8V (TTL low) to 2.0V (TTL high), time for Gate transition from 2V to 10V.

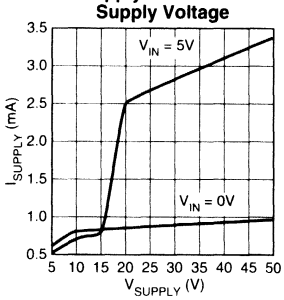
Note 5 Input switched from 2.0V (TTL high) to 0.8V (TTL low), time for Gate transition from 11V (Gate ON voltage) to 10V.

Note 6 Input switched from 2.0V (TTL high) to 0.8V (TTL low), time for Gate transition from 10V from 2V.

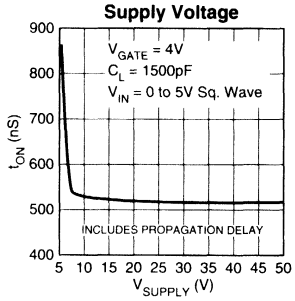
Note 7 Frequency where gate on voltage reduces to 10V with 50% input duty cycle.

Typical Characteristics

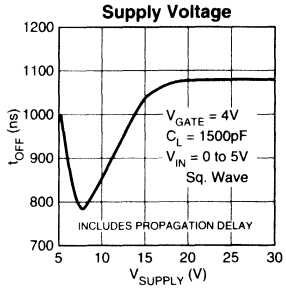
Supply Current vs. Supply Voltage



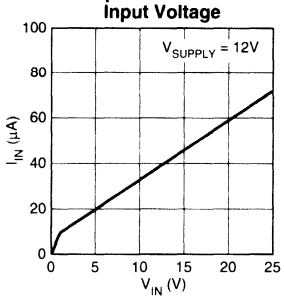
Turn-On Time vs. Supply Voltage



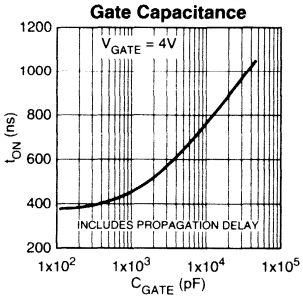
Turn-Off Time vs. Supply Voltage



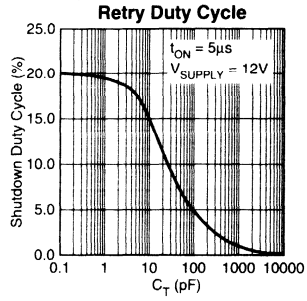
Input Current vs. Input Voltage



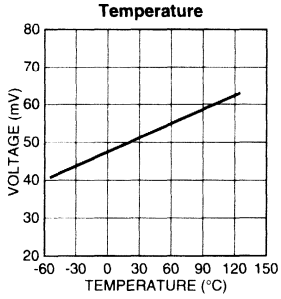
Turn-On Time vs. Gate Capacitance

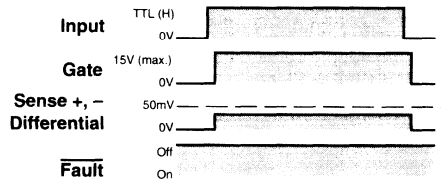


Overcurrent Shutdown Retry Duty Cycle

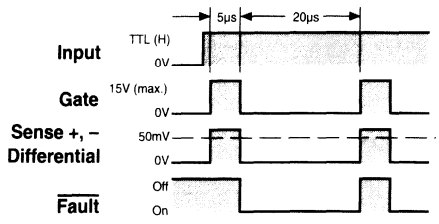


Sense Threshold vs. Temperature

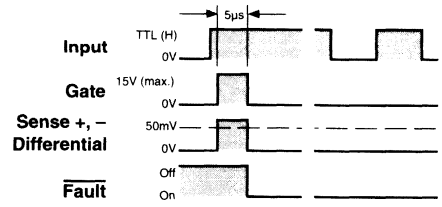




Timing Diagram 1. Normal Operation



Timing Diagram 2. Fault Condition, C_T = Open



Timing Diagram 3. Fault Condition, C_T = Grounded

Functional Description

Refer to the MIC5020 block diagram.

Input

A signal greater than 1.4V (nominal) applied to the MIC5020 INPUT causes gate enhancement on an external MOSFET turning the external MOSFET on.

An internal pull-down resistor insures that an open INPUT remains low, keeping the external MOSFET turned off.

Gate Output

Rapid rise and fall times on the GATE output are possible because each input state change triggers a one-shot which activates a high-value current sink ($10I_2$) for a short time. This draws a high current through a current mirror circuit causing the output transistors to quickly charge or discharge the external MOSFET's gate.

A second current sink continuously draws the lower value of current used to maintain the gate voltage for the selected state.

An internal 15V Zener diode protects the external MOSFET by limiting the gate output voltage when V_{DD} is connected to higher voltages.

Overcurrent Limiting

Current source I_1 charges C_{INT} upon power up. An optional external capacitor connected to C_T is discharged through MOSFET Q1.

A fault condition (> 50mV from SENSE + to SENSE –) causes the overcurrent comparator to enable current sink $2I_1$ which overcomes current source I_1 to discharge C_{INT} in a short time. When C_{INT} is discharged, the INPUT is disabled, which turns off the GATE output; the FAULT output is enabled; and C_{INT} and C_T are ready to be charged.

When the GATE output turns the MOSFET off, the overcurrent signal is removed from the sense inputs which deactivates current sink $2I_1$. This allows C_{INT} and the optional capacitor connected to C_T to recharge. A Schmitt trigger delays the retry while the capacitor(s) recharge. Retry delay is increased by connecting a capacitor to C_T (optional).

The retry cycle will continue until the the fault is removed or the input is changed to TTL low.

If C_T is connected to ground, the circuit will not retry upon a fault condition.

Fault Output

The FAULT output is an open collector transistor. FAULT is active at approximately the same time the output is disabled by a fault condition (5µs after an overcurrent condition is sensed). The FAULT output is open circuit (off) during each successive retry (5µs).

Applications Information

The MIC5020 MOSFET driver is intended for low-side switching applications where higher supply voltage, overcurrent sensing, and moderate speed are required.

Supply Voltage

A feature of the MIC5020 is that its supply voltage rating of up to 50V is higher than many other low-side drivers.

The minimum supply voltage required to fully enhance an N-channel MOSFET is 11V.

A lower supply voltage may be used with logic level MOSFETs. Approximately 6V is needed to provide 5V of gate enhancement.

Low-Side Switch Circuit Advantages

A moderate-speed low-side driver is generally much faster than a comparable high-side driver. The MIC5020 can provide the gate drive switching times and low propagation delay times that are necessary for high-frequency high-efficiency circuit operation in PWM (pulse width modulation) designs used for motor control, SMPS (switch mode power supply) and heating element control. Switched loads (on/off) can benefit from the MIC5020's fast switching times by allowing use of MOSFETs with smaller safe operating areas. (Larger MOSFETs are often required when using slower drivers.)

Overcurrent Limiting

A 50mV comparator is provided for current sensing. The low level trip point minimizes I^2R losses when power resistors are used for current sensing. Flexibility in choosing drain or source side sensing is provided by access to both SENSE + and SENSE – comparator inputs.

The adjustable retry feature can be used to handle loads with high initial currents, such as lamps, motors, or heating elements and can be adjusted from the C_T connection.

C_T to ground causes maintained gate drive shutdown following overcurrent detection.

C_T open, or through a capacitor to ground, causes automatic retry . The default duty cycle (C_T open) is approximately 20%. Refer to the electrical characteristics when selecting a capacitor for a reduced duty cycle.

C_T through a pull-up resistor to V_{DD} increases the duty cycle. *Increasing the duty cycle increases the power dissipation in the load and MOSFET.* Circuits may become unstable at a duty cycles of about 75% or higher, depending on the conditions. *Caution: The MIC5020 may be damaged if the voltage on C_T exceeds the absolute maximum rating.*

An overcurrent condition is externally signaled by an open collector (FAULT) output.

The MIC5020 may be used without current sensing by connecting SENSE + and SENSE – to ground.

Current Sense Resistors

Lead length can be significant when using low value (< 1Ω) resistors for current sensing. Errors caused by lead length can be avoided by using four-terminal current sensing resistors. Four-terminal resistors are available from several manufacturers.

Lamp Driver Application

Incandescent lamps have a high inrush current (low resistance) when turned on. The MIC5020 can perform a "soft start" by pulsing the MOSFET (overcurrent condition) until the filament is warm enough for its current to decrease (resistance increases). The sense resistor is selected so the voltage across the sense resistor drops below the sense threshold (50mV) as the filament becomes warm. The MOSFET is no longer pulsed to limit current and the lamp turns completely on.

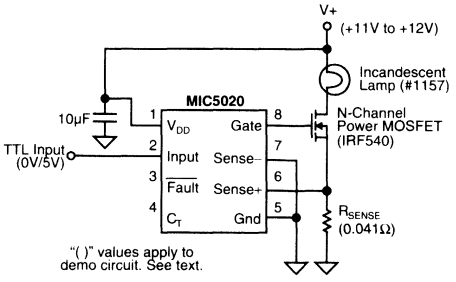


Figure 1. Lamp Driver with Current Sensing

A lamp may not fully turn on if the filament does not heat up adequately. Changing the duty cycle, sense resistor, or both to match the filament characteristics can correct the problem.

Soft start can be demonstrated using a #1157 dual-filament automotive lamp. The value of R_S shown in figure 1 allows for soft start of the higher-resistance filament (measures approx. 2.1Ω cold or 21Ω hot).

Solenoid Driver Application

The MIC5020 can be directly powered by the control voltage supply in typical 11Vdc through 50Vdc control applications. Current sensing has been omitted as an example.

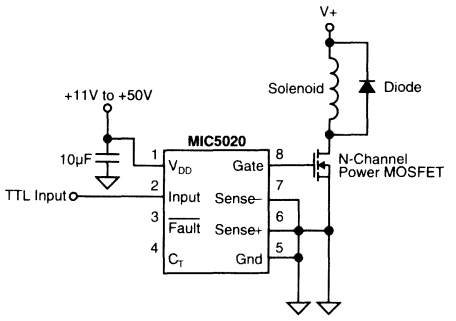


Figure 2. Solenoid Driver, Without Current Sensing

A diode across the load protects the MOSFET from the voltage spike generated by the inductive load upon MOSFET turn off. The peak forward current rating of the diode should be greater than the load current.

Current Sensing MOSFET Application

A current sensing MOSFET allows current sensing without adding additional resistance to the power switching circuit.

A current sensing MOSFET has two source connections: a "power source" for power switching and a "current source" for current sensing. The current from the current source is approximately proportional to the current through the power source, but much smaller. A current sensing ratio (I_{SOURCE}/I_{SENSE}) is provided by the MOSFET manufacturer.

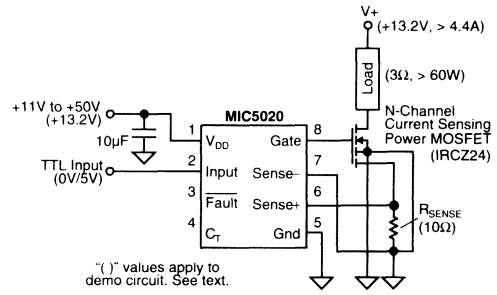


Figure 3. Using a Current Sensing MOSFET

The MOSFET current source is used to develop a voltage across a sense resistor. This voltage is monitored by the MIC5020 (SENSE + and SENSE – pins) to identify an overcurrent condition.

The value of the sense resistor can be estimated with:

$R_{SENSE} = (r\ V_{TRIP}\ R_{DS(ON)}) / (I_{LOAD}\ R_{DS(ON)} - V_{TRIP})$

where:

R_{SENSE} = external "sense" resistor

V_{TRIP} = 50mV (0.050V) for the MIC5020

r = manufacturer's current sense ratio: (I_{SOURCE}/I_{SENSE})

$R_{DS(ON)}$ = manufacturer's power source on resistance

I_{LOAD} = load current (power source current)

The drain to source voltage under different fault conditions affects the behavior of the MOSFET current source; that is, the current source will respond differently to a slight overcurrent condition ($V_{DS(ON)}$ very small) than to a short circuit (where $V_{DS(ON)}$ is approximately equal to the supply voltage). Adjustment of the sense resistor value by experiment starting from the above formula will provide the quickest selection of R_{SENSE}.

Refer to manufacture's data sheets and application notes for detailed information on current sensing MOSFET characteristics.

Figure 3 includes values which can be used to demonstrate circuit operation. The IRCZ24 MOSFET has a typical sense ratio of 780 and a $R_{DS(ON)}$ of 0.10Ω. A large 3Ω wirewound load resistor will cause inductive spikes which should be suppressed using a diode (using the same configuration as figure 2).

Faster MOSFET Switching

The MIC5020's GATE current can be multiplied using a pair of bipolar transistors to permit faster charging and discharging of the external MOSFET's gate.

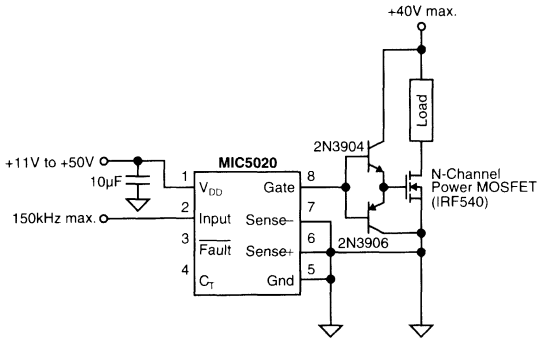


Figure 4. Faster MOSFET Switching Circuit

NPN and PNP transistors are used to respectively charge and discharge the MOSFET gate. The MIC5020 gate current is multiplied by the transistor β.

The switched circuit voltage can be increased above 40V by selecting transistors with higher ratings.

Remote Overcurrent Limiting Reset

In circuit breaker applications where the MIC5020 maintains an off condition after an overcurrent condition is sensed, the C_T pin can be used to reset the MIC5020.

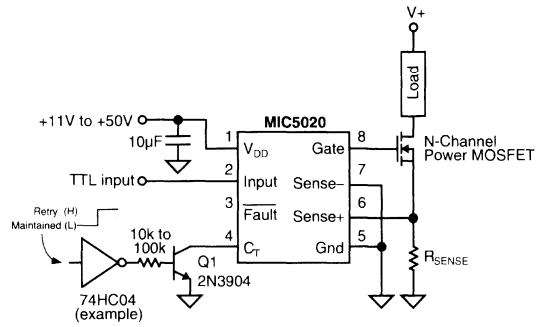


Figure 5. Remote Control Circuit

Switching Q1 on pulls C_T low which keeps the MIC5020 GATE output off when an overcurrent is sensed. Switching Q1 off causes C_T to appear open. The MIC5020 retries in about 20µs and continues to retry until the overcurrent condition is removed.

For test purposes, a 680Ω load resistor and 3Ω sense resistor will produce an overcurrent condition when the load's supply (V+) is approximately 12V or greater.

MIC5021

High-Speed High-Side MOSFET Driver

Preliminary Information

General Description

The MIC5021 high-side MOSFET driver is designed to operate at frequencies up to 100kHz and is an ideal choice for high speed applications such as motor control, SMPS (switch mode power supplies), and applications using IGBTs. The MIC5021 can also operate as a circuit breaker with or without automatic retry.

A rising or falling edge on the input results in a current source pulse or sink pulse on the gate output. This output current pulse can turn on a 2000pF MOSFET in approximately 550ns. The MIC5021 then supplies a limited current (< 2mA), if necessary, to maintain the output state. An external 0.01µF boost capacitor is required for fast turn on.

An overcurrent comparator with a trip voltage of 50mV makes the MIC5021 ideal for use with a current sensing MOSFET. An external low value resistor may be used instead of a sensing MOSFET for more precise overcurrent control. An optional external capacitor placed from the C_T pin to ground may be used to control the current shutdown duty cycle (dead time) from 20% to < 1%. A duty cycle from 20% to about 75% is possible with an optional pull-up resistor from C_T to V_{DD}.

The MIC5021 is available in 8-pin SOIC, plastic DIP and CERDIP packages.

Other members of the MIC502x family include the MIC5020 low-side driver and the MIC5022 half-bridge driver with a cross-conduction interlock.

Features

- 12V to 36V operation
- 550ns rise/fall time driving 2000pF
- TTL compatible input with internal pull-down resistor
- Overcurrent limit
- Gate to source protection
- Internal charge pump
- 100kHz operation guaranteed over full temperature and operating voltage range
- Compatible with current sensing MOSFETs
- Current source drive reduces EMI

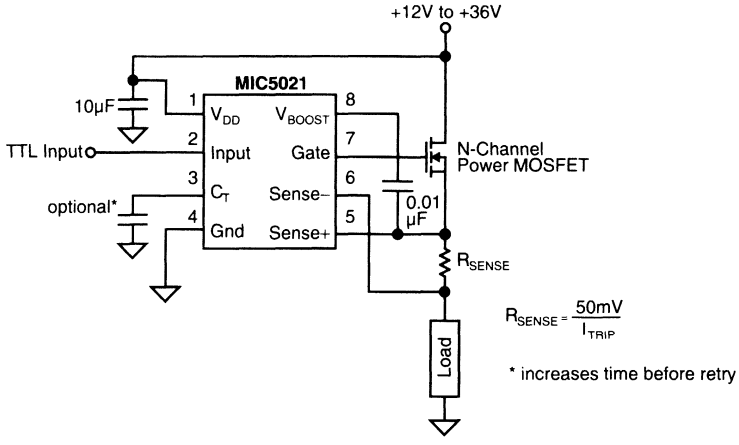
Applications

- Lamp control
- Heater control
- Motor control
- Solenoid switching
- Switch-mode power supplies
- Circuit breaker

Ordering Information

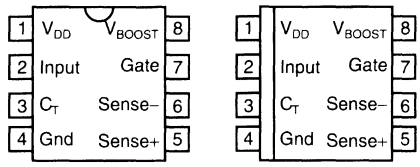
Part Number	Temperature Range	Package
MIC5021AJ	–55°C to +125°C	8-pin CerDIP
MIC5021BM	–40°C to +85°C	8-pin SOIC
MIC5021BN	–40°C to +85°C	8-pin Plastic DIP

Typical Application



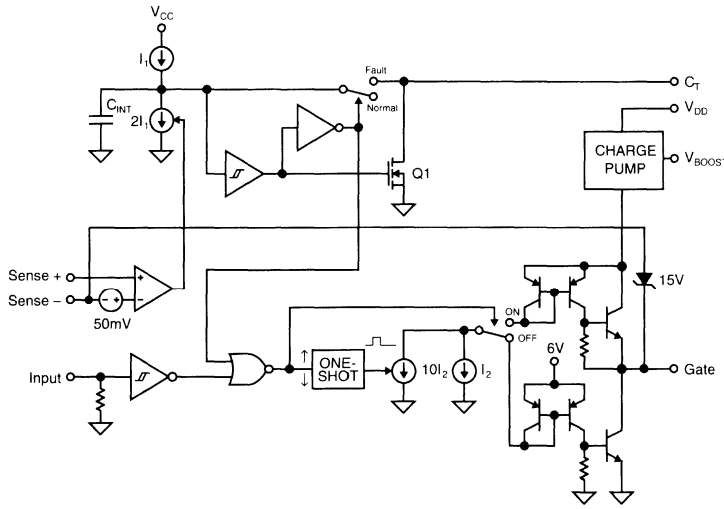
High-Side Driver with Overcurrent Trip and Retry

Pin Configuration



DIP Packages (N, J) **SOIC Package (M)**

Block Diagram



Pin Description

Pin Number	Pin Name	Pin Function
1	V_{DD}	Supply: +12V to +36V. Decouple with ≥ 10µF capacitor.
2	Input	TTL Compatible Input: Logic high turns the external MOSFET on. An internal pull-down returns an open pin to logic low.
3	C_T	Retry Timing Capacitor: Controls the off time ($t_{G(OFF)}$) of the overcurrent retry cycle. (Duty cycle adjustment.) • Open = approx. 20% duty cycle. • Capacitor to Ground = approx. 20% to < 1% duty cycle. • Pull-up resistor = approx. 20% to approx. 75% duty cycle. • Ground = maintained shutdown upon overcurrent condition.
4	Gnd	Circuit Ground
5	Sense +	Current Sense Comparator (+) Input: Connect to high side of sense resistor or current sensing MOSFET sense lead. A built-in offset in conjunction with R_{SENSE} sets the load overcurrent trip point.
6	Sense –	Current Sense Comparator (–) Input: Connect to the low side of the sense resistor (usually the high side of the load).
7	Gate	Gate Drive: Drives the gate of an external power MOSFET. Also limits V_{GS} to 15V max. to prevent Gate to Source damage. Will sink and source current.
8	V_{BOOST}	Charge Pump Boost Capacitor: A 0.01µF bootstrap capacitor from V_{BOOST} to the FET source pin supplies charge to quickly enhance the Gate output during turn-on.

Absolute Maximum Ratings

Supply Voltage (V_{DD}) ..... +36V
Input Voltage ..... –0.5V to +15V
Sense Differential Voltage ..... ±6.5V
Sense + or Sense – to Gnd ..... –0.5V to +36V
Timer Voltage (C_T) ..... +5.5V
V_{BOOST} Capacitor 0.01µF

Operating Ratings

Supply Voltage (V_{DD}) ..... +12V to +36V
Temperature Range
CerDIP ..... –55°C to +125°C
PDIP ..... –40°C to +85°C
SOIC ..... –40°C to +85°C

Electrical Characteristics

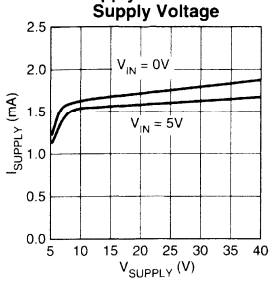
T_A = 25°C, Gnd = 0V, V_{DD} = 12V, C_T = Open, Gate C_L = 1500pF (IRF540 MOSFET) unless otherwise specified

Symbol	Parameter	Condition	Min	Typ	Max	Units
	D.C. Supply Current	V_{DD} = 12V, Input = 0V		1.8	4	mA
		V_{DD} = 36V, Input = 0V		2.5	6	mA
		V_{DD} = 12V, Input = 5V		1.7	4	mA
		V_{DD} = 36V, Input = 5V		2.5	6	mA
	Input Threshold		0.8	1.4	2.0	V
	Input Hysteresis			0.1		V
	Input Pull-Down Current	Input = 5V	10	20	40	µA
	Current Limit Threshold	**Note 1**	30	50	70	mV
	Gate On Voltage	V_{DD} = 12V **Note 2**	16	18	21	V
		V_{DD} = 36V **Note 2**	46	50	52	V
$t_{G(ON)}$	Gate On Time, Fixed	Sense Differential > 70mV	2	6	10	µs
$t_{G(OFF)}$	Gate Off Time, Adjustable	Sense Differential > 70mV, C_T = 0pF	10	20	50	µs
t_{DLH}	Gate Turn-On Delay	**Note 3**		500	1000	ns
t_R	Gate Rise Time	**Note 4**		400	500	ns
t_{DLH}	Gate Turn-Off Delay	**Note 5**		800	1500	ns
t_F	Gate Fall Time	**Note 6**		400	500	ns
f_{max}	Maximum Operating Frequency	**Note 7**	100	150		kHz

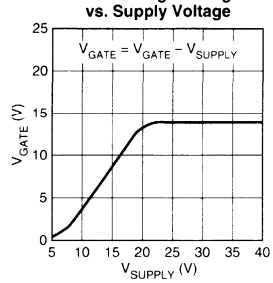
Note 1 When using sense MOSFETs, it is recommended that R_{SENSE} < 50Ω. Higher values may affect the sense MOSFET's current transfer ratio.
Note 2 DC measurement.
Note 3 Input switched from 0.8V (TTL low) to 2.0V (TTL high), time for Gate transition from 0V to 2V.
Note 4 Input switched from 0.8V (TTL low) to 2.0V (TTL high), time for Gate transition from 2V to 17V.
Note 5 Input switched from 2.0V (TTL high) to 0.8V (TTL low), time for Gate transition from 20V (Gate on voltage) to 17V.
Note 6 Input switched from 2.0V (TTL high) to 0.8V (TTL low), time for Gate transition from 17V to 2V.
Note 7 Frequency where gate on voltage reduces to 17V with 50% input duty cycle.

Typical Characteristics

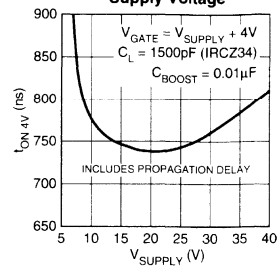
Supply Current vs. Supply Voltage



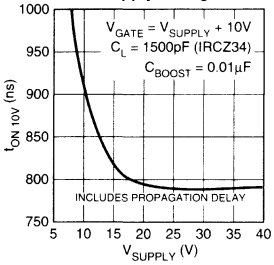
Gate Voltage Change vs. Supply Voltage



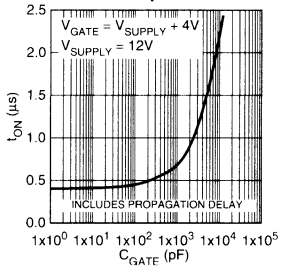
Gate Turn-On Delay vs. Supply Voltage



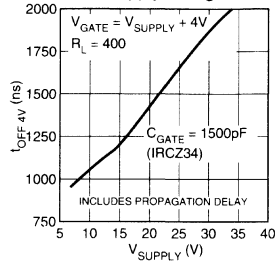
Gate Turn-On Delay vs. Supply Voltage



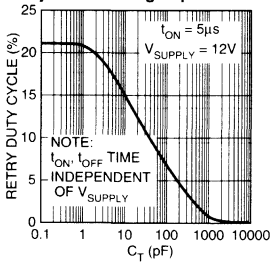
Gate Turn-On Delay vs. Gate Capacitance



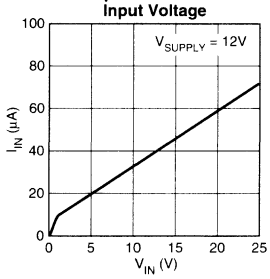
Gate Turn-Off Delay vs. Supply Voltage



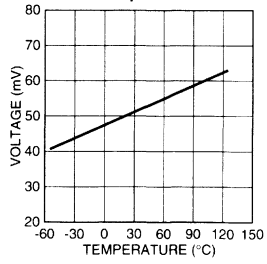
Overcurrent Retry Duty Cycle vs. Timing Capacitance

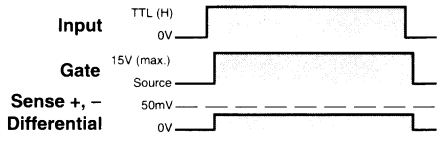


Input Current vs. Input Voltage

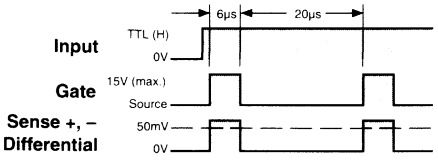


Sense Threshold vs. Temperature

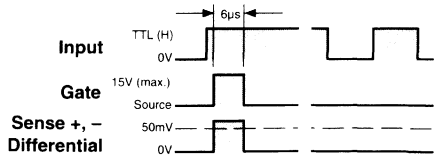




Timing Diagram 1. Normal Operation



Timing Diagram 2. Fault Condition, C_T = Open



Timing Diagram 3. Fault Condition, C_T = Grounded

Functional Description

Refer to the MIC5021 block diagram.

Input

A signal greater than 1.4V (nominal) applied to the MIC5021 INPUT causes gate enhancement on an external MOSFET turning the MOSFET on.

An internal pull-down resistor insures that an open INPUT remains low, keeping the external MOSFET turned off.

Gate Output

Rapid rise and fall times on the GATE output are possible because each input state change triggers a one-shot which activates a high-value current sink ($10I_2$) for a short time. This draws a high current though a current mirror circuit causing the output transistors to quickly charge or discharge the external MOSFET's gate.

A second current sink continuously draws the lower value of current used to maintain the gate voltage for the selected state.

An internal charge pump utilizes an external "boost" capacitor connected between V_{BOOST} and the source of the external MOSFET. (Refer to typical application.) The boost capacitor stores charge when the MOSFET is off. As the MOSFET turns on, its source to ground voltage increases and is added to the voltage across the capacitor, raising the V_{BOOST} pin voltage. The boost capacitor charge is directed through the GATE pin to quickly charge the MOSFET's gate to 16V maximum above V_{DD}. The internal charge pump maintains the gate voltage.

An internal Zener diode protects the external MOSFET by limiting the gate to source voltage.

Overcurrent Limiting

Current source I_1 charges C_{INT} upon power up. An optional external capacitor connected to C_T is kept discharged through a MOSFET Q1.

A fault condition (> 50mV from SENSE + to SENSE –) causes the overcurrent comparator to enable current sink $2I_1$ which overcomes current source I_1 to discharge C_{INT} in a short time. When C_{INT} is discharged, the INPUT is disabled, which turns off the gate output, and C_{INT} and C_T are ready to be charged.

When the gate output turns the MOSFET off, the overcurrent signal is removed from the sense inputs which deactivates current sink $2I_1$. This allows C_{INT} and the optional capacitor connected to C_T to recharge. A Schmitt trigger delays the retry while the capacitor(s) recharge. Retry delay is increased by connecting a capacitor to C_T (optional).

The retry cycle will continue until the fault is removed or the input is changed to TTL low.

If C_T is connected to ground, the circuit will not retry upon a fault condition.

Applications Information

The MIC5021 MOSFET driver is intended for high-side switching applications where overcurrent limiting and high speed are required. The MIC5021 can control MOSFETs that switch voltages up to 36V.

Supply Voltage

The MIC5021's supply voltage rating is up to 36V. For proper gate enhancement, the MIC5021's supply voltage should be equal to the MOSFET's drain voltage.

The minimum supply voltage required to effectively enhance an N-channel MOSFET is 12V.

High-Side Switch Circuit Advantages

High-side switching allows more of the load related components and wiring to remain near ground potential when compared to low-side switching. This reduces the chances of short-to-ground accidents or failures.

Speed Advantage

The MIC5021 is about two orders of magnitude faster than the low cost MIC5014 making it suitable for high-frequency high-efficiency circuit operation in PWM (pulse width modulation) designs used for motor control, SMPS (switch mode power supply) and heating element control.

Switched loads (on/off) benefit from the MIC5021's fast switching times by allowing use of MOSFETs with smaller safe operating areas. (Larger MOSFETs are often required when using slower drivers.)

Overcurrent Limiting

A 50mV comparator is provided for current sensing. The low level trip point minimizes I^2R losses when a power resistor is used for current sensing.

The adjustable retry feature can be used to handle loads with high initial currents, such as lamps or heating elements, and can be adjusted from the C_T connection.

C_T to ground causes maintained gate drive shutdown following an overcurrent condition.

C_T open, or a capacitor to ground, causes automatic retry. The default duty cycle (C_T open) is approximately 20%. Refer to the electrical characteristics when selecting a capacitor for a reduced duty cycle.

C_T through a pull-up resistor to V_{DD} increases the duty cycle. *Increasing the duty cycle increases the power dissipation in the load and MOSFET under a "fault" condition.* Circuits may become unstable at a duty cycle of about 75% or higher, depending on conditions. *Caution: The MIC5021 may be damaged if the voltage applied to C_T exceeds the absolute maximum voltage rating.*

Boost Capacitor Selection

The boost capacitor should be 0.01µF. Larger capacitors can damage the MIC5021.

Current Sense Resistors

Lead length can be significant when using low value (< 1Ω) resistors for current sensing. Errors caused by lead length can be avoided by using four-teminal current sensing resistors. Four-terminal resistors are available from several manufacturers.

Circuits Without Current Sensing

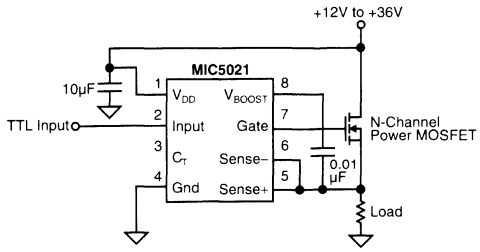


Figure 1. Current Sensing Omitted

Current sensing may be omitted by connecting the SENSE + and SENSE – pins to the source of the MOSFET. Do not connect the SENSE pins to ground.

Lamp Driver Application

Incandescent lamps have a high inrush current (low resistance) when turned on. The MIC5021 can perform a "soft start" by pulsing the MOSFET (overcurrent condition) until the filament is warm and its current decreases (resistance increases). The sense resistor value is selected so the voltage drop across the sense resistor decreases below the sense threshold (50mV) as the filament becomes warm. The FET is no longer pulsed and the lamp turns completely on.

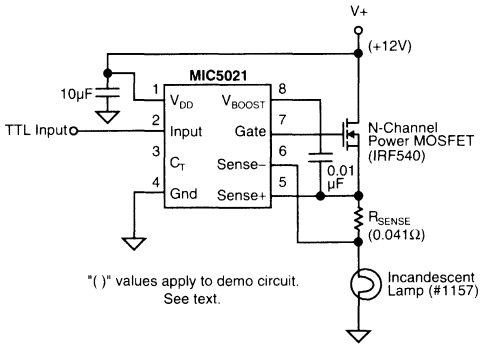


Figure 2. Lamp Driver with Current Sensing

A lamp may not fully turn on if the filament does not heat up adequately. Changing the duty cycle, sense resistor, or both to match the filament characteristics can correct the problem.

Soft start can be demonstrated using a #1157 dual filament automotive lamp. The value of R_S shown in figure 2 allows for soft start of the higher-resistance filament (measures approx. 2.1Ω cold or 21Ω hot).

Inductive Load Precautions

Circuits controlling inductive loads, such as solenoids (figure 3) and motors, require precautions when controlled by the MIC5021. Wire wound resistors, which are sometimes used to simulate other loads, can also show significant inductive properties.

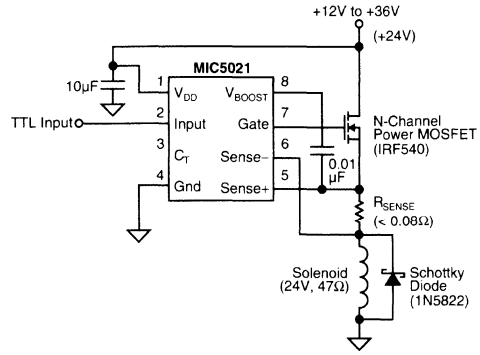


Figure 3. Solenoid Driver with Current Sensing

An inductive load releases stored energy when its current flow is interrupted (when the MOSFET is switched off). The voltage across the inductor reverses and the inductor attempts to force current flow. Since the circuit appears open (the MOSFET appears as a very high resistance) a very large voltage occurs across the inductor. Unless limited, this inductive spike can cause unpredictable circuit behavior and damage the MIC5021 and/or MOSFET.

Limiting Inductive Spikes

The voltage across the inductor can be limited by connecting a diode across the load. The diode is forward biased only when the load is switched off. A Schottky diode is recommended for low-side sensing applications (figure 3) because of its low forward voltage drop. When selecting a Schottky diode to protect the MIC5021 in low-side sensing applications, its forward drop at the load current should be determined from the manufacturer's data. Larger Schottky diodes maintain lower forward voltage drops at higher currents. The forward voltage drop should not exceed approximately 0.5V.

The diode should have a peak forward current rating greater than the load current. This is because the current through the diode is the same as the load current at the instant the MOSFET is turned off.

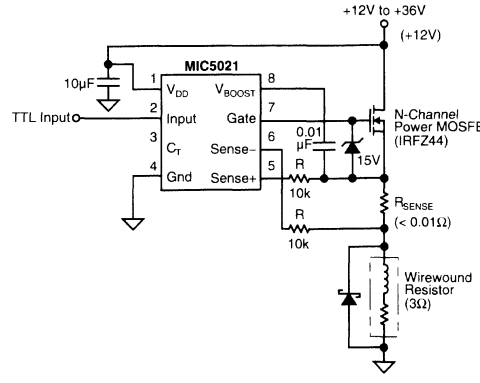


Figure 4. Resistor Placement

Sense Pin Considerations

The sense pins of the MIC5021 are sensitive to negative voltages. If a voltage spike is too negative (below approximately –0.5V), current will be drawn from functional sections of the IC resulting in unpredictable circuit behavior or damage.

Resistors may be used to isolate the sense pins from the load (figure 4). The resistors limit current draw from the sense pins during negative spikes. Limiting the current to less than approximately 600µA allows internal Schottky diodes to protect the MIC5021's functional circuitry.

During normal operation, almost no current flows into the sense pins. This means the resistors cause negligible voltage drop and do not degrade the sense measurement.

Connecting a resistor to SENSE + makes the MIC5021's internal gate to source Zener diode ineffective. When a resistor is used, an external 15V Zener diode should be connected between the gate and source of the MOSFET.

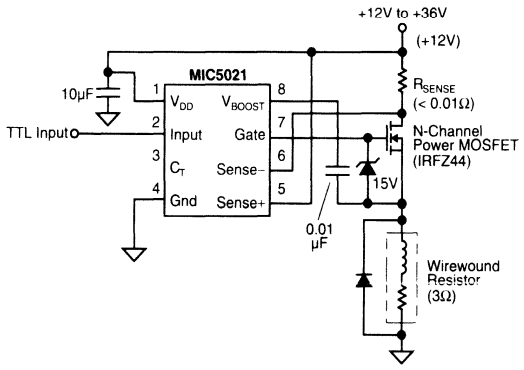


Figure 5. High Side Sensing

High-Side Sensing

Sensing the current on the high side of the MOSFET locates the SENSE pins away from the inductive spike.

Remote Overcurrent Limiting Reset

In circuit breaker applications where the MIC5021 maintains an off condition after an overcurrent condition is sensed, the C_T pin can be used to reset the MIC5021.

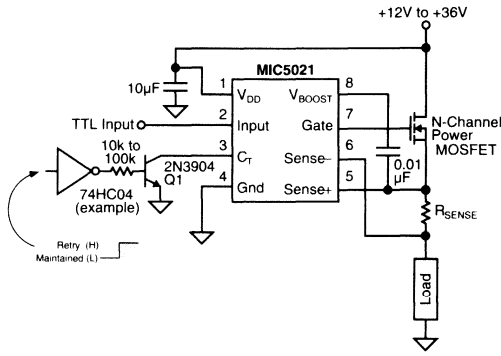


Figure 6. Remote Control Circuit

Switching Q1 on pulls C_T low which keeps the MIC5021 GATE output off when an overcurrent is sensed. Switching Q1 off causes C_T to appear open. The MIC5021 retries in about 20µs and continues to retry until the overcurrent condition is removed.

For test purposes, a 680Ω load resistor and 3Ω sense resistor will produce an overcurrent condition when the load's supply (V+) is approximately 12V or greater.

2

MIC5022

Half-Bridge MOSFET Driver

Preliminary Information

General Description

The MIC5022 half-bridge MOSFET driver is designed to operate at frequencies up to 100kHz and is an ideal choice for high speed applications such as motor control and SMPS (switch mode power supplies).

A rising or falling edge on the input results in a current source pulse or sink pulse on the gate outputs. This output current pulse can turn on a 2000pF MOSFET in approximately 1μs. The MIC5022 then supplies a limited current (< 2mA), if necessary, to maintain the output states. An external 0.01μF boost capacitor is required for fast turn on.

Two overcurrent comparators with nominal trip voltages of 50mV make the MIC5022 ideal for use with current sensing MOSFETs. External low value resistors may be used instead of sensing MOSFETs for more precise overcurrent control. Optional external capacitors placed on the C_{TH} and C_{TL} pins may be used to individually control the current shutdown duty cycles from approximately 20% to <1%. Duty cycles from 20% to about 75% are possible with individual pull-up resistors from C_{TL} and C_{TH} to V_{DD}. An open collector output provides a fault indication when either sense input is tripped.

The MIC5022 is available in 16-pin surface mount and 14-pin plastic DIP and CerDIP packages.

Other members of the MIC502x family include the MIC5020 low-side driver and the MIC5021 high-side driver.

Features

- 12V to 36V operation
- 600ns rise time into 1000pF (high side)
- TTL compatible input with internal pull-down resistor
- Outputs interlocked to prevent cross conduction
- TTL compatible enable
- Fault output indication
- Individual overcurrent limits
- Gate protection
- Internal charge pump (high-side)
- Current source drive scheme reduces EMI

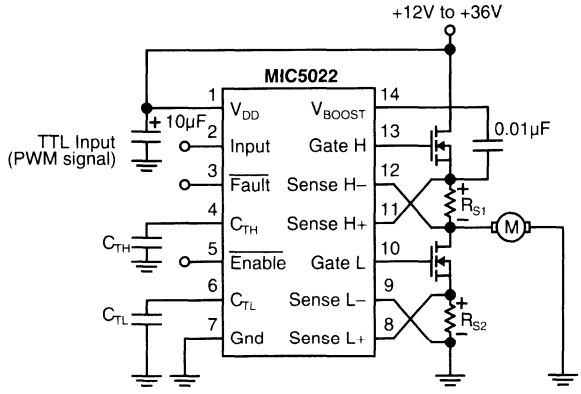
Applications

- Motor control
- Switch-mode power supplies

Ordering Information

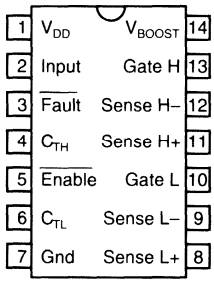
Part Number	Temperature Range	Package
MIC5022AJ	–55°C to +125°C	14-pin CerDIP
MIC5022BWM	–40°C to +85°C	16-pin Wide SOIC
MIC5022BN	–40°C to +85°C	14-pin Plastic DIP

Typical Application

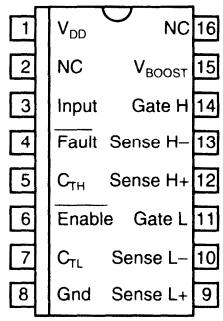


DC Motor Control Application

Pin Configuration



DIP Packages (N, J)

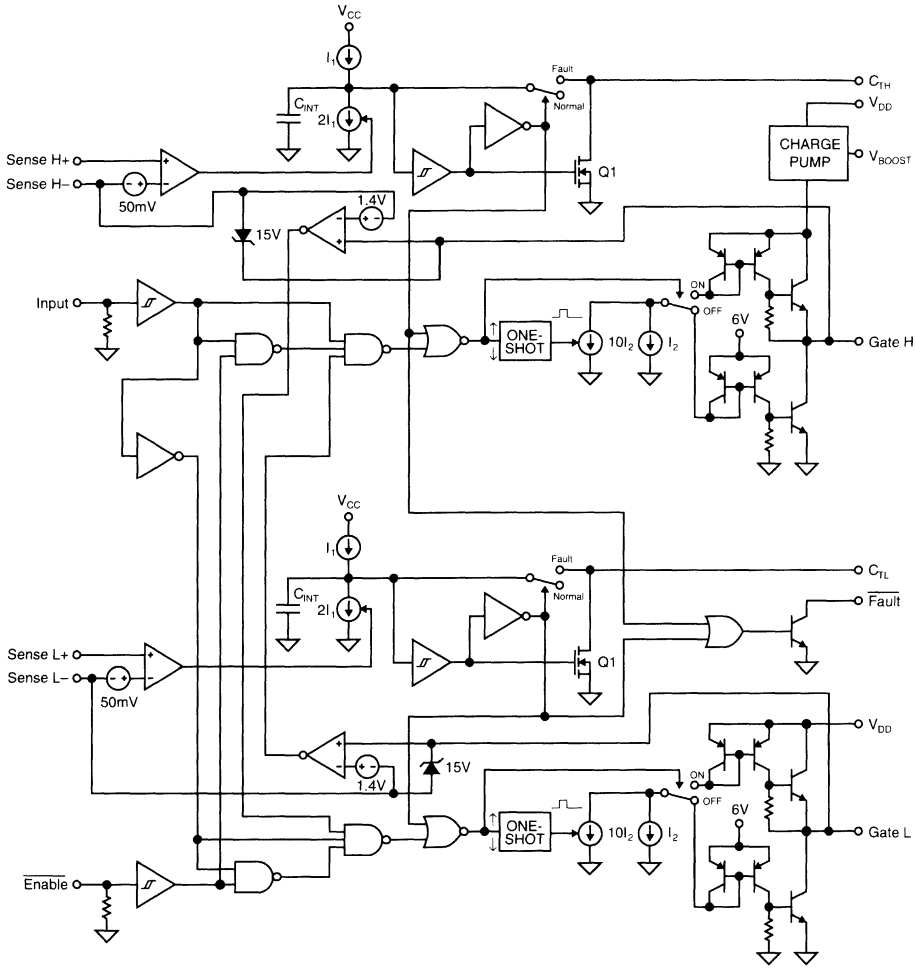


SOIC Package (WM)

Pin Description

DIP Pin No.	SOIC Pin No.	Pin Name	Pin Function
1	1	V_{DD}	Supply: +12V to +36V. Decouple with ≥ 10µF capacitor.
2	3	Input	TTL Compatible Input: Logic high turns the high-side external MOSFET on and the low-side external MOSFET off. Logic low turns the high-side external MOSFET off and the low-side external MOSFET on. An internal pull-down returns an open pin to logic low.
3	4	$\overline{Fault}$	When either sense voltage exceeds threshold, open collector output is open circuit for 5µs ($t_{G(ON)}$), then pulled low for $t_{G(OFF)}$. $t_{G(OFF)}$ is adjustable from C_T.
4	5	C_{TH}	Retry Trimming Capacitor, High Side: Controls the off time ($t_{G(OFF)}$) of the overcurrent retry cycle. (Duty cycle adjustment.) • Open = approx. 20% duty cycle. • Capacitor to Ground = approx. 20% to < 1% duty cycle. • Pullup resistor = approx. 20% to approx. 75% duty cycle. • Ground = maintained shutdown upon overcurrent condition.
5	6	$\overline{Enable}$	Output Enable: Disables operation of the output drivers; active high. An internal pull-down returns an open pin to logic low.
6	7	C_{TL}	Retry Trimming Capacitor, Low Side: Same function as C_{TH}.
7	8	Gnd	Circuit Ground
8	8	Sense L +	Current Sense Comparator (+) Input, Low Side: Connect to source of low-side MOSFET. A built-in offset (nominal 50mV) in conjunction with R_{SENSE} sets the load overcurrent trip point.
9	10	Sense L –	Current Sense Comparator (–) Input, Low Side: Connect to the negative side of the low-side sense resistor.
10	11	Gate L	Gate Drive, Low Side: Drives the gate of an external power MOSFET. Also limits V_{GS} to 15V max. to prevent Gate to Source damage. Will sink and source current.
11	12	Sense H +	Current Sense Comparator (+) Input, High Side: Connect to source of high-side MOSFET. A built-in offset (nominal 50mV) in conjunction with R_{SENSE} sets the load overcurrent trip point.
12	13	Source H –	Current Sense Comparator (–) Input, High Side: Connect to the negative side of the high-side sense resistor.
13	14	Gate H	Gate Drive, High Side: Drives the gate of an external power MOSFET. Also limits V_{GS} to 15V max. to prevent Gate to Source damage. Will sink and source current.
14	15	V_{BOOST}	Charge Pump Boost Capacitor: A 0.01µF bootstrap capacitor from V_{BOOST} to the MOSFET source pin supplies charge to quickly enhance the external MOSFET's gate .

Block Diagram



Absolute Maximum Ratings

Supply Voltage (V_{DD}) ..... +36V
Input Voltage ..... –0.5V to 15V
Sense Differential Voltage ..... ±6.5V
Sense + or Sense – to Gnd ..... –0.5V to +36V
$\overline{Fault}$ Voltage ..... +36V
Current into $\overline{Fault}$ 50mA
Timer Voltage (C_T) ..... +5.5V
V_{BOOST} Capacitor 0.01µF

Operating Ratings

Supply Voltage (V_{DD}) ..... +12V to +36V
Temperature Range
CerDIP ..... –55°C to +125°C
SOIC ..... –40°C to +85°C
PDIP ..... –40°C to +85°C

Electrical Characteristics

T_A = 25°C, Gnd = 0V, V_{DD} = 12V, Gate C_L = 1500pF (IRF540 MOSFET) unless otherwise specificed

Symbol	Parameter	Condition	Min	Typ	Max	Units
	D.C. Supply Current	V_{DD} = 12V, Input = 0V		2.5	5	mA
		V_{DD} = 36V, Input = 0V		6.0	10	mA
		V_{DD} = 12V, Input = 5V		2.4	5	mA
		V_{DD} = 36V, Input = 5V		3.0	25	mA
	Input Threshold		0.8	1.4	2.0	V
	Input Hysteresis			0.1		V
	Input Pull-Down Current	Input = 5V	10	20	40	µA
	Enable Threshold		0.8	1.4	2.0	V
	Enable Hysteresis			0.1		V
	Fault Output Saturation Voltage	Fault Current = 1.6mA **Note 1**		0.15	0.4	V
	Fault Output Leakage	Fault = 36V	–1	0.01	+1	µA
	Current Limit Thresh., Low-Side	**Note 2**	30	50	70	mV
	Current Limit Thresh., High-Side	**Note 2**	30	50	70	mV
	Gate On Voltage, High-Side	V_{DD} = 12V, **Note 3**	16	18	21	V
		V_{DD} = 36V, **Note 3**	46	49	52	V
	Gate On Voltage, Low-Side	V_{DD} = 12V, **Note 3**	10	11		V
		V_{DD} = 36V, **Note 3**	14	15	18	V
$t_{G(ON)}$	Gate On Time, Fixed	Sense Differential > 70mV	2	5	10	µs
$t_{G(OFF)}$	Gate Off Time, Adjustable	Sense Differential > 70mV, C_T = 0pF	10	20	50	µs
t_{DLH}	Gate Turn-On Delay, High-Side	**Note 4**		1.4	2.0	µs
t_R	Gate Rise Time, High-Side	**Note 5**		0.8	1.5	µs
t_{DHL}	Gate Turn-Off Delay, High-Side	**Note 6**		1.2	2.0	µs
t_F	Gate Fall Time, High-Side	**Note 7**		0.6	1.5	µs
t_{DLH}	Gate Turn-On Delay, Low-Side	**Note 4**		1.7	2.5	µs
t_R	Gate Rise Time, Low-Side	**Note 8**		0.7	1.5	µs
t_{DHL}	Gate Turn-Off Delay, Low-Side	**Note 9**		0.5	1.0	µs
t_F	Gate Fall Time, Low-Side	**Note 10**		1.0	1.5	µs

Note 1 Voltage remains low for time affected by C_T.

Note 2 When using sense MOSFETs, it is recommended that R_{SENSE} < 50Ω. Higher values may affect the sense MOSFET's current transfer ratio.

Note 3 DC measurement.

Note 4 Input switched from 0.8V (TTL low) to 2.0V (TTL high), time for Gate transition from 0V to 2V.

Note 5 Input switched from 0.8V (TTL low) to 2.0V (TTL high), time for Gate transition from 2V to 17V.

Note 6 Input switched from 2.0V (TTL high) to 0.8V (TTL low), time for Gate transition from 20V (Gate on voltage) to 17V.

Note 7 Input switched from 2.0V (TTL high) to 0.8V (TTL low), time for Gate transition from 17V to 2V.

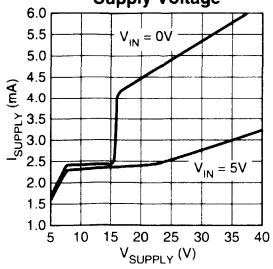
Note 8 Input switched from 0.8V (TTL low) to 2.0V (TTL high), time for Gate transition from 2V to 10V.

Note 9 Input switched from 2.0V (TTL high) to 0.8V (TTL low), time for Gate transition from 15V (Gate on voltage) to 10V.

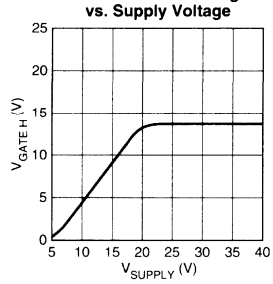
Note 10 Input switched from 2.0V (TTL high) to 0.8V (TTL low), time for Gate transition from 10V to 2V.

Typical Characteristics

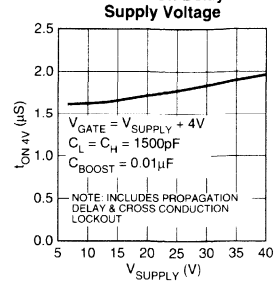
Supply Current vs. Supply Voltage



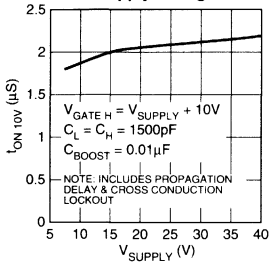
Gate to Source Voltage vs. Supply Voltage



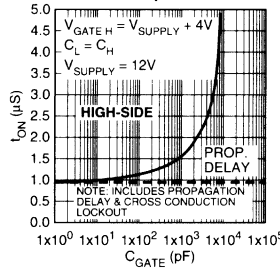
Gate Turn-On Delay vs. Supply Voltage



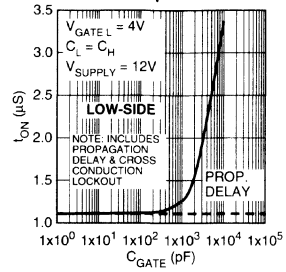
Gate Turn-On Delay vs. Supply Voltage



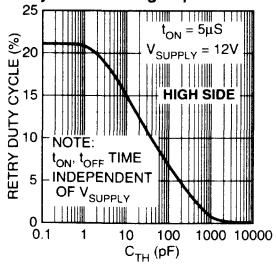
Gate Turn-On/Off Delay vs. Gate Capacitance



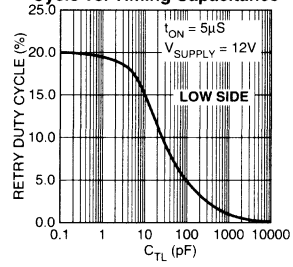
Gate Turn-On/Off Delay vs. Gate Capacitance



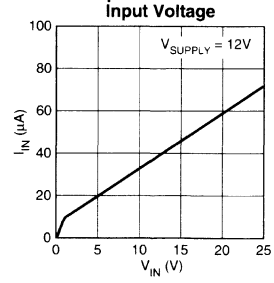
Overcurrent Retry Duty Cycle vs. Timing Capacitance



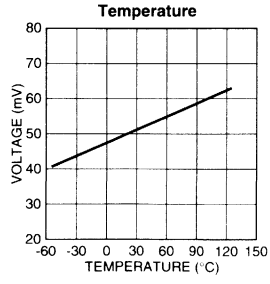
Overcurrent Retry Duty Cycle vs. Timing Capacitance

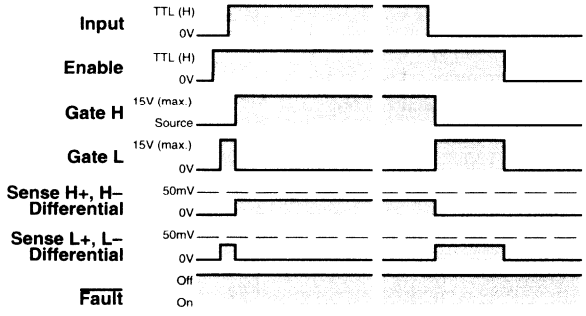


Input Current vs. Input Voltage

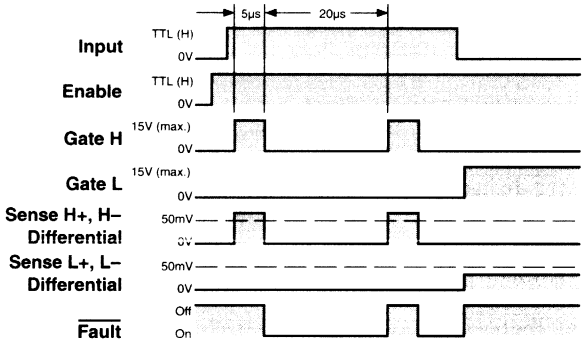


Sense Threshold vs. Temperature

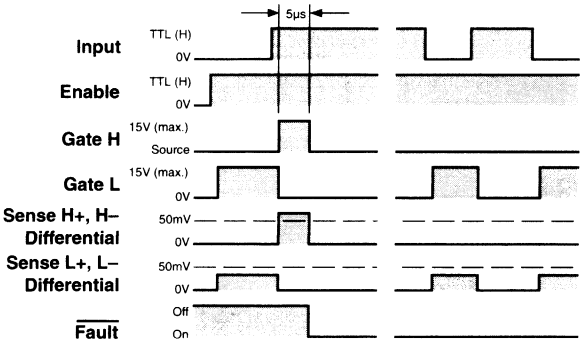




Timing Diagram 1. Normal Operation



Timing Diagram 2. Overcurrent Fault with Retry



Timing Diagram 3. Overcurrent Fault with Maintained Off

Functional Description

Refer to the MIC5022 block diagram.

Input

A signal greater than 1.4V (nominal) applied to the MIC5022 INPUT causes gate enhancement on an external MOSFET connected to GATE H turning the high-side MOSFET on.

At the same time internal logic removes gate enhancement from an external MOSFET connected to GATE L, turning the low-side MOSFET off.

An internal pull-down resistor insures that an open INPUT remains low, keeping the external high-side MOSFET turned off and the low-side MOSFET turned on.

Enable

A signal greater than 1.4V (nominal) applied to the MIC5022 ENABLE keeps both GATE outputs off. An internal pull-down resistor insures that the MIC5022 is enabled if the pin is open.

Gate Outputs

Rapid rise and fall times on the GATE output are possible because each input state change triggers a one-shot which activates a high-value current sink ($10I_2$) for a short time. This draws a high current though a current mirror circuit causing the output transistors to quickly charge or discharge the external FET's gate.

A second current sink continuously draws the lower value of current used to maintain the gate voltage for the selected state.

Internal 15V Zener diodes protect the external high-side and low-side MOSFETs by limiting the gate to source voltage.

Charge Pump (High-Side)

An internal charge pump utilizes an external "boost" capacitor connected between V_{BOOST} and the source of the external FET (refer to Typical Application). The boost capacitor stores charge when the FET is off. As the FET begins to turn on the voltage on the source side of the capacitor increases (because it is on the high side of the load) raising the V_{BOOST} pin voltage. The boost capacitor charge is directed through the gate pin to quickly charge the FET's gate to 15V maximum above V_{DD}. The internal charge pump maintains the gate voltage by supplying a small current as needed.

Overcurrent Limiting (High or Low-Side)

Current source I_1 charges C_{INT} upon power up. An optional external capacitor connected to C_T is kept discharged through a FET Q1.

A fault condition (> 50mV from SENSE + to SENSE –) causes the overcurrent comparator to enable current sink $2I_1$ which overcomes current source I_1 to discharge C_{INT} in about 5µs time. When C_{INT} is discharged, the INPUT is disabled, the FAULT output is enabled, and C_{INT} and C_T are ready to be charged. Since the INPUT is disabled the GATE output turns off.

When the GATE output turns off the FET, the overcurrent signal is removed from the sense inputs which deactivates current sink $2I_1$. This allows C_{INT} and the optional capacitor connected to C_T to recharge. A Schmitt trigger delays the retry while the capacitor(s) recharge. Retry delay is increased by connecting a capacitor connected to C_T (optional).

The MIC5022's low-side driver may be used without current sensing by grounding both SENSE + and SENSE – pins. The high-side driver may be used without current sensing by connecting SENSE + and SENSE – to the source of the external high-side MOSFET.

Fault Output

The FAULT output is an open collector transistor. FAULT is active at approximately the same time the output is disabled by a fault condition (5µs after an overcurrent condition is sensed). The FAULT output is open circuit (off) during each successive retry (5µs).

Typical Full-Bridge Application

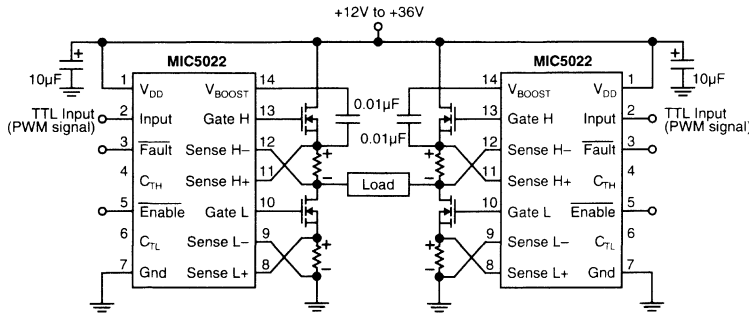


Figure 1. Basic Full-Bridge Circuit

Applications Information

The MIC5022 MOSFET driver is designed for half-bridge switching applications where overcurrent limiting and high speed are required. The MIC5022 can control MOSFETs that switch voltages up to 36V.

The MIC5022 is functionally a MIC5020 low-side driver and MIC5021 high-side driver with additional circuitry to coordinate the operation of the high and low-side drivers. Since most output considerations are similar, *refer to the MIC5020 and MIC5021 data sheets for additional applications information.*

Supply Voltage

The MIC5022's supply voltage rating is up to 36V. For proper high-side gate enhancement, the MIC5021's supply voltage should be equal to the high-side MOSFET's drain voltage.

The minimum supply voltage required to effectively enhance an N-channel MOSFET is 12V.

Overcurrent Limiting

Separate high and low-side 50mV comparators are provided for current sensing. The low level trip point minimizes I^2R losses when a power resistor is used for current sensing.

The adjustable retry feature can be used to handle loads with high initial currents, such as lamps or heating elements, and can be adjusted from the C_T connection.

C_T to ground causes maintained gate drive shutdown following an overcurrent condition.

C_T open, or a capacitor to ground, causes automatic retry. The default duty cycle (C_T open) is approximately 20% (the high side is slightly greater than the low side). Refer to the typical characteristics when selecting a capacitor for a reduced duty cycle.

C_T through a pull-up resistor to V_{DD} increases the duty cycle. *Increasing the duty cycle increases the power dissipation in the load and MOSFET under a "fault" condition.* Circuits may become unstable at a duty cycle of about 75% or higher, depending on conditions. *Caution: The MIC5022 may be damaged if the voltage applied to C_T exceeds the absolute maximum voltage rating.*

Boost Capacitor Selection

The boost capacitor should be 0.01µF. Larger capacitors can damage the MIC5021.

Circuits Without Current Sensing

Current sensing may be omitted by connecting the high-side SENSE + and SENSE – pins to the source of the MOSFET and the low-side SENSE + and SENSE – pins to ground. Do not connect the high-side sense pins to ground.

Inductive Load Precautions

Circuits controlling inductive loads require precautions when controlled by the MIC5022. Wire wound resistors, which are sometimes used to simulate other loads, can also show significant inductive properties.

Sense Pin Considerations

The sense pins of the MIC5022 are sensitive to negative voltages. If a voltage spike is too negative (below approximately –0.5V), current will be drawn from functional sections of the IC resulting in unpredictable circuit behavior or damage. Resistors may be used to isolate the sense pins from the load. Refer to the MIC5021 data sheet for details.

High-Side Sensing

For the high-side driver, sensing the current on the supply side of the high-side MOSFET locates the SENSE pins away from the inductive spike. Refer to the MIC5021 data sheet for details.

Full-Bridge Motor Control

An application for two MIC5022s is the full-bridge motor control circuit.

Two high or two low-side sense inputs may be used for overcurrent detection. (Low-side sensing is shown in figure 2). Sensing at four locations is usually unnecessary.

When switching inductive loads, such as motors, it is desirable to place the high-side sense inputs on the supply side of the MOSFETs. The helps prevent the inductive spikes that occur upon load shutoff from affecting the sense inputs. External Zener diodes take over the function of the internal GATE to SENSE – diodes (gate to source protection diodes).

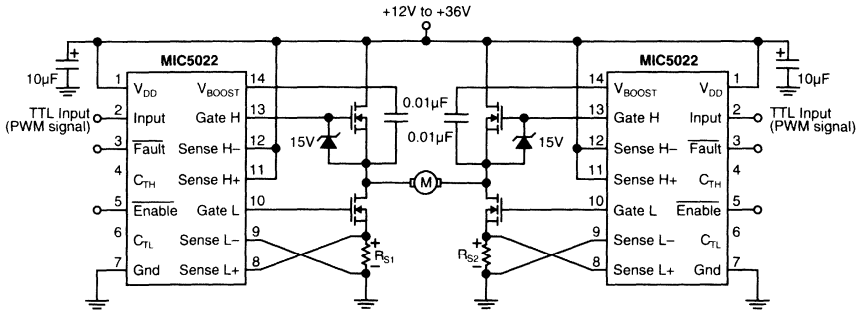


Figure 2. Full-Bridge Motor Control Application

Synchronous Rectifier Converter

The MIC5022 can be part of a synchronous rectifier in SMPS (switch mode power supply) applications.

This circuit uses the MIC38C43 SMPS controller IC to switch a pass transistor (Q1) and a "synchronous rectifier" transistor (Q2) using the MIC5022.

The MIC38C43 controller switches the transistors at 50kHz. Output regulation is maintained using PWM. When the pass transistor is on, the synchronous rectifier is off and current is forced through the inductor to the output capacitor and load. When the pass transistor is switched off, the synchronous rectifier is switched on allowing current to continue to flow as the inductor returns stored energy.

The synchronous rectifier MOSFET has a lower voltage drop than the forward voltage drop across a Schottky diode. This increases converter efficiency which extends battery life in portable equipment.

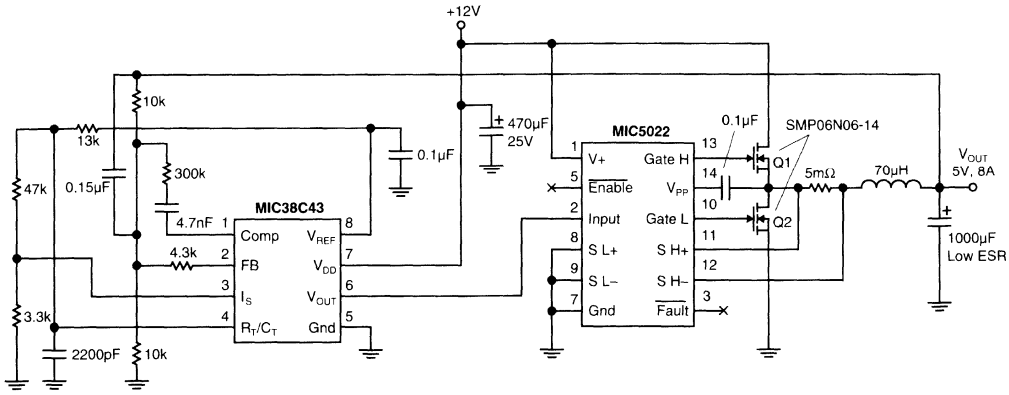


Figure 3. 50kHz Synchronous Rectifier Converter

Application Note 1

MIC5011 Design Techniques

by Mitchell Lee

Introduction

Power MOSFETs are often preferred over bipolar transistors as high current switches. In static switching applications the MOSFET takes no drive power, where a bipolar transistor requires a large base current. Bipolar transistors also exhibit inferior SOA when compared to power MOSFETs. In high side switching circuits N-channel MOSFETs are preferred over P-channel devices owing to the lower cost of an N-channel device for a given "on" resistance. Unfortunately, N-channel MOSFETs are not well-suited in high-side switch applications because in order to fully enhance the MOSFET, the gate must be driven to a potential higher than the drain supply. While a separate supply could be used for the gate drive circuitry, this is unnecessary if a charge pump is used to drive the MOSFET's gate.

A simple charge pump voltage doubler is shown in Figure 1. The object is to charge C1 from the supply, and then transfer its charge to C2. Since C2 is referred to V_{DD}, V_{OUT} will be greater than V_{DD}.

The switch is first connected to ground, charging C1 (through D1) to the supply voltage. Next, the switch is toggled to supply. C1 dumps its charge through D2 into C2. If the process is repeated, C2 will eventually charge to a potential equal to V_{DD}, lifting V_{OUT} to 2 x V_{DD} (neglecting switch and diode losses). If V_{OUT} is used to drive the gate of an N-channel MOSFET, the device will be enhanced by an amount equal to V_{DD}. A similar technique is employed by the MIC5011 high side MOSFET pre-driver to enhance an N-channel MOSFET without the need for a second supply.

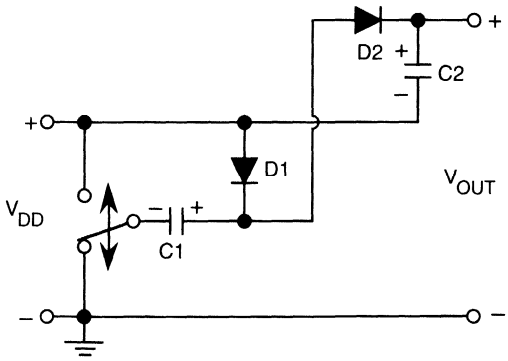


Figure 1. Charge Pump Voltage Doubler

The MIC5011

A simplified block diagram of the MIC5011 is shown in Figure 2. The charge pump is configured as a tripler, and operates at a 100 kHz rate. The oscillator is enabled by the control logic to turn the MOSFET on. For supplies greater than 13V the charge pump can develop in excess of 20V gate drive–more than the average power MOSFET can safely handle. A clamp is included on-chip to limit the gate drive to approximately 12.5V. Figure 3 shows gate drive as a function of supply voltage.

Turning the MOSFET off involves more than just stopping the charge pump oscillator: charge stored on the gate of the MOSFET must be dumped by an active pull-down. The pull-down is turned off when the MIC5011 is commanded to turn the power MOSFET back on.

Small charge pump capacitors (≈100pF) are included on-chip, and provision is made for adding external pump capacitors (pins 6, 7, and 8) where faster switching is desired. A useful increase in turn-on switching speed will be observed for values of 100pF to 1nF. Full enhancement gate rise times range from several hundred microseconds for low supply voltage, a large MOSFET, and no external charge pump capacitors, to less than 50µs for supplies of 12 to 15V and 1nF external charge pump capacitors. The output rise time is very fast when operating on high (15V) supply voltages, as the charge pump drives the MOSFET gate up to V_{DD} within 2µs of the input going high.

The control input turns the MOSFET on for any input greater than approximately 3.5V, so the MIC5011 interfaces directly with CMOS logic, open collector gates, opto-isolators, switches, etc. Interfacing techniques are discussed in greater detail in a later section.

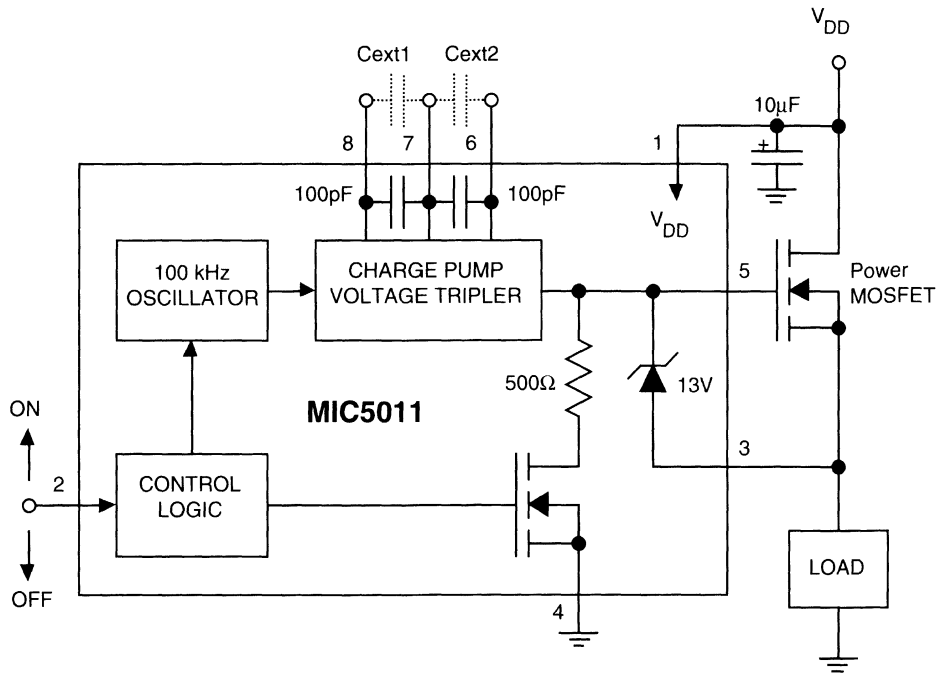


Figure 2. MIC5011 Block Diagram

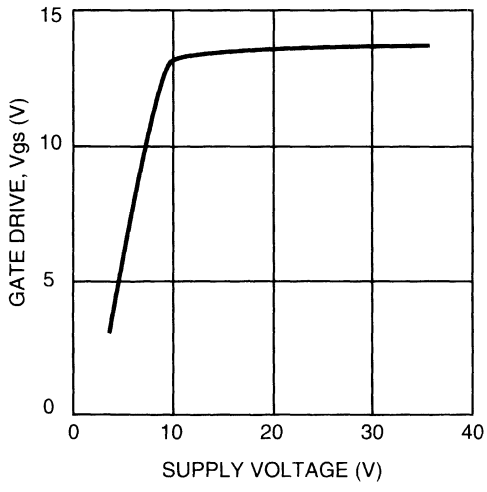


Figure 3. Gate Drive vs. Supply Voltage

Inductive Loads

Many loads such as solenoids, motors, and relays, exhibit inductive characteristics. When an inductive load is commutated a negative voltage spike results (see Figure 4). The spike is clamped by the power MOSFET's source as the MIC5011 holds the gate at ground potential. The load inductance drives the source as far negative as necessary to threshold the MOSFET and force it to carry the load current (typically 5 to 8V below ground). In Figure 4 the spike develops 29V across the MOSFET while it carries the full load current. No clamp diode is necessary since the MOSFET performs this task, but safe operating area (SOA) and the additional dissipation should not be forgotten. SOA is often not an issue, such as in this example where the IRF530 can handle 25A at 29V V_{DS} (the load is only 0.5A).

Motors, which are often considered "inductive" loads present a different problem. A spinning motor continues to generate a voltage after the MIC5011 shuts off. In applications where feedback is employed to control the MIC5011, the motor voltage may interfere with the operation of the circuit. The circuits of Figure 5 and "Push Button Control" of Figure 7 will not work with motor loads.

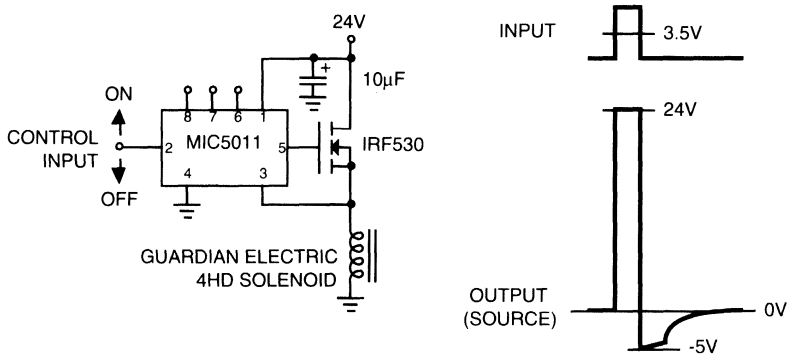


Figure 4. Clamping Inductive Transients

Noise Immunity

In combination with an appropriate power MOSFET, the MIC5011 can control virtually any load that operates on a 4.75 to 32V supply. Aside from the negative spike produced by inductive loads, other pitfalls await the unwary high-side switch designer. For example, ground noise generated when switching a high-power load, especially one with a high inrush current such as an incandescent lamp, can cause oscillations at turn-on or turn-off with slow-moving inputs. Good bypassing is essential; a 10µF aluminum electrolytic capacitor is recommended from supply to ground. Don't confuse charge pump action with spurious oscillations. A slight "ripple" (synchronous with the charge pump clock at pin 8) is normally present on the rising edge of the output; rail-to-rail oscillations at the output are indicative of spurious feedback.

Attention should be paid to layout. For example, the MIC5011 ground pin should be returned to the input signal ground, not the load ground. The MIC5011 is non-inverting, and hysteresis is easily added for any load other than a motor (see Figure 5). Any arbitrary noise margin is added by selecting the appropriate resistor ratio.

5V Operation

The MIC5011 is suitable for use in high-side driver circuits down to about 7V. A low-side driver topology works down to 4.75V, and is suitable for operation on a 5V logic supply. Figure 6 shows a complete low-side driver for use on 4.75 to 15V supplies. Pin 3 is grounded to clamp the gate potential at 12.5V.

Only the power MOSFET breakdown ratings limit the load voltage. In fact, half- or full-wave rectified ac could be applied to the load where economy is important. Don't forget to add a clamp diode to inductive loads.

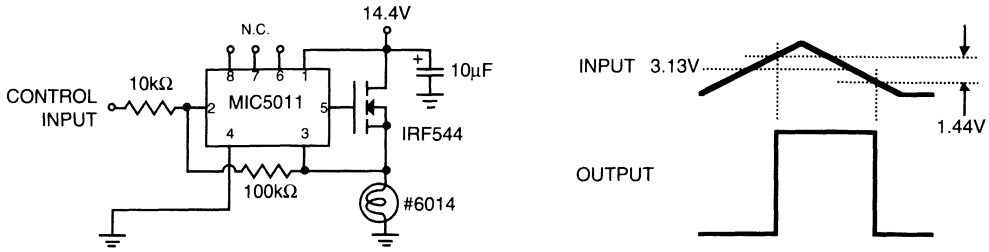


Figure 5. Adding Hysteresis to Suppress Oscillations with Slow-Moving Inputs

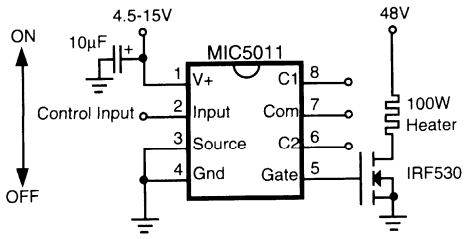
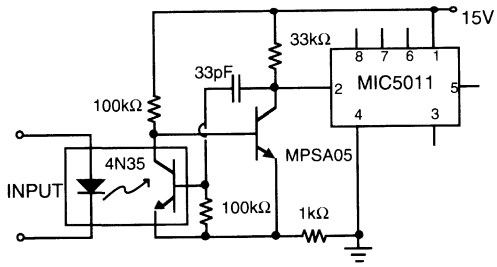


Figure 6. Low-Side Driver

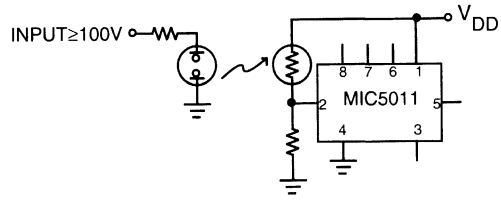
Control Inputs

The MIC5011 is easily interfaced to any control signal. The input threshold is approximately 3.5V, and the input current is less than 1µA. Some examples of typical control inputs are shown in Figure 7. For industrial applications, electrical isolation may be desirable for either safety or noise reasons. Opto-isolators are a good choice for this use and with the hysteresis circuit shown, they provide clean switching. High voltages can be sensed and acted upon with a neon light and a light-dependent resistor.

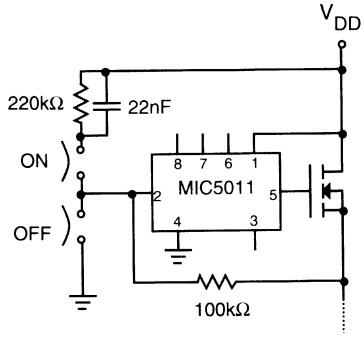
Familiar momentary "ON/OFF" push buttons are easily accommodated as shown. The "ON" button is AC coupled so that any contention between the "ON" and "OFF" buttons is resolved in favor of the "OFF" button. Hysteresis is used to latch the output into the appropriate state. 5V logic commands are interfaced by a CMOS gate. Since the MIC5011 input includes electrostatic discharge protection to the supply, the logic gate should not be powered from a supply higher than V_{DD}.



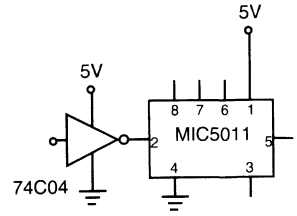
OPTICALLY ISOLATED INPUT



HIGH VOLTAGE INPUT (POSITIVE OR NEGATIVE POLARITY)



PUSH BUTTON CONTROL



5V LOGIC INTERFACE

Figure 7. Various Interface Circuits

Application Note 3

Driving Halogen Lamps

by Brenda Kovacevic

Introduction

Halogen lamps are preferable to incandescents in many applications due to their increased brightness and longevity. Halogen bulbs are used in many varied applications, such as:

- automotive headlamps
- police vehicle-top flashers
- ambulance, tow truck, fire engine-top flashers
- machine vision
- fiber optic illumination
- large scale lighting displays
- medical and analytical equipment
- school bus flashers

Halogen Lamps vs. Incandescent

A typical incandescent lamp is a glass bulb filled with an inert gas (such as krypton or argon) with a tungsten filament in the center. The filament glows as a potential difference is applied across the terminals of the bulb, giving off light and heat. However, the tungsten molecules are evaporating from the filament to cause this glow; the convection currents of the fill gas carry these molecules to the cooler inner surface of the bulb wall where they are deposited. This decreases bulb output and life in two ways: first, the effective filament diameter is decreased, which increases the resistance of the bulb, and second, the glass is "blackened" by these deposits. This mechanism limits the wattage that a conventional lamp can be used at if a satisfactory lifetime is to be achieved.

A halogen lamp operates in the same manner, except that a small amount of halogen gas has been added to the fill gas; this halogen is normally bromine. When the bulb wall temperature reaches roughly 250°C, the "halogen regenerative cycle" begins to take place. The evaporated tungsten molecules now combine with the free halogens to form a tungsten halide compound with a condensation temperature below the wall temperature. Hence, the tungsten does not settle on the glass wall, but returns to the filament where it is redeposited. This process accounts for the almost infinite lifetime of halogens as compared to incandescents. As this cycle begins at a wall temperature of 250° C, the filament must not only generate light but must also maintain this high temperature. Gas pressure is also higher in a halogen bulb than in an incandescent bulb, which retards the tungsten evaporation and allows operation at higher temperatures and greater efficiencies. This is why they are brighter than normal incandescent bulbs.

Basic Considerations

Although halogens operate similarly to incandescents, they do have some key differences that must be taken into consideration while designing/prototyping with them. Most obviously, it is important not to touch or look directly at them while testing as they do operate at greatly increased temperatures and brightness levels. Tinted safety glasses or sunglasses should be worn while working with halogens. Also, as the condition of the glass wall is crucial to the halogen regenerative cycle, it is important not to leave finger marks or imprints on the glass surface. At best, the imprint will be permanently etched into the glass. At worst, the bulb will explode due to the change in pressure (halogens operate at a high internal gas pressure). To remedy this, any finger marks can be cleaned off the bulb prior to use with acetone or propanol.

As the filament must generate the heat necessary to maintain the wall temperature of 250 ° C, it is important not to operate the lamp at any more than 10% (continuously) below its rated design voltage. As halogen lamps are usually designed to their maximum limits, it is also not recommended that they be operated at a continuous voltage higher than the rated design voltage. Operation above rated voltage is considered the single most damaging factor in terms of lamp lifetime. Unfortunately, since incandescents do not have this restriction, this is commonly overlooked.

Special sockets/holders are also required due to the high temperatures generated. For bulbs rated at 35 Watts or below, heat resistant phenolic (hard plastic) holders are adequate. Bulbs rated at 50 Watts or above require the use of special ceramic holders; two excellent sources of supply for such holders are Gilway Technical Lamp, and GTE Sylvania.

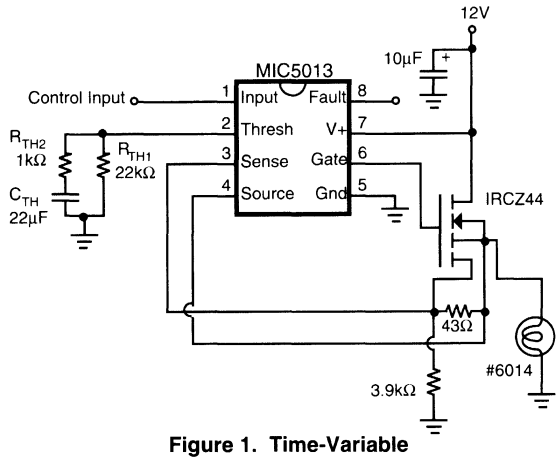
A Simple Power MOSFET Drive Circuit

A major consideration when driving halogen lamps is the inrush current generated when starting up a cold filament. This inrush can range from 20 A to100 A and lasts from 10 to100 ms depending on the construction of the lamp. As power MOSFETs have large peak currents and wider SOAs (safe operating areas) than do bipolar junction transistors, they are a good choice for driving halogen lamps. N-channel MOSFETs are more cost effective and have lower on resistances than P-channel MOSFETs. However, N-channel MOSFETs require a significant gate enhancement above the positive rail when driving a grounded load. This necessitates the use of a charge pump.

A MIC5010 family MOSFET predriver and an N-channel power MOSFET make an excellent drive circuit for a halogen lamp. The MIC5010 family of predrivers have an on-board charge pump, which saves space and design time. The MIC5013 also offers an over current sense feature to detect a

short circuit and turn off the power FET in time (10µs typical shutdown time) to prevent damage. This overcurrent shutdown can be delayed such that the initial inrush current doesn't cause a false triggering of this protection feature. This can easily be accomplished by adding an RC network to the threshold pin of the MIC5013 such that the initial trip point is very high, but decays with time to a reasonable value (figure 1).

The design equations as shown are used in this circuit to set a final current trip point of roughly twice the current needed by the lamp. R_{TH2} is used to increase the current limit at turn-on to roughly 10X the steady-state value. The choice of C_{TH} governs the time constant or decay of the high initial trip point, and will need to be varied depending on the time constant of the inrush current of the particular lamp used. This design has a 20 ms time constant.



$$R_S = \frac{SR\,(V_{TRIP} + 100mV)}{R\,I_L - (V_{TRIP} + 100mV)}$$

$$R1 = \frac{V + SRR_S}{100mV\,(SR + R_S)}$$

$$R_{TH} = \frac{220}{V_{TRIP}} - 1000$$

For this example:

I_L = 30A (trip current)

V_{TRIP} = 100mV

Figure 1. Time-Variable Trip Threshold

If the lamp being driven by this circuit is pulse-width modulated, extra care must be taken in choosing a PWM frequency and capacitor value. When the device is switched off, the threshold pin appears as an open circuit and C_{TH} is discharged through the two resistors. This is a slower process than the turn-on time constant; any residual charge in the capacitor will act to reduce the current limit. If the device is switched at certain frequencies, (dependent on capacitor value) the capacitor will have time to charge during every cycle, but not to discharge properly. This can lead to erroneous over current shutdown at normal operating currents.

A 75X/Minute Halogen Flasher Circuit

Illustrated in Figure 2 is a 75X/minute, 50% duty cycle halogen flasher circuit, prototyped using six MIC5011s and six 100 Watt halogen bulbs. Over current sensing was not used for this prototype, but could easily be added to each lamp by using MIC5013s per figure 1. The drains of the power FETs, the timing circuit and the MIC5011s were all driven from one power supply.

Potential applications for this design are tops of emergency vehicles such as ambulances and police cars, school bus flashers, turn signals, beacons, and large scale lighting displays.

Government specification KKK – A – 1822C, which governs flashers for emergency vehicles, dictates that a 50% duty cycle with a variation of no more than 3% be used. The timing circuit shown in figure 2 achieves this by first creating a clean 50% duty cycle signal from a 7555 (CMOS 555) at twice the needed flashing frequency, or 150 X/minute. This is accomplished by using equal resistors and diodes, as shown. This clean, but not quite in-spec, oscillator is then fed into a CD4013 D flip-flop configured as a simple "divide-by-two" circuit. This ensures that the duty cycle is 50% with very little error. It is crucial to bypass both chips with a 0.01 µF ceramic disc capacitor from V_{CC} to ground, as system noise will greatly affect the accuracy of this oscillator.

This design has one set of three lamps flashing 180 degrees out of phase with the other group of three, emulating the red and blue halves of a police car-top. This is accomplished easily by using the $\overline{Q}$ output of the flip-flop for the one set and the Q output for the other. The set and reset functions of the flip-flop, tied to ground in this prototype, could be used to provide external control of the flasher (ie, to turn it on constantly or shut it down).

This specification also stipulates that the maximum voltage drop across the entire flasher be not more than 0.5V. The best way to achieve this is by the use of low R_{DS}(on) power FETs.

This is crucial for other reasons as well; the current requirements are very stringent for this system. If the switch loss is not kept to a minimum, the lamps may not receive adequate voltage for turn on. Also, the I^2R loss associated with the switch creates a great deal of heating that can cause the early demise of the power FET. Chosen for this design was the IRF Z40,which has an R_{DS}(on) of 28 mΩ, a peak drain current rating of 160A, and a continuous drain current rating of 35A. A high peak as well as continuous current rating is crucial as the inrush currents for each lamp may be as high as 100A, and the continuous current will be 5 to 10A. (This of course, varies widely from lamp to lamp). The drawback that this power FET has is that it is only rated to 50V. If a system with high voltage spikes is used, then some form of protection such as power zeners or Transzorbs will be necessary (a FET with a higher peak V_{DS} can be used if a higher R_{DS}(on) can be tolerated).

Prototyping this design requires that the FETs be adequately heat sunk to prevent damage. A large 1/8" thick aluminum heat sink was employed, with the power FETs spaced roughly 2" apart. The final package used should also allow for adequate heat sinking, to prolong the operating life. The lamps should NOT be heat sunk, as they must reach high temperatures to initiate the halogen cycle.

As the lamps are driven in parallel, the currents are additive.Very high currents are generated during the inrush stage; this requires that #10 (or similar)copper wire be used for the V_{CC} and ground connections to the power supply. If the power supply used in prototyping doesn't have the current capability to start up the lamps, a car battery may be used.

Finally, the lamps and MIC5011s must be operated from a common ground. If connected to ground via long wires or to separate grounds, a "ground loop" or situation where one ground is actually at some potential above the other ground may result. Such a resistive ground may result in a current flow that prevents proper lamp turn off between flashes. Use of either a single point ground or a chassis ground to form a ground plane will prevent this. If this is impossible, optoisolators may be effectively used to "open" such ground loops, eliminating this problem (see the Hewlett Packard Optoelectronics Applications Handbook for more details).

A 120X/Minute Flasher Design

As an alternative to the above design, a higher frequency design with longer on-time is shown in figure 3. The design methodology is to prolong lamp life by maximizing on time. This design does not meet the government specification referenced earlier, but is suggested for applications where long service life is essential.

Possible applications include hazard lighting, beacons, large scale lighting displays, emergency vehicle tops not covered by the referenced specification, and large scale lighted store front signs.

Timing is controlled via a simple 7555 (CMOS 555) circuit, set to flash the lamps 120X/minute. The duty cycle is set to insure an on time of 65% and an off time of 35%, which gives a visible flashing while allowing the lamps to remain on long enough to achieve the necessary wall temperatures. Slower flashing frequencies (or shorter on-times at this frequency) will reduce the lifetime of the lamps by allowing them to cool down between blinks. This reduced filament life is due to the lamp completely reheating during each on cycle. If a slower flashing frequency is to be used, the duty cycle should be adjusted such that the lamps are on for the longest portion of the time possible that still allows for visible flashing (i.e., the lamp must be given time to visibly blink). Once again, the 7555 must be adequately bypassed to prevent system noise from interfering with duty cycle and frequency. If greater accuracy is desired, a film capacitor may be substituted for the indicated tantalum.

The power FET chosen for this design is an IRF540, which has an R_{DS}(on) of 77 mΩ , but a peak voltage capability of 100 V. It has a peak drain current specification of 110 A maximum, and a continuous drain current specification of 28 A maximum. Although it does have a higher R_{DS}(on) than the IRFZ40, it is a more rugged part in terms of withstanding systems transients and noisy environments. It will require more rigorous heat sinking than the IRFZ40. FETs with higher R_{DS} (on) that the IRF540 are not recommended for this design due to the high peak currents encountered, and the amount of heat that would be generated.

All lamps are flashing in unison in this design; if this is not desirable an inverter can be used in conjunction with the 7555 such that 180 degrees out of phase flashing of two (or more) sets of lamps can be accomplished.

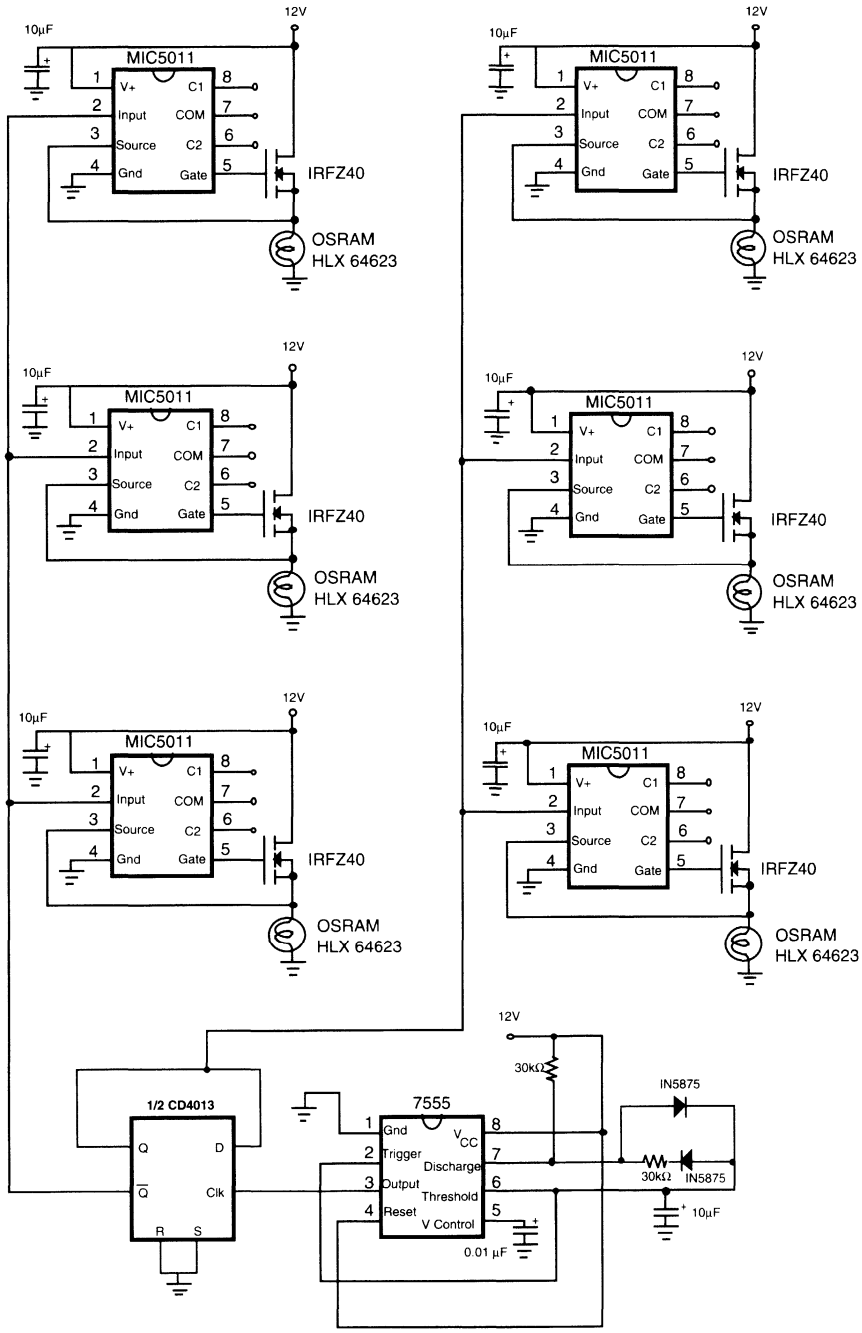


Figure 2: A 75X/Minute, 50% Duty Cycle Halogen Flasher

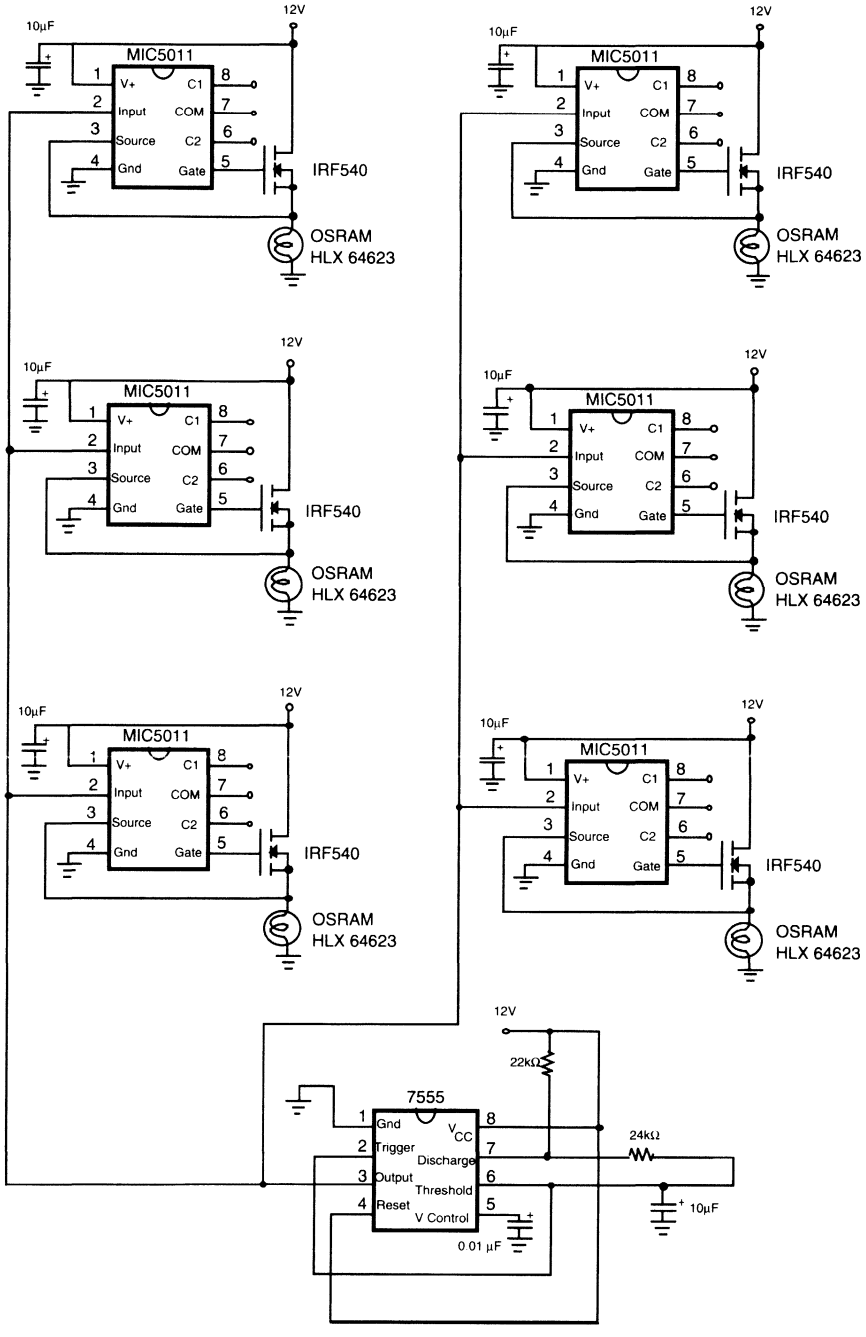


Figure 3: A 120X/Minute Halogen Flasher

Application Note 4

Using the MIC5010 Family in Automobile Alarm Systems

by Bob Wolbert

Introduction

For better or worse, automobile alarm systems are a fast-growing segment of the automotive aftermarket. This note briefly describes some of the more common systems, some ideas for future development, and how the MIC5010 family of high side MOSFET drivers can ease their design while improving performance and reliability.

Automotive Alarm Background

The typical automotive alarm system consists of three main blocks: sensors for intrusion detection, the control unit, and output devices for alerting passersby or disabling the vehicle.

Sensors vary from electronic ultrasonic intrusion detectors and audio devices (microphones and audio amplifiers) for vibration and glass breakage detection, through a mercury switch for motion detection, to electromechanical contact switches showing an open door, trunk or hood.

The control unit is the processing device. It enables and disables the sensors and output devices, and knows whether an input is expected or is cause for alarm.

Alarm system output devices range from simple, already installed standard automobile accessories such as the horn and headlamps, through accessory sirens, to more exotic systems such as an alerting transmitter or ignition "kill" switch. Some proposed systems have provisions for cellular telephone output for calling the authorities(!). "Help me! I'm being stolen.....! This is a recording....." Figure 1 shows a typical alarm system, including sensors, a control unit, and outputs, and Table 1 shows some typical inputs and actions.

Alarms have three main modes: disarmed, armed, and alert (or emergency). In disarmed mode, the alarm is transparent to the user. When armed, the control unit enables the sensors and awaits input. There are usually two types of alerts—one is immediate, triggered by breaking glass, for example; the

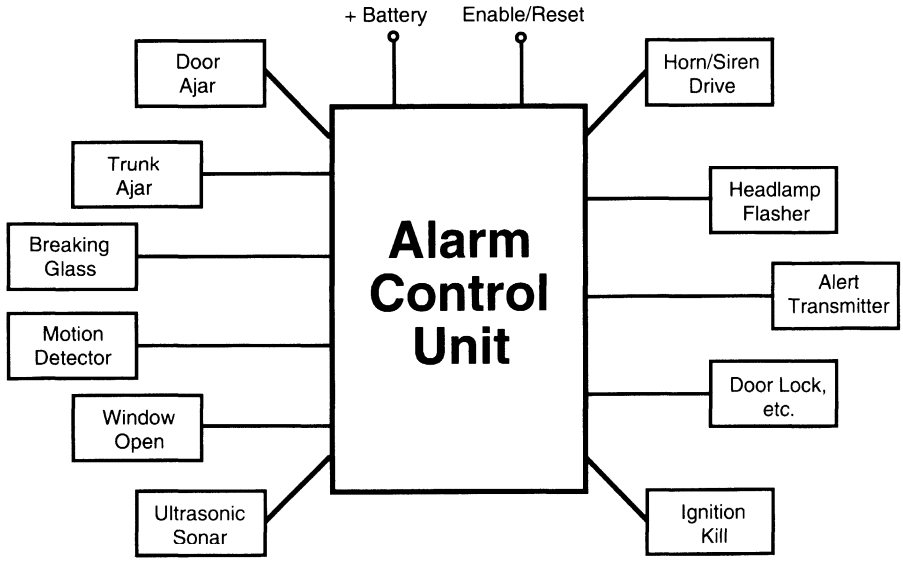


Figure 1. Automobile Alarm System Typical Block Diagram

Table 1. Alarm System Typical Input & Output

Input	Output (Set Mode)	Output (Emergency Mode)
Door Ajar Switch	Raise Window	Horn
Hood Ajar Switch	Lock Door	Flash Headlamps
Trunk Ajar Switch	Close & Lock Sunroof or Moonroof	Siren
Motion detector	Lights off (timer)	Pager/Alert Transmitter
Glass Breakage Detector (audio)	Close Convertible Top	Kill Ignition
Ultrasonic Detector	Enable Alarm	(Phone police)

other is delayed and occurs after a door is opened, allowing the owner time to disarm the system. Output devices are turned on, either immediately or after a reset delay.

Newer systems have an additional mode—a set mode, where the car is readied for safe parking. Upon initialization, the control unit checks the status of door locks, windows, sunroof/ moonroof, convertible top, etc., and closes and locks each if necessary. Then normal alarm arming takes place.

Design Philosophy

Like most automotive products, several design goals are specified. Automobile alarms must be small in size, operate from the 12V negative ground battery system, have low standby current drain, operate over a wide temperature range, withstand reversed supply polarity and electrical load dumps, etc.

The control unit is designed for high reliability and low power consumption. CMOS logic is extensively employed. The output devices are moderate to high current drains, and require power switching devices. "High Side", or positive rail, switching is preferred due to the chassis negative ground electrical system.

Some systems use a single system board while others use distributed control, sense, and drive boards. If distributed, communications is provided through serial or 4 bit parallel data busses.

All systems require one or more power switches to cause or control actions in the "real" world by switching anywhere from 1 to 30 Amperes.

Load Switching

Switching 1A to 30A or so loads is non-trivial. Most present-day systems use relays for load control. Relays have several problems associated with their use (see Table 2). A far more ideal switch is the Power MOSFET, with its smaller size, lower cost, higher reliability, and minute drive requirements. Almost all automotive electrical systems have a negative chassis ground. Safety and this "common" point constraint requires that most electrical power switching be done in the positive path—"High-Side" switching is preferred. Thus, alarm system outputs should be high-side controlled. Using a Power MOSFET in the high-side mode requires the FET gate voltage be switched from a low level "OFF" state to an "ON" state where the gate is at a voltage higher than V_{CC}. Generating and controlling this high switching voltage has required large amounts of external circuitry in the past, effectively restricting the Power MOSFET from the automobile. The MIC5010 High Side FET Driver family combines all necessary high side driving functions into a single IC package, and allows the economic and reliable introduction of DMOS to automotive electronics.

The MIC5010 FET Driver Family

The MIC5010 family of high- and low-side FET drivers is ideally suited to this application. Configured as a high side driver, the MIC5010 will take a CMOS control input and drive the gate of an N-Channel MOSFET above the positive supply. The low power MIC5010 family employs CMOS logic for compatibility and a charge-pump voltage tripler with internal capacitors for gate voltage generation. CMOS input compatibility guarantees proper termination for the controller logic, and the power MOSFET can be protected by adjustable current limiting, all controlled by the MIC5010 (or MIC5013). The relatively fast switching speed of the MIC5010 family of drivers reduces the power dissipation of the MOSFET by quickly transiting from the no current, high V_{DS} off state to the high current, low voltage ON state. The benefit is both increased reliability and little or no heat sinking required (depending on the size of power MOSFET employed).

The MIC5010 family has four members, the "full featured" MIC5010, with over-current limiting, fault detection, speed-up capacitor options, and an extra ENABLE input; the no-external-parts MIC5011; the dual driver MIC5012; and the MIC5013, offering over-current protection with fault signalling in an 8-pin package. Table 3 summarizes the features and differences between the variants.

Table 2. Switches for Alarm Outputs

Power MOSFET Advantages vs. Relays

- Extremely low drive current requirement
- Smaller size
- Lighter weight
- Non-mechanical (much longer life)
- No contact bounce
- Lower cost

Power MOSFET Advantages vs. PNP

- No fixed voltage drop
- Extremely low drive current requirement
- Larger Safe Operating Region

MIC5011

The lowest cost member of the 5010 family, the 8-pin MIC5011 requires no external components for high-side driving applications. As shown in Figure 2, when a logic HIGH is forced on the input, the oscillator and charge pump begin their voltage tripling action. The output charges the FET gate capacitor and turns on the FET. Standard Power MOSFETs are damaged if V_{GS} is greater than 20V, but are not fully on unless V_{GS} is around 10V. The internal 12.5V zener diode connecting the FET gate and source limits the voltage multiplication action so that V_{GS} is approximately 12.5V, a value that ensures low ON resistance as well as long FET life.

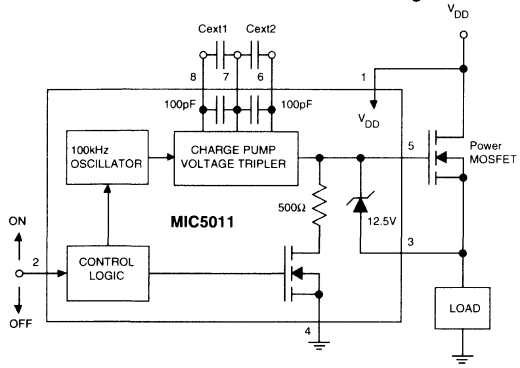


Figure 2. MIC5011 Block Diagram

Inductive loads, such as the horn or headlight relay, give many drivers problems. The MIC5011 takes inductive loads in stride, however, and a "catch" diode to clamp inductive flyback spikes is not even necessary (see Figure 3). As an inductive load is switched off, a negative flyback pulse is applied to the FET source. The MIC5011 holds the gate firmly near ground level, sourcing or sinking current as required. The resultant $+V_{GS}$ (V_G=0, V_S=negative) temporarily biases ON the FET and dissipates the spike (See Application Note 1, *MIC5011 Design Techniques*, for full details).

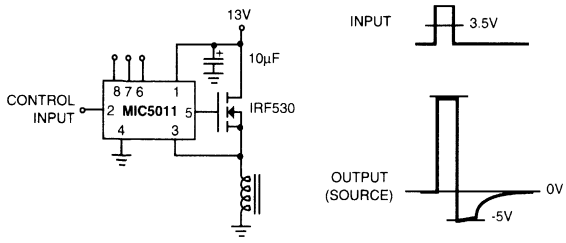


Figure 3. Inductive Spike Clamping

MIC5012

The MIC5012 is a dual version of the MIC5011. Two completely independent drivers control two loads from one 14-pin (16-pin surface mount) package. Operationally, each half of the MIC5012 is identical to the MIC5011.

MIC5013

When over-current protection is required, the 8-pin MIC5013 should be used. In a basic application, MIC5013 circuitry is similar to the MIC5011 or MIC5012. However, by adding four resistors, the MIC5013 can act as a circuit breaker; its output switches off if load current exceeds a user-determined value. As shown in Figure 4, the user has three design variables for limit selection, allowing a small sense resistor, R_S, for best efficiency. R_{TH} sets the internal voltage comparison threshold; current limit is inversely proportional to R_{TH}. R_1 and R_2 may be eliminated in many applications where the load is generally resistive and open loads are not expected. See the MIC5013 datasheet for full details on flexibly programming the current trip point.

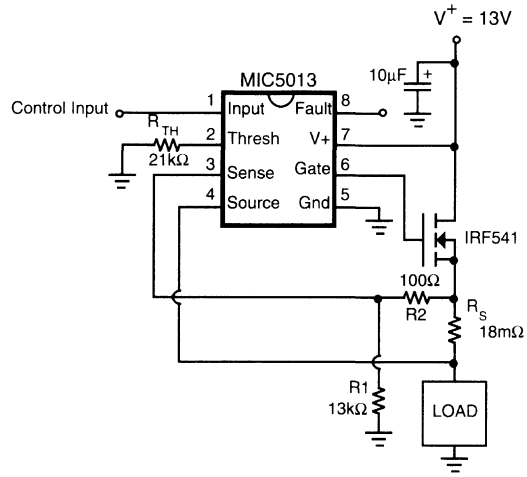


Figure 4. Current Protected Driver

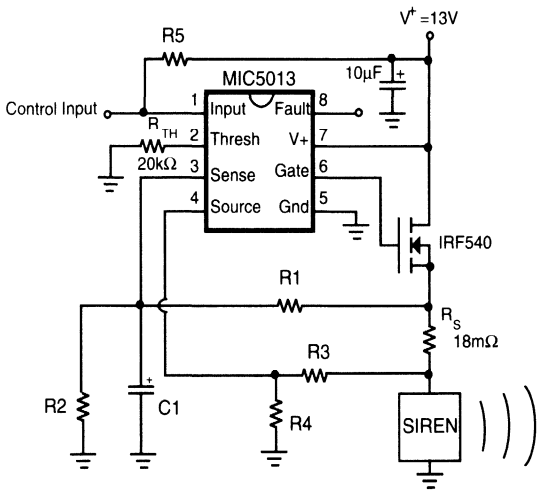
Automotive Alarm Hint: Remote Siren Drive with Automatic Shutdown

High security alarm systems provide an alert mechanism if the control unit is compromised. Figure 5 shows a circuit that :

- Is controlled by a single small gauge wire
- Is remotely mounted, perhaps under the hood
- **Will automatically switch ON if the control line is cut**
- Will reset itself after a time delay
- Requires only a MIC5013, a FET, and a few passive components

The circuit is built on a small board, and may be attached to the siren (or other output device) directly. The MIC5013 is configured with a direct battery line, ground and a single control line. If the alarm output unit is compromised by severing the control line, pull-up resistor R_5 enables the MIC5013, which activates the FET, and the siren sounds.

Basically, the circuit operates in a standard current detect mode. The difference is that an additional capacitor, C_1, begins to charge through R1 as soon as the alarm activates.



Circuit sounds immediately upon Control Input triggering or Control Input disconnect (cut) and will reset after t ≈ 120 seconds.

R1 = 91kΩ
R2 = R3 =100 kΩ
R4 = 68kΩ
R5 = 470kΩ
C1 = 100µF

Figure 5. MIC5013 Driver With Automatic Sound/Reset

As the voltage across C_1 exceeds the voltage on Pin 4 plus the V_{TH} set by R_{TH}, an over-current condition is simulated, and the output is shut down. Reset occurs with control line cycling or power interruption. This means that the siren will sound once, for a fixed amount of time, and then silence itself in accordance with some local laws and good engineering practice (not to mention preventing total battery discharge).

Because the MIC5013 takes almost no current in the OFF or standby modes (0.1µA, typical), both it and the driven FET can be directly connected to the battery.

Conclusion

The automotive alarm marketplace demands smaller and less expensive yet more reliable methods for output load drive and control. In alarm applications, where standby current drain is paramount, the low power MIC5010 series allows easy interface with low power CMOS logic control while providing all necessary drive control for small, efficient Power MOSFETs. For applications where the output devices are original equipment—horns and headlamps, for example—and the control unit drives the stock horn relay or headlamp relay, the MIC5011 or MIC5012 dual FET drivers are suggested. Where high current loads are directly driven, the protection offered by the MIC5013 is attractive.

The winning combination of MIC5010 drivers and Power MOSFET switches enables configuring a simple, hence reliable. and rugged alarm system.

Table 3. Comparing the MIC5010 Family Options

Device	Features
MIC5010	• Over Current Sensing • Fault Flag Output • 14-Pin DIP or Surface Mount Packages • Provision for Optional Speed-Up Capacitors • Over Current Enable Pin
MIC5011	• No External Components Required • Provision for Optional Speed-Up Capacitors • 8-Pin DIP or Surface Mount Packages
MIC5012	• Dual High Side Driver • No External Components Required • 14-Pin DIP or 16-Pin Surface Mount Packages
MIC5013	• Over Current Sensing • Fault Flag Output • 8-Pin DIP or Surface Mount Packages

Application Note 5

Solid State Circuit Breakers

by Brenda Kovacevic

Introduction

Until very recently, few alternatives to electromechanical and magnetic circuit breakers existed. Designers were forced to live with such undesirable characteristics as arcing and switch bounce (with corresponding noise and wear), while accomodating large unwieldly packages in their high power systems.

Solid state technology applied to this traditional device has resulted in circuit breakers free from arcing and switch bounce, that offer correspondingly higher reliability and longer lifetimes as well as faster switching times. A typical solid state circuit breaker will switch in a matter of microseconds, as opposed to milliseconds or even seconds for a mechanical version.

New solid state products currently on the market utilize the many benefits associated with power MOSFETs to deliver a product far superior to earlier silicon versions. Power MOSFETs offer low on resistances (as compared to bipolar transistors), low voltage drops, low EMI, faster switching times and good thermal stability of key parameters.

However, two key advantages that the electromechanical devices have over the solid state versions are simplicity and low cost. For example, a simple commercial circuit breaker relay combination will sell for $4.00 to $6.00 in low volume . The existing solid state circuit breakers will run from several times that amount, and typically include many bells and whistles that the average designer can do without. This cost difference is somewhat less in military versions, as the mechanical devices must also undergo extensive testing.

One reason for the corresponding complexity of the silicon based systems is the power MOSFET drive circuitry required. If N-channel FETs are to be used (N-channel FETs are preferable to P-channel as they have roughly 2.5 times lower R_{DS} (On) and correspondingly lower cost), a charge pump or voltage tripler must be supplied to provide sufficient gate enhancement to turn on the FET. This involves supplying an oscillator as well as the necessary diodes and capacitors, which definitely take board/hybrid package space.

A simple, inexpensive solid state circuit breaker can be made using the MIC5013 power MOSFET predriver with overcurrent sense. This predriver was designed for driving N-channel FETs, and has an on-board charge pump to provide sufficient gate enhancement. This eliminates the issue of providing this enhancement externally; providing a one component solution to what once consumed extensive "real estate".

As any size FET can be driven by the MIC5013, almost any load can be accomodated. High inrush or inductive loads are driven with equal ease, greatly expanding the realm of possibilities for these circuit breaker topologies.

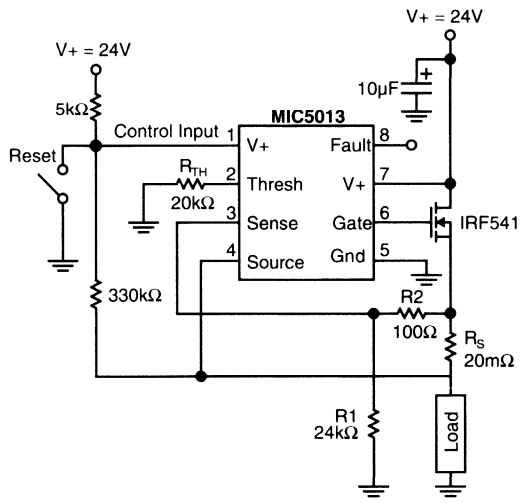
An internal comparator is used to sense an over-current condition; this feature allows the use of this product as a circuit breaker that can be programmed to trip at a specified current via choice of an external sense resistor. An overcurrent flag provides this information externally, allowing easy digital interface /control of the device. This feature allows its use in more complex, remotely controlled designs such as those currently used in high reliability applications.

Using this highly versatile device, four circuit breaker configurations have been devised; a low parts count, low cost externally resettable version, a minimal parts count remotely resettable version with indicator, a minimal parts count automatically resettable version, and a full blown power controller design with Z8™ microcontroller interface. Typical applications for the first three versions include a variety of commercial, industrial and military applications, such as battery pack circuit breakers/current limiting, electric vehicles, and heavy machinery. The latter design is useful in high end applications such as military avionics or industrial automation. It offers a substantial cost savings over the currently available remotely controllable electromechanical units, as well as most currently available hybrid designs of this complexity.

Minimum Parts Count Configuration

Figure1 illustrates the most basic configuration.The overcurrent trip point is set via the design equations in this figure. The current sense operates via a comparator which compares the voltage on the sense pin to an offset version of the voltage on the source pin. The current on the threshold pin, set by choice of R_{TH}, is mirrored and returned to the source by a 1 kΩ resistor.

This sets the trip voltage of the comparator. When a fault condition occurs, an internal current sense latch is set, which turns off the power FET. The control input pin must be toggled low then high by the reset switch before the FET will be switched on again (after the short has been removed). A 330kΩ resistor is provided to hold the input low and keep the FET off until the circuit is reset. Advantages of this topology are its simplicity and correspondingly low cost.



R1 = V+ / 1mA

R2 = 100Ω

$R_S = (100mV + V_{TRIP}) / I_L$

$R_{TH} = (2200/V_{TRIP}) - 1000$

For this example:
I_L = 10A (trip current)

V_{TRIP} = 105mV

Figure 1: Basic Circuit Breaker/Switch Configuration

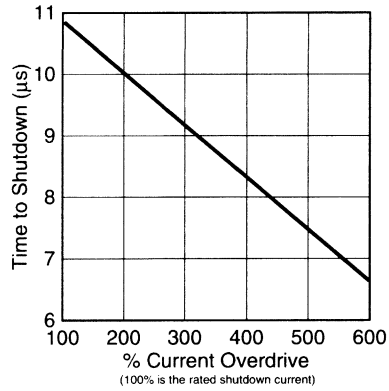


Figure 2: Shutdown Time vs. % Current Overdrive

Response Time

Figure 2 illustrates an advantage that is common to all MIC5013 based topologies: fast response times. A graph of shutdown time versus current overdrive is shown. The data was taken using this simple topology without the 330kΩ pulldown resistor, however, all configurations (with similar loads) will have a similar response as it is mostly a function of device parameters. (Note: This data was averaged from a small sample size; about 5-10% variation from this line may occur).

Response times in the order of µs means that a short circuit can be detected in time to prevent extensive damage, and is an improvement of an order of magnitude over electromechanical circuit breakers.

Remotely Resettable Configuration

The circuit breaker configuration of Figure 3 is designed to be used for applications requiring remote indication and reset capability. When the breaker is tripped, the fault output pin switches high (to a diode drop below the positive rail). This output is used to drive a remotely located LED. (If an incandescent lamp is desired, the fault output should be used to drive a power FET switch that could withstand the inrush generated). Resetting of the breaker is accomplished by toggling the control input with a remotely located switch. If the distance between the control point and the breaker is large, an optocoupler is recommended to open any ground loops that may occur. Many switch manufacturers offer a package that combines both the switch and the indicator while providing internal isolation, making this circuit even more compact. Shown here is the NKK-SS12SDP2-LE, a small slide switch suitable for instrument or control panels where space is at a premium.

Potential applications for this circuit include use as remotely controlled circuit breakers in aircraft with the indicator/switch located in the cockpit, industrial control panels, heavy machinery, and robotics.

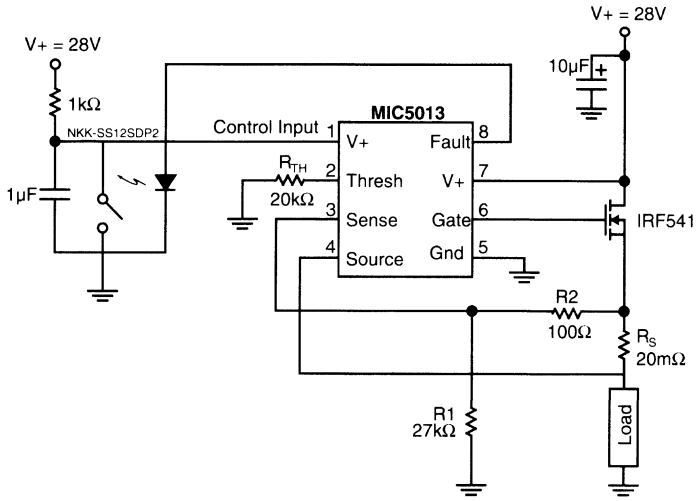


Figure 3: Remotely Resettable Circuit Breaker

Automatically Resettable Configuration

The third circuit,shown in Figure 4, is useful when automatic resetting is desired. This is accomplished by adding feedback from the fault pin back to the control input. A simple Miller integrator circuit is used to test the load every 18 ms until the short is removed. When the short condition no longer exists, the circuit latches on and operates as before. Although no reset button is necessary, an indicator could be added to the fault line if remote notification of a short circuit condition is desired.

The beauty of this configuration is that no human intervention is necessary once a short has occured. A possible drawback is that the gate does briefly turn on every 18ms to test the load. However, if the short still exists, it shuts down again in 10µs. This time duration is short enough to be acceptable in most applications.

Potential applications for this circuit include industrial automation, automotive circuitry, motor drive (stall sensing), and protection for power supplies/battery packs.

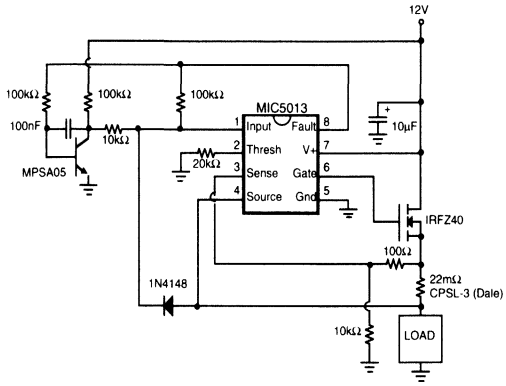


Figure 4: Automatically Resettable 10 A Circuit Breaker

Microcontroller Based Power Controller

A current trend in power electronics is the combination of intelligent power circuitry with microcontrollers; a so called "brains and brawn" combination. The power circuitry provides, in this case, the high current drive and circuit breaker function. The microcontroller can be used to make decisions in the event of a short, i.e., it can drive a warning signal, shut down other components of the system, or switch in a reserve or auxiliary motor (or pump, fan, heater, etc.).

An example of a microcontroller based power controller designed and built using the MIC5013 is shown in Figure 5. Here, three functions are monitored by the microcontroller; condition of the power supply (low or off), open load, and shorted load. If any of these three conditions exist, power is taken from the load and the control input of the MIC5013 and an appropriate LED is turned on. An additional LED is used to flag a hardware fault when an impossible condition (such as an open and short load) are flagged to the microcontroller.

Under normal operation (no fault condition exists), the microcontroller provides drive to the MIC5013 control input, and keeps bit 4 on I/O port 2 (P24) low, supplying drive to an LED signifying that conditions are "OK". (Note: a buffer may be necessary, as the MIC5013 is not TTL compatible).

The circuit breaker subsystem operates similarly to the other cases described earlier, however, all resetting is accomplished by the microcontroller. When the fault output goes high, indicating a short circuit has occurred, one input of the NOR gate is pulled high, causing a low output on the NOR gate. This toggles P32 (bit 2, port 3,) low, initiating the cond_init subroutine (see Figure 6 for Z8 code). This subroutine scans P20-P22 to determine which flag caused the NOR gate to go low. Upon determining that it was P20, P35 is brought low, providing the necessary toggling of the MIC5013 control input such that operation can resume once the short is removed (The MIC5013 current sense comparator output is connected to an internal latch which must be reset). Power has already been removed from the gate output of the MIC5013 by its internal current sense mechanism, shutting down the power FET and corresponding load. P26 is pulled low, lighting an LED that signifies that a fault has occurred.

When the fault is removed, the Z8 will restore power to the "OK" LED, shut down the "Overcurrent" LED, and restore power to the control input of the MIC5013. No isolation between the microcontroller and the MIC5013 was deemed necessary in this case, as the fault output is current limited by the voltage divider resistors, and tends to be fairly clean.

Open load detection is accomplished via the use of an LM301 op amp configured as a comparator. The LM301 was chosen for this application as it has more headroom than most op amps. The inverting input of the LM301 is set to 25 mV below the positive rail, which the non-inverting input will never reach unless the load is removed. The output of the op amp/comparator is fed to the HCPL-2602 optocoupler with the enable pin tied high. Under normal conditions, the output of the HCPL-2602 will be low; it toggles high in the event of an open load condition. The HCPL-2602 is also used to provide isolation between the digital and analog portions of the circuit. A high output from the HCPL-2602 causes the NOR gate to switch low, triggering the cond_int subroutine. The microcontroller reacts as before, removing power from the MIC5013 control input, and flagging the user that a problem has occurred.

The 1000 pF capacitor placed between the inverting and non-inverting inputs of the LM301 along with the 100 kΩ resistor serves as a noise filter, which prevents oscillations. Another way of doing this is to provide a small amount of hysteresis from the output back to the non-inverting input (See reference 4).

Low power detection is accomplished via the use of an optocoupler, the HCPL-3700, that also contains a Schmidt trigger. This provides hysteresis, allowing us to shut the system down when power reaches roughly 50% of rated value, and not turn back on again until we are at roughly 75% of rated value (These levels are chosen via selection of input resistor values and can be changed to meet the requirements of most systems. See the Hewlett-Packard Optoelectronics Designer's Manual for more details). Again, the optoisolator also provides isolation between the digital and analog portions of the circuit.

Shutdown and resetting of the system in the case of a low power condition is accomplished as before, by triggering the cond_int subroutine, which in turn scans port 2 to find the appropriate cause for the trigger and lights the corresponding LED.

If subroutine cond_int detects an impossible combination of conditions, i.e. short and open, a hardware fault has probably occurred. The microcontroller then lights an indicator LED attached to P34, and hangs up until the problem is removed.

The emergency override feature allows a pilot (or vehicle commander) to keep the system alive even though a short circuit has been detected. In a combat or other emergency situation, the equipment could be kept operating until the short circuit causes the FET to blow.

A switch located in the cockpit is used to provide this function. When it is depressed, IRQ2 (P31) is pulled low, causing the internal timer/counter to begin an 11 ms switch debounce count. If IRQ2 is still low (switch is still depressed) after 11 ms, then internal interrupt IRQ5 is activated on time out. Interrupt service routine T1_int then keeps power flowing to the control input of the MIC5013 , and toggles P23 high. This turns on the base of Q1, which pulls the signal on the sense input of the MIC5013 to ground, disabling the current sense function of the part. (If a 14-pin MIC5010 is used instead of the MIC5013, an external inhibit pin is available).

A key advantage of this circuit is that 2/4 interrupt lines and one complete I/O port is left unused. This would allow the microcontroller to be used for other functions in addition to power management.

If this is to be a dedicated power management system and the unused I/O has no other potential purpose, then some ideas for modifications include using an alphanumeric display instead of indicator LEDs, and including a self test mode with indicators on power-up.

If a PWM'ed load is to be used, the Z8 can be used to provide a variable frequency, variable pulse width signal by using the internal counter/timer registers (See the Z8 Design Manual for details). In this case, P36 should be connected to the control input of the MIC5013 instead of P35, and switch debounce will have to be performed in hardware instead of firmware. The MIC5013 can be switched up to a maximum frequency of 20kHz. Digital closed loop motion control can also be performed using the controller.

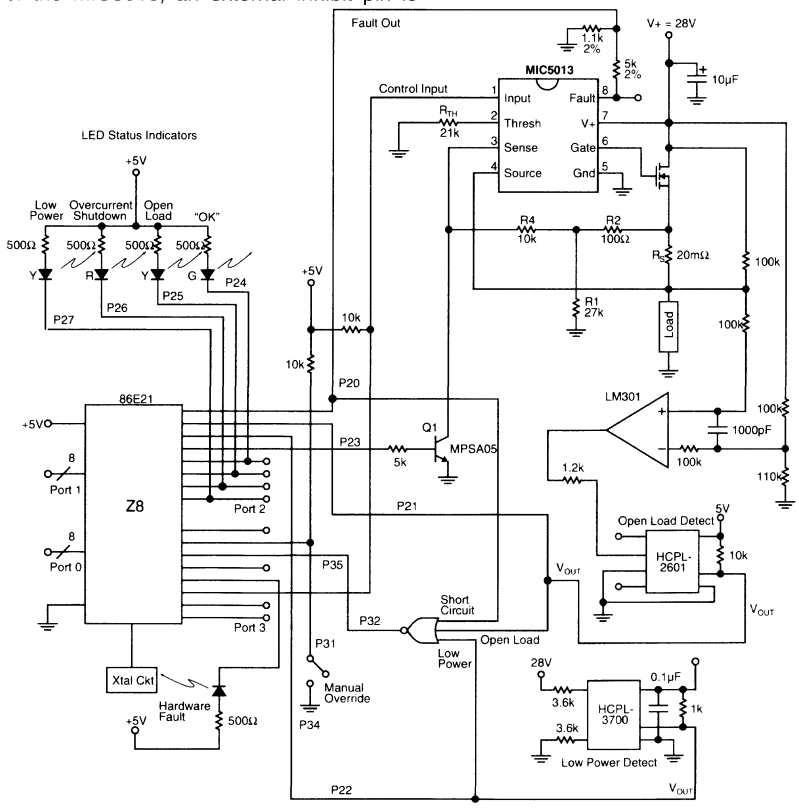


Figure 5: Z8 Based Power Controller

Summary

The MIC5013 MOSFET predriver with over current protection brings a whole new dimension to the world of power management with its versatility, ease of use, and quick response times. Four different lab tested circuit breaker configurations were presented and discussed; a minimum parts count version, a remotely resettable version, an automatically resettable version, and a complete microcontroller based power management system. Many more unique configurations are possible; a configuration to fit most needs can potentially be designed using the MIC5013.

References

1. The Z8 Design Manual, Zilog, 1985

2. The Optoelectronics Applications Manual, HP Optoelectronics, McGraw-Hill, 1981

3. Micrel Databook, 1991

4. Pease, R. A. , Troubleshooting Analog Circuits , Butterworth - Heinemann, 1991

5. Faber, Al and Kennelly, Bob, "Hybrid Power Controller Outperforms Conventional Circuit Breakers", *PCIM* , November 1990, pg. 40

6. HP Application Note 1004, "Threshold Sensing For Industrial Control Systems With the HCPL-3700 Interface Optocoupler"

7. Frank, Randy and Psaenich, Al "Surviving Short Circuits", *Machine Design* , March 8,1990, pg 89

8. Conner, Margery, "Devices Let Aircraft Use Higher Voltages", *EDN* , August 17, 1989, pg 59

9. asmS8™ Super 8/Z8™ Cross Assembler User's Guide, Zilog 1985

Figure 6: Z8 Microcode

```
.title CIRBR.S
.page 53                        ; set maximum lines/page to 55
.title                  CIRCUIT BREAKER CODE
;*****************************************************************************
;       TITLE                   P32.S
;       PROGRAMMER:             BRENDA KOVACEVIC
;       PURPOSE: THE FOLLOWING PROGRAM ENABLES THE Z8
;         MICROCONTROLLER TO RECEIVE DIAGNOSTIC INFORMATION
;         FROM A  SOLID STATE POWER CONTROLLER AND FEED THIS
;         INFORMATION BACK TO THE USER. FOUR INDICATIONS
;         ARE GIVEN; SHORT CIRCUIT, LOW POWER, OPEN LOAD,
;         AND 'OK' CONDITIONS ARE FLAGGED VIA THE USE OF LEDS
;         DRIVEN DIRECTLY BY THE Z8.
;
;*****************************************************************************

;*****************************************************************************
;                       EQUATES AND VARIABLES
;*****************************************************************************

        dbnce_actv: .EQU        R0      ; working register r0 is the '
                                        ; 'debounce timer active' flag

;*****************************************************************************
        .BEGIN
        .ORG    %8400
        int0:   jp      null_iret       ; unused interrupt
        int1:   jp      null_iret       ; unused interrupt
        int2:   jp      null_iret       ; unused interrupt
        int3:   jp      null_iret       ; unused interrupt
        int4:   jp      null_iret       ; unused interrupt.
        int5:   jp      T1_int          ; Counter/Timer 1 interrupt.

; First user-available location in RAM is at %8500
        .ORG %8500

start:
        jp      init                    ; jump around ascii data,
                                        ; strings,...

.ascii 'created 2/26/91 by BLK.'

init:
; 1) Set up interrupts:  Interrupts are configured here.

        di                              ;
        clr     imr                     ; mask out all interrupts
        clr     irq                     ; clear out any pending
                                        ; interrupts
        ei                              ; initialize interrupt request
                                        ; enable latch.
        di
        ld      IPR,#00001000b          ; irq5 has highest priority

        ld      IMR,#00100000b          ; enables interrupt 5(internal
                                        ; timer interrupt);masks off
                                        ; unused interrupts

; 2) Initialize Register pointer and stack:
        srp     #%50                    ; put scratch "working register"
                                        ; set at %50-%60
        ld      SPH,#%A0
        ld      SPL,#%00                ; top of external memory is the
                                        ; top of the stack
; 3) Initialize I/O Ports:

        ld      P01M,#11010011b         ; port 0 address and data, port 1
                                        ; output, external stack, normal
                                        ; timing
        ld      P2M,#00000111b          ; P20-P22 inputs; P23-P27
                                        ; outputs
        ld      P3M,#01000000b          ; Port 2 pullups open drain,P30-
                                        ; P33 int. inputs, P34-P37
                                        ; outputs  : P31 = Tin
; 4) Initialize Counter/Timers.

        ld      PRE1,#10000010b         ; set prescaler to 64 (decimal),
                                        ; single pass
        ld      T1,#10000000b           ; loads 256 in the timer, allows
                                        ; 11 ms count
        ld      TMR,#00101100b          ; load and enable t1, triggered
                                        ; internal clock mode
```

```
; 5) Initialize flag.
            clr   dbnce_actv                ; start with a clean debounce
                                            ; timer flag

; 6) All set up.  Enable interrupts and go!
            ei                              ; enable interrupts

status_check:
            tm    P3,#00000100b             ; check for bad condition
            jr    z,chk_pwr_cond            ; active low

good_status:
            ld    p2,#11100111b             ; sends power to 'OK' LED
            ld    p3,#00110000b             ; sends power to control input
                                            ; of MIC5013
            jr    ovrd_chk                  ; jump over subroutine call

chk_pwr_cond:
            call  cond_int                  ; check power circuits
ovrd_chk:
            tm    dbnce_actv,#1             ; If the emergency override has
                                            ; already been pressed, skip the
                                            ; test for emer. override.
            jr    nz,status_check           ; go back and start status check
                                            ; over the timer's already
                                            ; running
            tm    P3,#00000010b             ; Has the emergency override
                                            ; (P31) been pressed?
            jr    z,emer_ovrd               ; If yes, trigger debounce timer

            jr    status_check              ; no - start over again looking
                                            ; for status
emer_ovrd:
            or    dbnce_actv,#1             ; set debounce timer active flag
                                            ; to indicate that the timer's
                                            ; rolling.
            or    TMR,#00100011b            ; start debounce timer rolling
            jr    status_check              ; continue to wait for something
                                            ; else to happen

;*****************************************************************************************
;                       **************************
;                       Subroutine cond_int
;                       **************************
;*****************************************************************************************
;Subroutine:  P32 low , signals power malfunction
;Function:    Is tripped for any of the three malfunction conditions;
;Action       Subroutine cond_int reads port 2 to determine which
;             condition exists, and toggles the appropriate diagnostic bits
;             of port 2 or 3.
;*****************************************************************************************
cond_int:

short_test:
            tm    P2,#00000001b             ; see if P20 is high (short
                                            ; condition)
            jr    z,open_test               ; jump if no short
            and   P3,#11011111b             ; reset bit 5 of P3 to shut down
                                            ; MIC5013
            ld    P2,#10110111b             ; reset P26 to turn on
                                                    ; overcurrent LED
                                            ; fall through to test open load
                                            ; condition, open and short
                                            ; coincident indicates h/w fault
open_test:
            tm    P2,#00000010b             ; see if P21 is high (open load
                                            ; condition).
            jr    z,low_test                ; jump if no open load condition

            tm    P2,#00000001b             ; Do we also have a short
                                            ; condition (illegal)?
            jr    z,open_only               ; Jump if not

            jr    hw_fault                  ; Catastrophic h/w failure -
                                            ; indicate separately.
open_only:
            and   P3,#11011111b             ; reset P35 to shut down the
                                            ; MIC5013
            ld    P2,#11010111b             ; reset P25 to turn on "Open
                                            ; Load" LED
                                            ; fall through to low voltage test

low_test:
            tm    P2,#00000100b             ; see if P22 is high (low power
                                            ; condition).
            jr    z,end_cond_int            ; jump if no low-voltage fault

            and   P3,#11011111b             ; reset P35 to shutdown the
                                            ; MIC5013
            ld    P2,#01110111b             ; reset P27 to turn on "low
                                            ; power" LED
            jr    end_cond_int              ; done with power condition
                                            ; tests
hw_fault:
            and   P3,#11001111b             ; reset P34 to turn on "h/w fault"
                                            ; LED - we have a circuit
                                            ; breaker malfunction - and
                                            ; turn off the MIC5013!
            or    P2,#00010000b             ; turn off the "OK" LED, we have
                                            ; a HW fault and things are
                                            ; NOT OK!!

end_cond_int:
            ret

;*****************************************************************************************
;Interrupt:  Emergency Override Switch Timer Interrupt
;Function:  Keeps the MIC5013 alive while shorted in emergency situations.
;Action:    When the manual override switch is depressed, internal timer
;           T1 begins counting for 11 ms (see main). At the end of this debounce
;           routine, interrupt IRQ5 is asserted. This takes priority over the cond_int
;           subroutine, and keeps the control input to the MIC5013 on while
;           disabling the current sense by pulling the sense pin
;            to ground through transistor Q1.
;*****************************************************************************************
T1_int:
            di                              ; disable interrupts
            and   dbnce_actv,#0             ; reset 'debounce active' flag
            and   irq,#11011111b            ; Reset the interrupt source

            tm    P2,#00000001b             ; Don't take action if there is no
                                            ; short
            jr    nz, end_T1_int            ; Bail out.

            tm    P3,#00000010b             ; Check to see if override switch
                                            ; is still depressed
            jr    nz,end_T1_int             ; If not, then it was just noise
                                            ; triggered
                                            ; go back to main.
            or    P2,#00010000b             ; Sends power to Q1 to disable
                                            ; current sense
            or    P3,#00100000b             ; Makes sure the control input is
                                            ; still on
end_T1_int:

            ei
            iret



;*****************************************************************************************
;Interrupt:   Null interrupt
;Function:    Intercept any spurious interrupts.
;Action:      None. Just return from the interrupt.
;*****************************************************************************************
null_iret:
            and   irq,#00100000b            ; Reset any spurious pending
                                            ; interrupt.
            iret


            .END
```

Application Hint 5

Logic Controlled Power Switch

by Bob Wolbert

Introduction

In battery powered applications, such as laptop computers, power control has a major impact on battery life. For example, laptop or notebook computers often have a "sleep" mode, where the hard drive spins down and the display backlighting turns off while the RAM—containing valuable user data—is maintained. A microprocessor can easily make such power management decisions, but implementing the hardware for the actual switching can be complicated. "High-side" switching is required; i.e., the positive supply voltage must be controlled. Common grounds for busses and shielding limits the possibility of "low side" switching in a standard negative ground system. This note discusses a logic controlled power switch that simplifies microprocessor driven high-side supply switching.

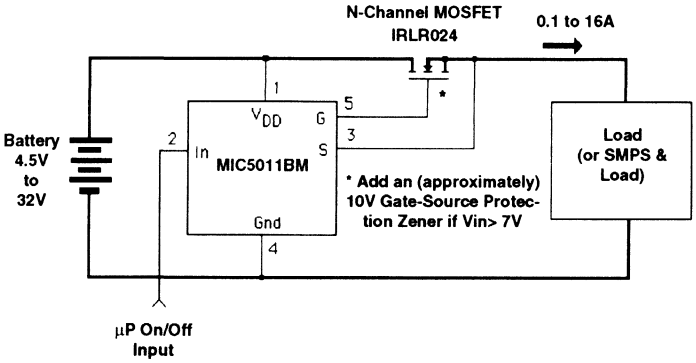


Figure 1. MIC5011 DB-1 Schematic Diagram.

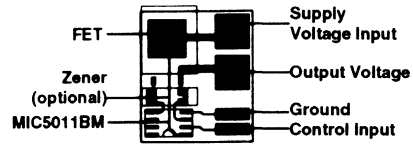


Figure 2. MIC5011 DB-1 Low Voltage Logic Controlled Power Switch

Power Switches

These high-side implementations have historically taken one of two forms: relays or PNP transistors. Both have drawbacks in that relatively large drive current is required: neither can be switched directly from a microprocessor port or standard logic. Mechanical relays are bulky, expensive, and have limited lifetimes. Bipolar transistors exhibit a fixed voltage drop that reduce margins, especially in 5V logic systems. This voltage drop has a devastating effect on defining battery end-of-life (per charge cycle).

Another method of power switching is the N-Channel DMOS FET. This FET has no inherent voltage drop, except for the $I \times r_{DS}$ loss, and requires almost no drive power; unfortunately, it does need a gate driving voltage of from 4V to 10V above the supply voltage in high-side applications. In other words, it is an *almost* ideal switch.

DMOS FET Advantages vs. Relays

- Non-mechanical (much longer life)
- No contact bounce
- Extremely low drive current requirement
- Smaller Size
- Lighter weight
- Lower cost

DMOS FET Advantages vs. PNP

- No fixed voltage drop
- Extremely low drive current requirement
- Larger Safe Operating Region

The Micrel MIC5010 Family

The MIC5011 and its relatives control the N-Channel DMOS FET by generating a gate drive control voltage 4V to 10V above the supply. Its CMOS compatible control input directly interfaces with microprocessors, and its BCD (Bipolar-CMOS-DMOS) construction allows nearly zero power drain in the OFF state. Pairing the MIC5011 with a low cost DMOS FET gives you a simple, reliable, easy-to-interface method of power management.

The MIC5011 is designed for this application and features:

- 4.5V to 32V Operation
- Very low OFF power consumption—0.1μA typical
- No external components required
- Built-in zener clamp for protecting standard DMOS gates
- Available in small 8-pin surface mount packages

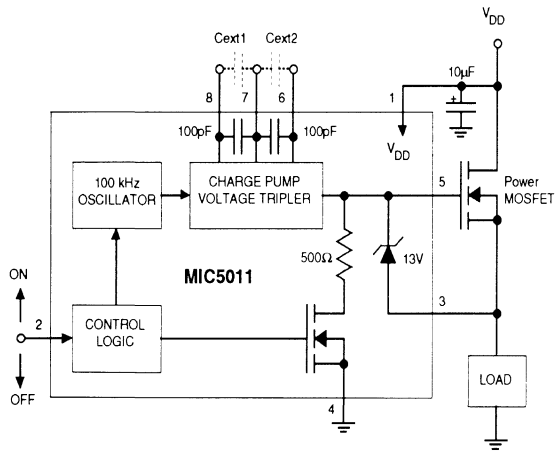


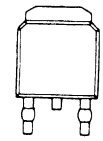
Figure 3. MIC5011 Block Diagram and Typical Application

The IRLR024 N-Channel DMOS FET

The 100mΩ surface mount IRLR024 is employed as the pass device in this demonstration circuit. This N-Channel DMOS FET features "Logic Level" gate drive voltages and can pass over 50A of peak current (limited by power dissipation considerations). Key features include:

- Low ON resistance—100mΩ maximum
- "Logic Level" gate threshold—ON at V_{GS}=4V; V_{GS}=5V for full enhancement.
- High pass current
- Surface mount package

One drawback of this "logic level" device is that its sensitive gate cannot withstand more than 10V of V_{GS} drive. Although the MIC5011 includes a protective zener clamp, the zener's 12.5V threshold is inadequate. With supply voltages from 4.5V to 7V, this is not a problem; however, above 7V, either an external zener clamp must be added to the MIC5011 gate drive output or else a standard threshold FET should be used.



G D S

Figure 4. IRLR024 DMOS FET

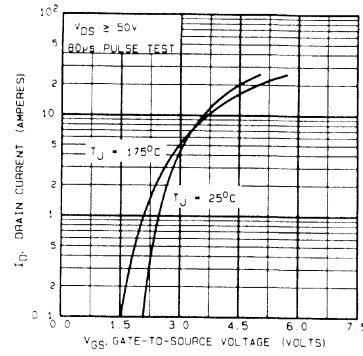


Figure 5. IRLR024 Characteristics

The Micrel MIC5011 DB-1 Demonstration Unit

This demonstration unit is built on a single sided board using surface mount techniques. It has been designed to control 4.5V to 7V supplies, but can easily be modified to use 4.5V to 32V supply voltages. The first thing you will notice from the schematic, Figure 1, is its simplicity; only two components are needed. The MIC5011 contains all of the necessary intelligence and the drive circuitry required by the N-Channel DMOS FET.

Four lines provide +V_{CC}, Switched-V_{CC}, Control, and Ground. V_{CC} and Switched-V_{CC} are current carrying lines, so thick, low resistances traces are necessary. Both Control and Ground are low current lines, so thin traces are sufficient.

Simply connect V_{CC} to 4.5V to 7V, Switched-V_{CC} to your load, Control to a logic output, and Ground. When the logic level is

high (greater than approximately 3.5V), the load will be energized. The IRLR024 will exhibit less than 100mΩ of resistance, so voltage drop, hence power loss, with typical peripherals will be low. Current drain of up to 16A continuous, 64A peak, can be drawn with suitable heatsinking (limit current to 3A without additional heatsinking). With a low logic level, the load will be switched off. Total power drain from the V_{CC} line will be negligible; only approximately 0.1μA (leakage current) flows.

Application Notes

Operating Voltages

This circuit, as designed, controls 4.5V to 7V digital supply voltages. If higher voltages must be switched, one of two modifications must be made. To switch widely varying supplies in the 4.5V to 32V range, use an approximately 7.5V zener clamp, such as the MLL4693 or equivalent, across the gate and source of the FET. If your application switches 7V to 32V, replace the "logic level" FET with a standard gate N-Channel DMOS FET, such as the IRF540, BUZ1LS2, or the SMP60N05. Regardless of the FET employed, the MIC5011 allows power control from a standard CMOS-level logic signal.

TO-220 Package FETs

The MIC5011-DB1 demonstration board also allows using a standard TO-220 package FET. Connect the gate and source to the zener diode pads, and solder the tab (drain) to the drain heatsink pad. Remove the center lead drain connection. The TO-220 tab will extend from the top of the board a short distance.

Faster Switching

If switching time is critical, adding a 1000pF capacitor from pins 6-7 on the MIC5011 will help. Another 1000pF capacitor from pins 7-8 will further accelerate switching time, but by a smaller margin.

Dual Independent Switches

When two separate circuits require switching, the MIC5012 Dual High Side FET Driver provides two independent drivers in a single 14-pin DIP or 16-pin surface mount package.

Over Current Protection

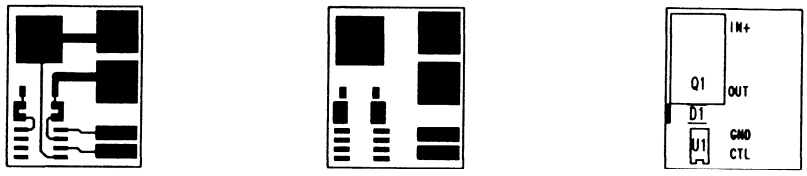
Replace the MIC5011 with the MIC5013 to enable over current protection with fault detection and signalling. See the MIC5013 datasheet for further information and suggested component values.

Parts List

- **MIC5011BM Surface mount MOSFET driver**
- **IRLR024 Surface mount DMOS FET**
- **MLL4693 Surface mount 7.5V zener diode (optional)**

Additional Notes

Although the MIC5011 datasheet specifically states that a minimum of 7V of supply voltage is required for high-side driving, the introduction of "logic level" N-Channel DMOS FETs requiring only 4V to 5V V_{GS} for full ON operation enables this minimum operating voltage to be lowered. The MIC5011 provides gate enhancement with supply voltages down to below 3.5V. Variations in the control voltage threshold, however, restrict low voltage operations to somewhat less than 4.5V (for lower voltage devices, please contact the factory).



Component Side Solder Mask Silk Screen

Figure 6. MIC5011 DB-1 Board Layout

Application Hint 9

Low Voltage Operation of the MIC5014 Family

by Brenda Kovacevic

Introduction

The current trend for more efficient use of power has led to a new standard in logic based systems: the use of 3.3V logic as opposed to 5V logic. Efficient power management is especially important in battery based systems such as portable laptop/notebook PCs and cellular phones where maximum use time is determined by battery life. **The MIC5014 family has a minimum required supply rail of 2.75V, which is the lowest required voltage of any high side driver in the industry!** This makes the MIC5014 family ideal for use in any low voltage environment where power switching is necessary. This note briefly describes the characteristics of these devices at low voltages, and shows several example applications where the low voltage feature is used.

Typical Parameters at $V^+ = 3.3V$

Table I shows the typical parameters expected at a 3.3V supply voltage. At 15µA quiescent current and 35µA operating current, we offer very little battery drain at this voltage. Also worthy of attention is the fact that these devices offer a full 4.5V gate enhancement with a supply voltage of only 3.0V! Perhaps the only drawback is the rise time at these low voltages, which is on the order of 35 to 40ms. For most power switching applications in this voltage range, this has not been seen to present difficulties and is a small price to pay for the greatly lowered battery drain. If faster switching speeds are desired, the rise time can be improved to 20 to 30ms by bootstrapping off the positive supply, as shown in figure 1. Faster times than this can be attained by increasing the size of the bootstrap capacitor at the expense of the additional space required. Fall times remain on the order of 6 to10µs.

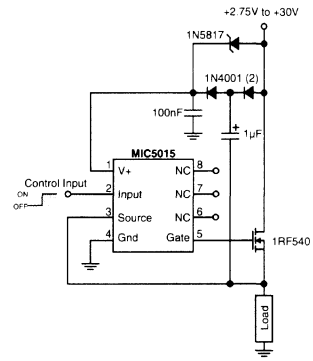


Figure 1. Low Voltage Bootstrapped High Side Switch

Table 1: Typical Parameters at $V^+ = 3.3V$

Parameter	Typical Value	Units
Supply Current,Off State	15	µA
Supply Current,On State	35	µA
High Side Turn-On Time (C_L = 1300 pF)	35	ms
Turn-Off Time	6	µs
Gate Enhancement (V_{GATE} - V_{SUPPLY})	4.5	V
Logic Input Current (High State)	1	µA

Typical Low Voltage Applications

Sleep Mode Switching

One commonly employed technique for extending battery life is the use of a "sleep mode" switch, in which the microprocessor shuts down all the functions that represent power drain after a preset time of nonuse while maintaining the system memory. This type of a switch must typically be a high side switch, or a switch that controls the availablity of the positive supply, as standard computer or logic based systems often have common ground busses and /or shielding.

The MIC5016 plus two logic level FETs make an ideal dual sleep mode switch (figure 2) without the bulk and unreliability of relays or the voltage drop of bipolar transistors (See Application Hint 5 for more information plus a board layout for sleep mode switching with regards to our MIC5011 high side driver).

A logic level FET is very similar to a regular power FET except for the threshold voltage requirements, which are VGS = 4 V for turn-on and 5 V for full enhancement. A regular power FET would require a minimum of 10V for full enhancement. This feature makes the logic level FET ideal for this kind of switching. The only drawback it has is that it's gate cannot withstand more than 10V of enhancement. The MIC5014/5016 devices are equipped with an internal zener clamp, but at 15V it will not save us here! We recommend that an external zener clamp or regular power FET be used if a supply higher than 4V is required.

As the MIC5014 is pin to pin compatible with the MIC5011, the board layout for a single sleep mode switch as featured in Application Hint 5 will also work for the MIC5014.

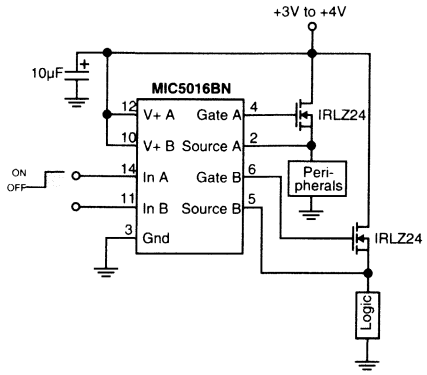


Figure 2: 3 to 4 V Dual Sleep Mode Switch

Low Battery Sense and Disconnect

When a battery is discharged to the point that the load goes significantly out of regulation, it is often beneficial to disconnect the load from the battery to prevent further discharge. In the case of NiCd or NiMH batteries, repeated deep discharging has a negative impact on battery life. A simple scheme can be formulated using the MIC2951 super low drop out regulator to generate a well regulated 3.3V supply from four 1.2V battery cells. When the output drops to below 5% of the rated value, the ERROR flag goes low, pulling down the RESETof the latch which shuts down the control input to the MIC5014. This turns off the MOSFET switch connecting the battery to the regulator. It is important to hold the SET input to the latch low for 30 to 40ms on start-up to allow the regulator to kick in. This output can also be fed to a microcontroller, signalling the user that it is time to charge his batteries.

Although it is possible to use feedback from the ERROR output to the shutdown input of the MIC2951 to perform this function, the addition of the MIC5014 and FET switch results in less current drain (20 to 25µA extra for the MIC5014 plus latch as opposed to the current required to bias and drive a bipolar transistor). It also allows the MIC2951 to act as the central controlling point for shutdown in applications where the unregulated battery voltage is fed to other subsystems, such as an SMPS converter, in addition to the MIC2951.

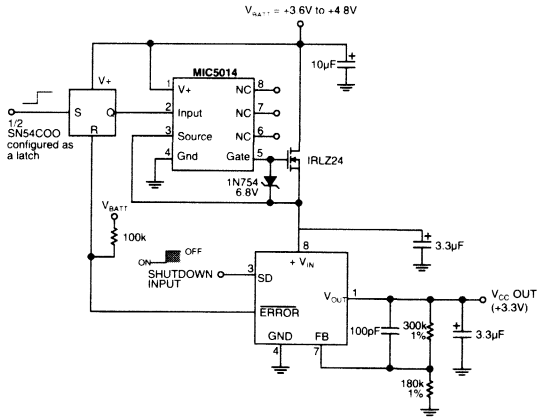


Figure 3: Low Battery Shutdown Switch

SECTION 3: LATCHED DRIVERS

Latched Driver Selection Guide

All Micrel Latched Drivers are available in die form. Special package options available on most latched drivers: please contact factory for details.

DEVICE	Sink Output	Source Output	Number of Output	Maximum Voltage	Nominal Drive Current (mA)	Parallel Input	Serial Input	Over T, I, UVLO Protection	Temperature	PACKAGE
MIC4807 Protected Addressable Low-Side Driver	•		8	80	200	•		•	A	18-pin CerDIP
									B	18-pin PDIP
MIC5800 Latched Driver	•		4	50	500	•			A	14-pin CerDIP
									B	14-pin PDIP, SOIC; 15-SIP
MIC5801 Latched Driver	•		8	50	500	•			A	22-pin CerDIP
									B,C	22-pin PDIP, 28-pin PLCC
MIC58P01 Protected Latched Driver	•		8	80	500	•		•	A	22-pin CerDIP
									B	22-pin PDIP, 28-pin PLCC
MIC5821 Serial Input Latched Driver	•		8	50	500		•		B,C	16-pin PDIP
MIC5822 Serial Input Latched Driver	•		8	80	500		•		A	16-pin CerDIP
									B	16-pin PDIP
MIC5841 Serial Input Latched Driver	•		8	50	500		•		A	18-pin CerDIP
									B	18-pin PDIP, SOIC, 20-pin PLCC
MIC5842 Serial Input Latched Driver	•		8	80	500		•		A	18-pin CerDIP
									B	18-PDIP, SOIC, 20-PLCC
MIC58P42 Protected Serial Input Latched Driver	•		8	80	500		•	•	A	18-pin CerDIP
									B	18-pin PDIP, SOIC, 20-pin PLCC
MIC5891 Latched Source Driver		•	8	50			•		A	16-pin CerDIP
									B	16-pin PDIP, SOIC,
MIC59P50 Protected Parallel Input Latched Driver	•		8	80	500	•		•	A	24-pin CerDIP (skinny)
									B	24-pin PDIP, SOIC, 28-pin PLCC
MIC59P60 Protected Serial Input Latched Driver	•		8	80	500		•	•	A	20-pin CerDIP
									B	20-pin PDIP, SOIC, PLCC

Temperature Code:

A = –55°C to +125°C
B = –40°C to +85°C
C = 0°C to +70°C

MIC4807

80V, 8-Channel, Addressable Low Side Driver

General Description

The MIC4807 is an 80V, 8-channel, addressable low side driver with latches and TTL/CMOS compatible logic inputs. Each logic input is composed of a comparator with a 1.4V bandgap-derived reference serving as the trip point. The addresses (A_{IN}, B_{IN}, and C_{IN}) and Data-in logic inputs have an internal 50µA pull-up current source, while the Output Enable (OE), Chip Select ($\overline{CS}$), and Clear logic inputs have an internal 75µA pull-down sink. If the logic lines to the MIC4807 are severed, these currents guarantee that the outputs will turn OFF.

Individual latches in the MIC4807 are selected by a binary address presented at inputs A_{IN}, B_{IN}, and C_{IN}. Data-in is directed to the addressed latch while $\overline{CS}$ is held low, allowing an individual output to be pulse-width modulated. When $\overline{CS}$ is set high again, the last Data-in is stored in the latch. If Data-in = "1", the addressed output is turned on, and if Data-in = "0", the addressed output is turned off.

Information presented to Data-in and the address inputs is transferred to the latches while $\overline{CS}$ is pulled low. For application, where several outputs must be (Continued)

Features

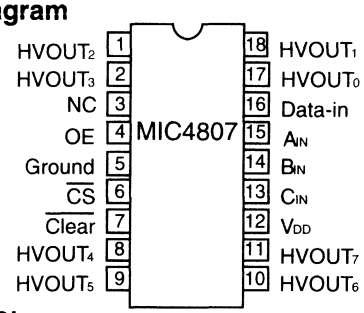
- 4.5V to 16V Operation
- Eight 80V 100mA Outputs
- Off-state Leakage less than 10µA at 25°C
- Short-Circuit Proof
- Thermal Shutdown with Hysteresis
- DMOS Output Devices ($R_{ON} \leq 7\Omega$ at 25°C)

Applications

- Lamp Drivers
- Solenoid Drivers
- Display Drivers
  - -Electroluminescent
  - -Vacuum Fluorescent
  - -Plasma
- Relay Drivers
- Print Head Drivers
- Heater Drivers
- Power Semiconductor Drivers
- Security Systems
- Environmental Controls
- Process Controllers

3

Pin Diagram

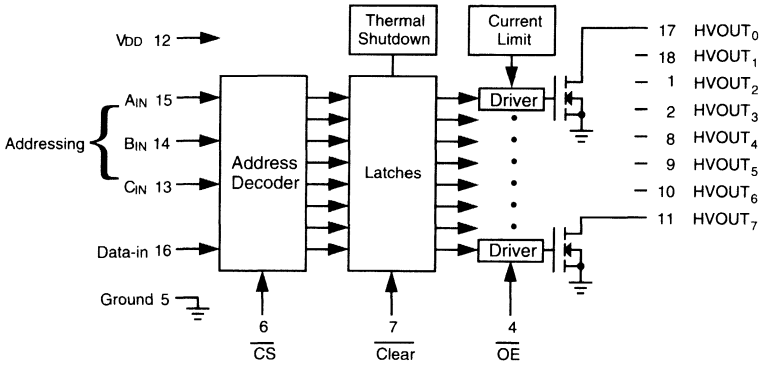


Ordering Information

Part Number	Operating Temperature-Range	Package
MIC4807AJB*	-55°C to 125°C	18-Pin Ceramic DIP
MIC4807BN	-40°C to 85°C	18-Pin Plastic DIP

* AJB indicates units screened to MIL-STD 883, Method 5004, condition B, and burned-in for 1-week.

Block Diagram



General Description (Continued)

turned on simultaneously, Gray Code address sequencing can be applied to Ain, Bin, Cin, while Data-in is held high and $\overline{CS}$ is held low. Data-in will be transferred to each address in turn, without the need to toggle $\overline{CS}$. Similarly, a set of outputs could be simultaneously turned off by setting Data-in low. Gray Code ensures that no intermediate addresses are inadvertently accessed. A typical Gray Code is 0, 1, 3, 2, 6, 7, 5, 4.

Each output drive circuit has a high-voltage, power DMOS device configured as a transconductance loop. This loop limits the output current to typically 200mA. While current limiting keeps the output device within its allowable safe-operating area (SOA), the power dissipation may be excessive. Long-term survival is guaranteed by thermal shutdown.

When operated below current limit, the outputs appear as small-valued resistors (typically 5.1Ω at 25°C) connected to ground. The "ON" resistance (R_{ON}) has a strong, positive temperature coefficient (approximately 7500 ppm/°C) which promotes current sharing if two or more outputs are paralleled.

Absolute Maximum Ratings (Notes 1, 2 and 3)

Output Voltage (V_{OUT}, OFF)	100V
Supply Voltage (V_{DD})	16.5V
Logic Input Voltage (V_{IN})	−0.3V TO V_{DD} + 0.3
Continuous Output Current (I_{OUT})	Internally Limited
Power Dissipation (P_D, Note 2)	Internally Limited
Ambient Temperature (T_A):	
B Version	−40°C to +85°C
A version	−55°C to +125°C
Maximum Junction Temperature (T_{JMAX})	150°C
Storage Temperature	−65°C to +150°C
θ_{JA} - Plastic DIP	130°C/W
θ_{JA} - Ceramic DIP	90°C/W

Electrical Characteristics: (Note 6) MIC4807BN, T_A = 25°C, V_{DD} = 15V unless otherwise specified (see Test Circuit).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DD}	Supply Voltage		4.5		16	V
I_{DD}	Supply Current	OE = L (Note 3) OE = H (Note 4)		5.5 1.5	10 3	mA mA
V_{IN} (0)	Logic Input Voltage	4.5V ≤ V_{DD} ≤ 16V			0.8	V
V_{IN} (1)			2.0			V
I_{IN} (0)	Logic Input Current for A_{IN}, B_{IN}, C_{IN}, and Data-in	V_{IN} = 0V	−150	−70	−25	µA
I_{IN} (1)	Logic Input Current for $\overline{CS}$, OE, and $\overline{Clear}$	V_{IN} = V_{DD}	25	130	250	µA
I_{OUT}	Output Leakage Current	OE = 0V, V_{OUT} = 80V		1	10	µA
R_{ON}	Output "ON" Resistance	Output is ON, V_{OUT} = 0.7V, V_{DD} = 10V		5.1	7	Ω
I_{SC}	Short Circuit Current	Output is ON< V_{OUT} = 50V 10V ≤ V_{DD} ≤ 15V (Note 5)	140	190	250	mA
V_{OUT}	Output Voltage (OFF)				80	V
V_{OUT}	Output Voltage (ON)	I_{OUT} = 50mA, V_{DD} = 10V I_{OUT} = 100mA, V_{DD} = 10V		0.26 0.51	0.35 0.7	V V
	Data and Address Set-up Time	V_{DD} = 10V for all timing tests (A, see **Timing Diagram**)	400			ns
	Data and Address Hold Time	(B)	50			ns
	$\overline{CS}$ Pulse Width	(C)	500			ns
	Turn-on Delay	(D)			2.5	ns

Electrical Characteristics: (Note 6) MIC4807BN, T_A = 25°C, V_{DD} = 15V unless otherwise specified (see Test Circuit).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Turn-Off Delay	(E)			2.5	µs
	Output Disable Response Time	(F)			2	µs
	Output Enable Response Time	(G)			2	µs
	$\overline{\text{Clear}}$ Response Time	(H)			2.5	µs
	$\overline{\text{Clear}}$ Pulse Width	(I)	500			ns

Electrical Characteristics: (Note 6) MIC4807AJB, T_A = –55°C to +125°C, V_{DD} = 15V unless otherwise specified (see Test Circuit).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DD}	Supply Voltage		4.5		16	V
I_{DD}	Supply Current	OE = L (Note 3) OE = H (Note 4)			15 4	mA mA
V_{IN} (0)	Logic Input Voltage	4.5V ≤ V_{DD} ≤ 16V			0.8	V
V_{IN} (1)			2.0			V
I_{IN} (0)	Logic Input Current for A_{IN}, B_{IN}, C_{IN}, and Data-in	V_{IN} = 0V	–250		–10	µA
I_{IN} (1)	Logic Input Current for $\overline{\text{CS}}$, OE, and $\overline{\text{Clear}}$	V_{IN} = V_{DD}	25		400	µA
I_{OUT}	Output Leakage Current	OE = 0V, V_{OUT} = 80V		5.1	7	µA
R_{ON}	Output "ON" Resistance	Output is ON, V_{OUT} =0.7V,V_{DD}=10V			12	Ω
I_{SC}	Short Circuit Current	Output is ON< V_{OUT} = 50V 10V ≤ V_{DD} ≤ 15V (Note 5)	100		300	mA
V_{OUT}	Output Voltage (OFF)				80	V
V_{OUT}	Output Voltage (ON)	I_{OUT} = 50mA,V_{DD} = 10V I_{OUT} = 100mA, V_{DD} = 10V			0.6 1.2	V V
	Data and Address Set-up Time	V_{DD} = 10V for all timing tests (A, see **Timing Diagram**)	700			ns
	Data and Address Hold Time	(B)	50			ns
	$\overline{\text{CS}}$ Pulse Width	(C)	1000			ns
	Turn-on Delay	(D)			5	µs

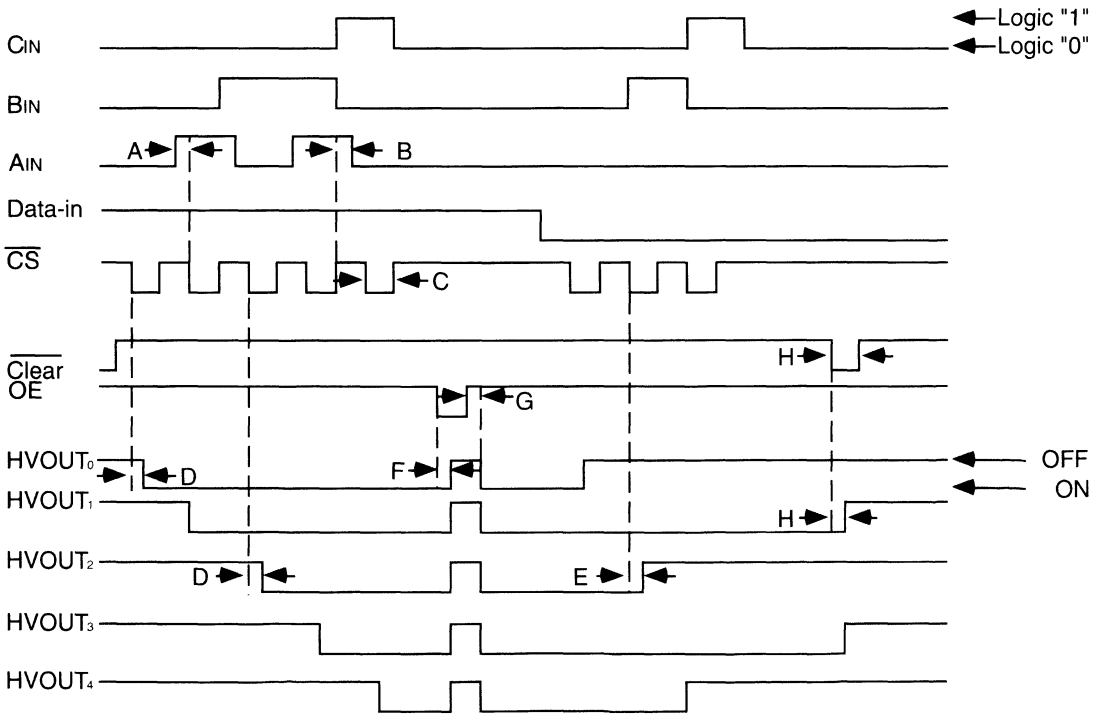
3

Electrical Characteristics: (Note 6) MIC4807BN, T_A = 25°C, V_{DD} = 15V unless otherwise specified (see Test Circuit).

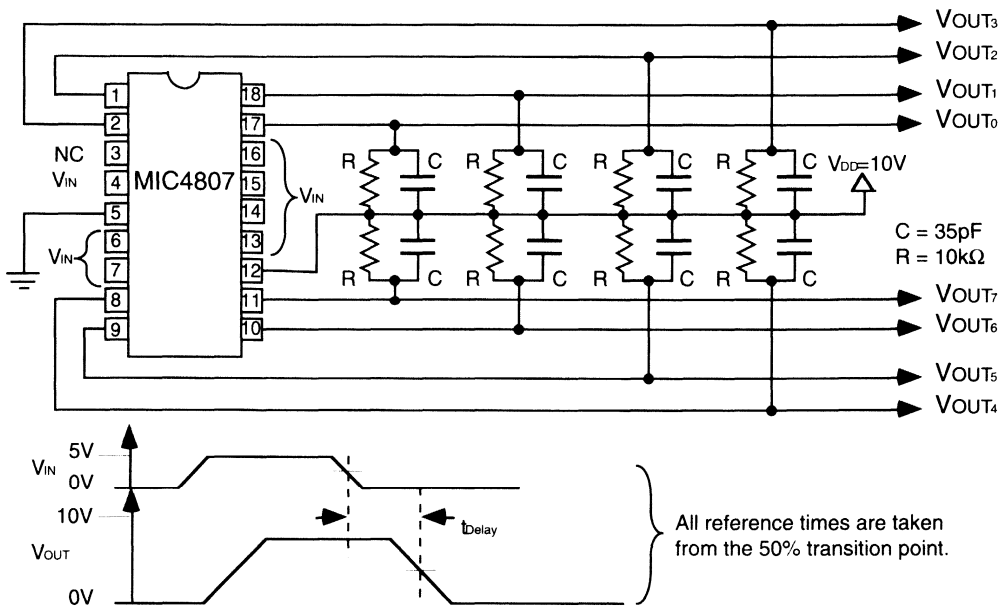
Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Turn-Off Delay	(E)			5	µs
	Output Disable Response Time	(F)			4	µs
	Output Enable Response Time	(G)			4	µs
	$\overline{\text{Clear}}$ Response Time	(H)			5	µs
	$\overline{\text{Clear}}$ Pulse Width	(I)	1000			ns

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Electrical specifications do not apply when operating the device beyond its specified operating ratings.
Note 2: The junction temperature is internally limited by a thermal shutdown circuit. The maximum power dissipation is a function of T_{JMAX}, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$. If this dissipation is exceeded, the die temperature will rise above 150°C, and the MIC4807 will go into thermal shutdown.
Note 3: All outputs are off when **OUTPUT ENABLE** is pulled low.
Note 4: All outputs are turned on during this test.
Note 5: Pulse testing is used to avoid thermal shutown.
Note 6: Minimum and Maximum limits are tested and 100% guaranteed over the temperature range specified. Typicals are measured at 25°C and represent the most likely parametric norm.

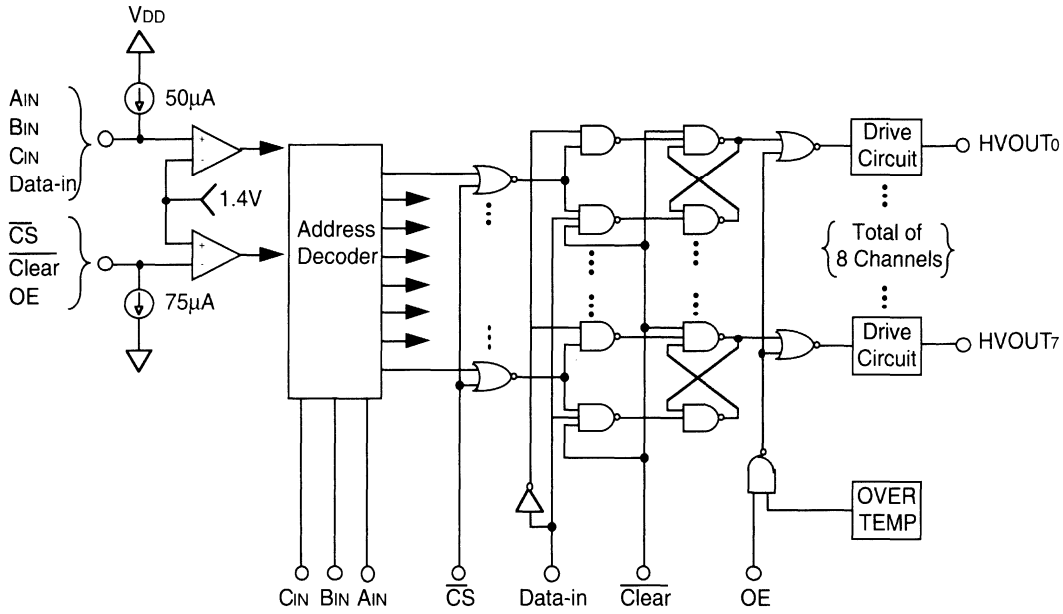
Timing Diagram



Test Circuit and AC Waveform Measurement Standards



Equivalent Logic Diagram



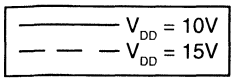
Truth Table

$\overline{CS}$	$\overline{Clear}$	Data-In	C_{IN}	B_{IN}	A_{IN}	OE	$HVOUT_0$	$HVOUT_1$	$HVOUT_2$	$HVOUT_3$	$HVOUT_4$	$HVOUT_5$	$HVOUT_6$	$HVOUT_7$	Functional Mode
X	L	X	X	X	X	X	H	H	H	H	H	H	H	H	Clear
H	H	X	X	X	X	H	P	P	P	P	P	P	P	P	Memory
L	H	D	L	L	L	H	$\overline{D}$	P	P	P	P	P	P	P	Address $HVOUT_0$
L	H	D	L	L	H	H	P	$\overline{D}$	P	P	P	P	P	P	Address $HVOUT_1$
L	H	D	L	H	L	H	P	P	$\overline{D}$	P	P	P	P	P	Address $HVOUT_2$
L	H	D	L	H	H	H	P	P	P	$\overline{D}$	P	P	P	P	Address $HVOUT_3$
L	H	D	H	L	L	H	P	P	P	P	$\overline{D}$	P	P	P	Address $HVOUT_4$
L	H	D	H	L	H	H	P	P	P	P	P	$\overline{D}$	P	P	Address $HVOUT_5$
L	H	D	H	H	L	H	P	P	P	P	P	P	$\overline{D}$	P	Address $HVOUT_6$
L	H	D	H	H	H	H	P	P	P	P	P	P	P	$\overline{D}$	Address $HVOUT_7$
X	X	X	X	X	X	L	H	H	H	H	H	H	H	H	Blanking

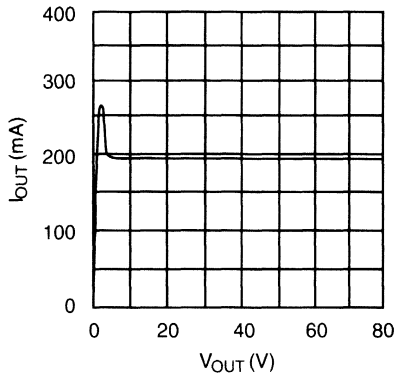
L = Low Logic Level
H = High Logic Level
D = Data (High or Low)
X = Don't Care
P = Previous State

Typical DC Output Characteristics for the "On" State:

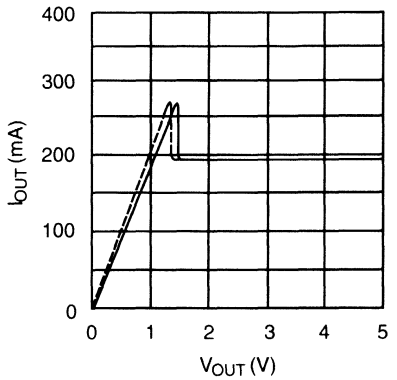
(V_{DD} = 10V and T_A = 25°C unless other wise specified)



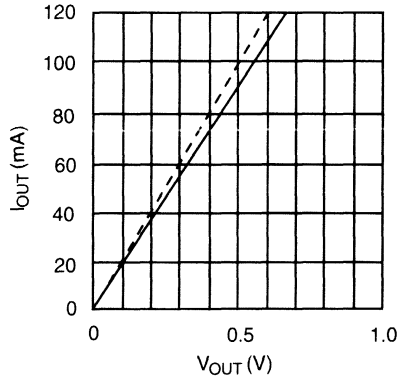
SHORT CIRCUIT CURRENT



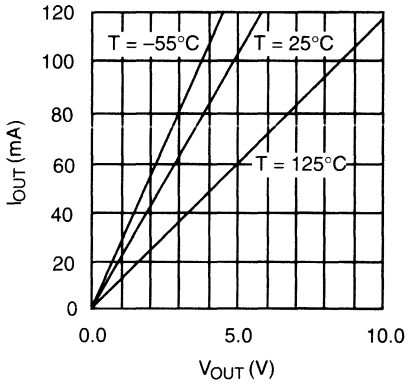
EXPANDED VERSION OF SHORT CIRCUIT CURRENT FOR LOW OUTPUT VOLTAGE (V_{OUT})



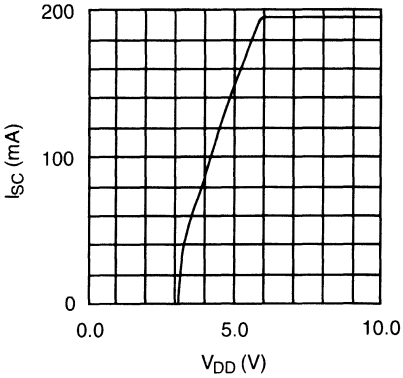
I_{OUT} FOR SEPARATE V_{DD}



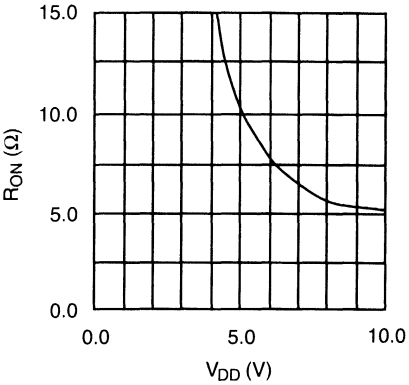
I_{OUT} AT 3 TEMPERATURES



SHORT CIRCUIT CURRENT LIMIT (I_{SC})



ON RESISTANCE (R_{ON})



3

Pin Description

Pin No.	Pin Name	Functional Description
5	Ground	Electrical ground to chip substrate.
12	V_{DD}	Positive logic supply voltage (10V-15V).
1, 2, 8, 9,10, 11, 17,18	$HVOUT_0$ through $HVOUT_7$	These are the high voltage (HV) open outputs, each of which is capable of sinking 100mA when switched on, and standing off 80V when switched off. In addition, each output channel is equipped with an analog current limiter to protect it from shorts to the positive high voltage supply. When an output is shorted (up to 80V), a maximum of 225mA (200mA nominal) will flow through it to ground.
13, 14, 15	C_{IN}, B_{IN}, $\&A_{IN}$	When these inputs are combined together they form the BCD address used to select the desired output. Each input is TTL compatible with an internal pull-up current source of 50mA.
6	CS	When $\overline{CS}$ is at logic "0" the device is actively addressed, and when $\overline{CS}$ is at logic "1" the decoded address and input Data are inhibited, making the part unaddressable. $\overline{CS}$ is TTL compatible with an internal pull-down current sink of 75µA.
7	$\overline{Clear}$	$\overline{Clear}$ resets all the outputs to the off state when pulled to logic "0", and is TTL compatible with an internal pull-down current sink of 75µA.
16	Data-in	Data-in determines the state of the output being addressed. When Data-in is at logic "0" the addressed output is turned off, and when Data-in is at logic "1" the addressed output is turned on. Data-in is TTL compatible with an internal pull-up current source of 50µA.
4	OE	OE allows the bank of eight outputs to be duty cycled together. When OE is at logic "1" the outputs are enabled to follow their respective latches, and when OE is at logic "0" all the outputs are turned off. OE is TTL Compatible with a pull-down current sink of 75µA.

MIC5800/5801

4/8 Bit Parallel-Input Latched Driver Family

General Description

The MIC5800/5801 latched drivers are high-voltage, high-current integrated circuits comprised of four or eight CMOS data latches, a bipolar Darlington transistor driver for each latch, and CMOS control circuitry for the common CLEAR, STROBE, and OUTPUT ENABLE functions.

The bipolar/MOS combination provides an extremely low-power latch with maximum interface flexibility. MIC5800 contains four latched drivers; MIC5801 contains eight latched drivers.

Data input rates are greatly improved in these devices. With a 5 V supply, they will typically operate at better than 5 MHz. With a 12 V supply, significantly higher speeds are obtained.

The CMOS inputs are compatible with standard CMOS, PMOS, and NMOS circuits. TTL or DTL circuits may require the use of appropriate pull-up resistors. The bipolar outputs are suitable for use with relays, solenoids, stepping motors, LED or incandescent displays, and other high-power loads.

Both units have open-collector outputs and integral diodes for inductive load transient suppression. The output transistors are capable of sinking 500 mA and will sustain at least 50 V in the OFF state. Because of limitations on package power dissipation, the simultaneous operation of all drivers at maximum rated current can only be accomplished by a reduction in duty cycle. Outputs may be paralleled for higher load current capability.

Features

- 4.4 MHz Minimum Data Input Rate
- High-Voltage, Current Sink Outputs
- Output Transient Protection
- CMOS, PMOS, NMOS, and TTL Compatible Inputs
- Internal Pull-Down Resistors
- Low-Power CMOS Latches

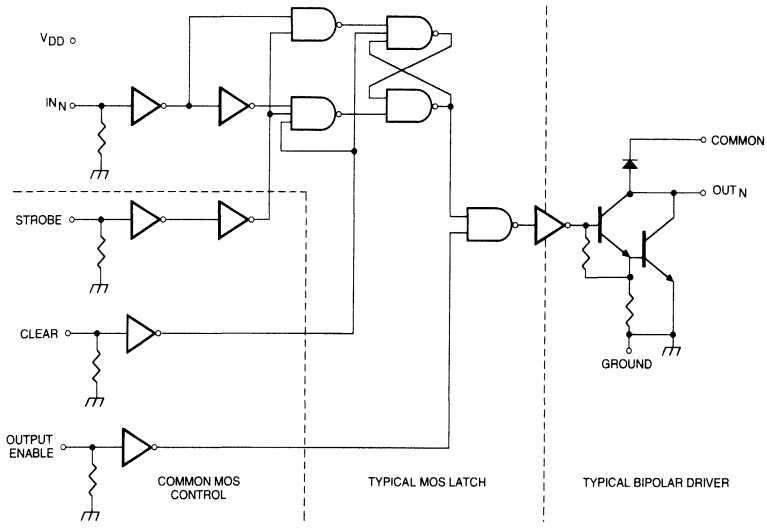
Ordering Information

Part Number	Temperature Range	Package
MIC5800BN	– 40°C to + 85°C	14–Pin Plastic DIP
MIC5800AJ	– 55°C to +125°C	14–Pin CERDIP
MIC5800AJB*	– 55°C to +125°C	14–Pin CERDIP
MIC5800BM	– 40°C to + 85°C	14–Pin SOIC
MIC5800BT	– 40°C to + 85°C	15–Pin Power SIP
MIC5801CN	0°C to +70°C	22–Pin Plastic DIP
MIC5801BN	– 40°C to +85°C	22–Pin Plastic DIP
MIC5801AJ	– 55°C to +125°C	22–Pin CERDIP
MIC5801AJB*	– 55°C to +125°C	22–Pin CERDIP
MIC5801BV	– 40°C to + 85°C	28–Pin PLCC
MIC5801BWM	– 40°C to +85°C	24–Pin SOIC

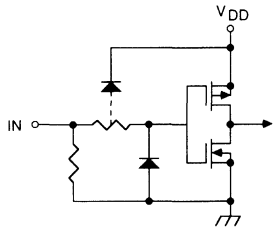
* AJB indicates units screened to MIL-STD 883, Method 5004, condition B, and burned-in for 1-week. MIC5800 is available in a Standard Military Drawing version. Order DESC # 5962-8764002WX. The MIC5801 is available as DESC # 5962-8764001WX. Please contact factory for full military temperature range specifications.

3

Functional Diagram



Typical Input



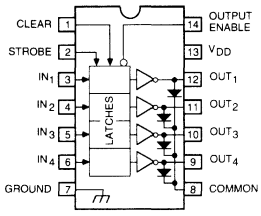
Absolute Maximum Ratings: (Notes 1-8)

at +25°C Free-Air Temperature

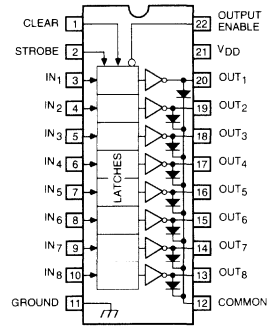
Output Voltage, V_{CE}	50 V
Output Voltage, V_{CE} continuous	35 V
Supply Voltage, V_{DD}	15 V
Input Voltage Range, V_{IN}	–0.3 V to V_{DD} + 0.3 V
Continuous Collector Current, I_C	500 mA
Package Power Dissipation:	
MIC5800 Plastic DIP (Note 1)	2.1 W
MIC5801 Plastic DIP (Note 2)	2.5 W
MIC5800 SOIC (Note 3)	1.0 W
MIC5801 PLCC (Note 4)	2.25 W
MIC5800 CERDIP (Note 5)	2.8 W
MIC5801 CERDIP (Note 6)	3.1 W
MIC5800 Power SIP(Note 7)	3.575 W
Operating Temperature Range, T_A	–40°C to +85°C
Storage Temperature Range, T_S	–65°C to +125°C

Note 1: Derate at 16.7 mW/°C above T_A = +25°C
Note 2: Derate at 20 mW/°C above T_A = +25°C
Note 3: Derate at 8.5 mW/°C above T_A = +25°C
Note 4: Derate at 18.2 mW/°C above T_A = +25°C
Note 5: Derate at 21.7 mW/°C above T_A = +25°C
Note 6: Derate at 25 mW/°C above T_A = +25°C
Note 7: Derate at 28.6 mW/°C above T_A = +25°C
Note 8: Micrel CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.

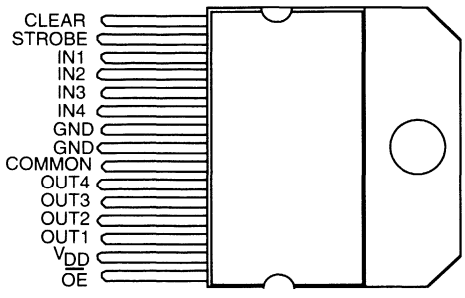
Pin Configuration



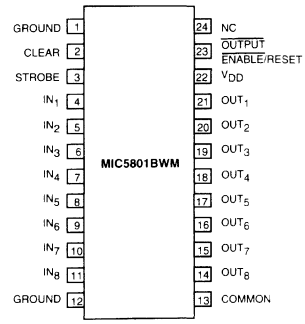
MIC5800BN,AJ,BM



MIC5801BN,CN,AJ

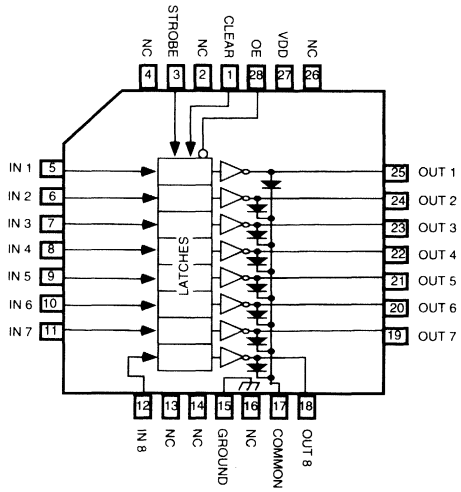


MIC5800BT



MIC5801BWM

Pin Configurations (continued)

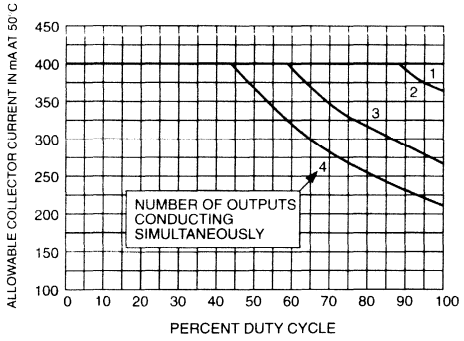


MIC5801BV

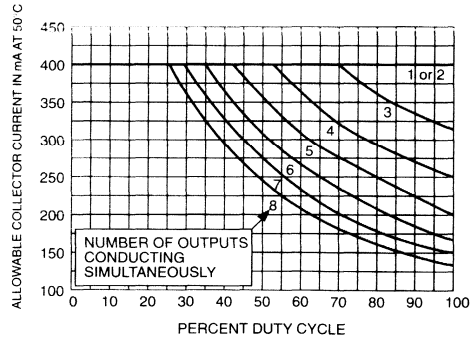
3

Allowable Output Current As A Function of Duty Cycle

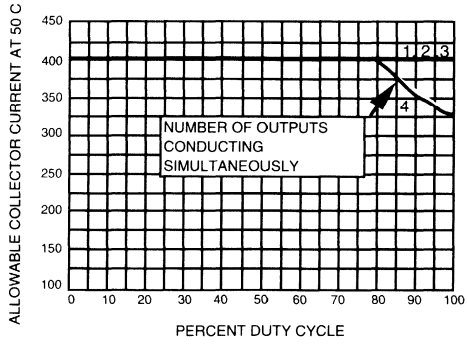
MIC5800BN,AJ,AJB,BM



MIC5801CN,BN,AJ,AJB



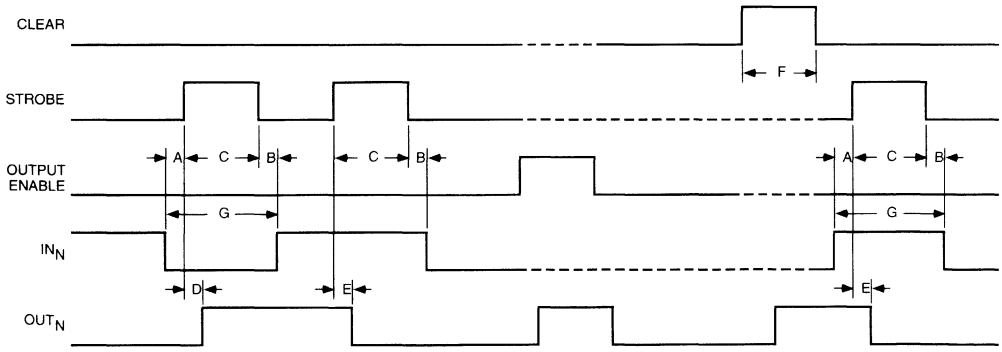
MIC5800BT



Electrical Characteristics: at T_A = +25°C, V_{DD} = 5V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Output Leakage Current	I_{CEX}	V_{CE} = 50 V, T_A = +25°C			50	µA
		V_{CE} = 50 V, T_A = +70°C			100	
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 100 mA		0.9	1.1	V
		I_C = 200 mA		1.1	1.3	
		I_C = 350 mA, V_{DD} = 7.0 V		1.3	1.6	
Input Voltage	$V_{IN(0)}$				1.0	V
	$V_{IN(1)}$	V_{DD} = 12 V	10.5			
		V_{DD} = 10 V	8.5			
		V_{DD} = 5.0 V (See Note)	3.5			
Input Resistance	R_{IN}	V_{DD} = 12 V	50	200		kΩ
		V_{DD} = 10 V	50	300		
		V_{DD} = 5.0 V	50	600		
Supply Current	$I_{DD(ON)}$ (Each Stage)	V_{DD} = 12 V, Outputs Open		1.0	2.0	mA
		V_{DD} = 10 V, Outputs Open		0.9	1.7	
		V_{DD} = 5.0 V, Outputs Open		0.7	1.0	
	$I_{DD(OFF)}$ (Total)	V_{DD} = 12 V, Outputs Open, Inputs = 0 V			200	µA
		V_{DD} = 5.0 V, Outputs Open, Inputs = 0 V		50	100	
Clamp Diode Leakage Current	I_R	V_R = 50 V, T_A = +25°C			50	µA
		V_R = 50 V, T_A = +70°C			100	
Clamp Diode Forward Voltage	V_F	I_F = 350 mA		1.7	2.0	V

NOTE : Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to insure a minimum logic "1".



Timing Conditions

(Logic Levels are V_{DD} and Ground)

A. Minimum data active time before strobe enabled (data set-up time) ..... 50 ns
B. Minimum data active time after strobe disabled (data hold time) ..... 50 ns
C. Minimum strobe pulse width ..... 125 ns
D. Typical time between strobe activation and output on to off transition ..... 500 ns
E. Typical time between strobe activation and output off to on transition ..... 500 ns
F. Minimum clear pulse width ..... 300 ns
G. Minimum data pulse width ..... 225 ns

Truth Table

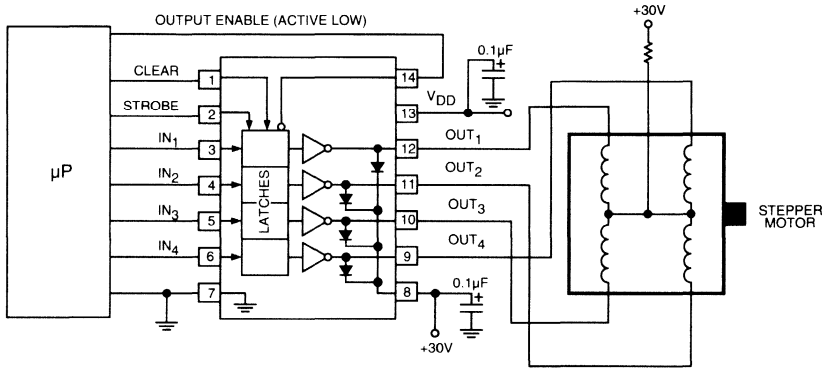
IN_N	Strobe	Clear	Output Enable	OUT_N t-1	OUT_N t
0	1	0	0	X	OFF
1	1	0	0	X	ON
X	X	1	X	X	OFF
X	X	X	1	X	OFF
X	0	0	0	ON	ON
X	0	0	0	OFF	OFF

X = Irrelevant
t-1 = previous output state
t = present output state

Information present at an input is transferred to its latch when the STROBE is high. A high CLEAR input will set all latches to the output OFF condition regardless of the data or STROBE input levels. A high OUTPUT ENABLE will set all outputs to the off condition, regardless of any other input conditions. When the OUTPUT ENABLE is low, the outputs depend on the state of their respective latches.

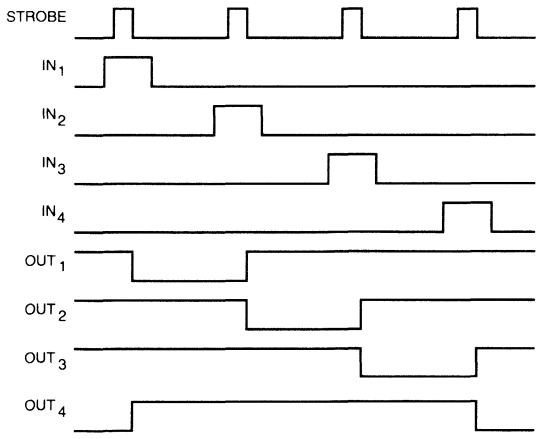
Typical Application

Unipolar Stepper-Motor Drive

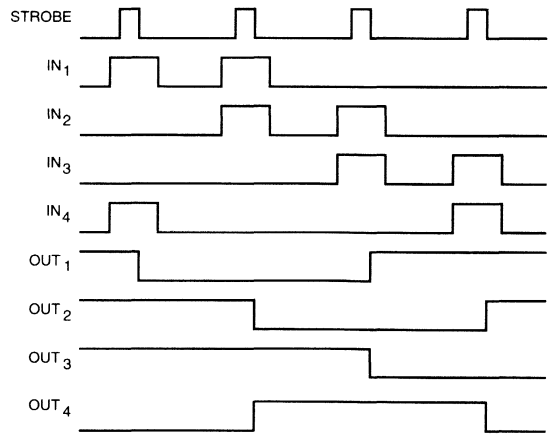


MIC5800

UNIPOLAR WAVE DRIVE

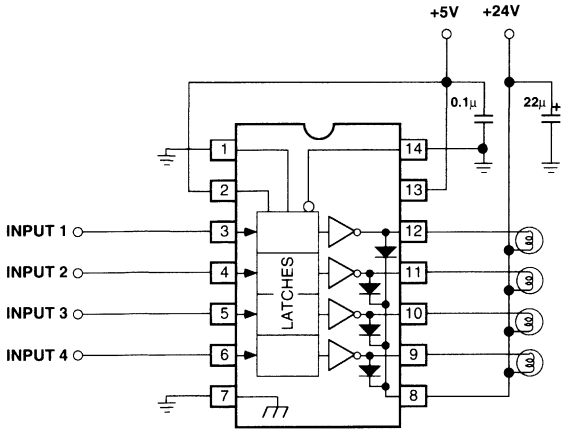


UNIPOLAR 2-PHASE DRIVE

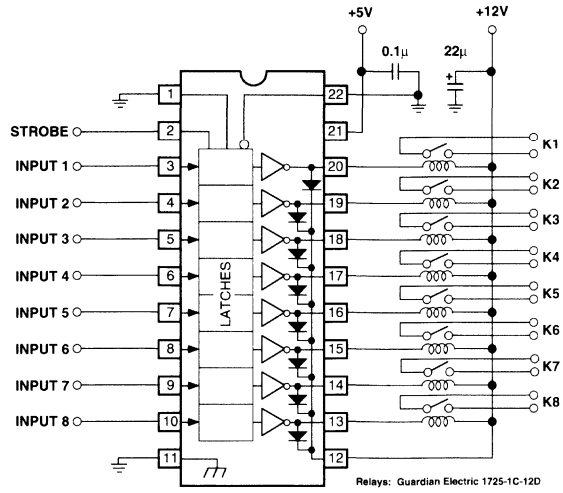


Typical Applications, Continued

MIC5800 Incandescent/Halogen Lamp Driver



MIC5801 Relay Driver



MIC58P01

8-Bit Parallel Input Protected Latched Driver

General Description

The MIC58P01 parallel-input latched driver is a high-voltage (80V), high-current (500mA) integrated circuit comprised of eight CMOS data latches, a bipolar Darlington transistor driver for each latch, and CMOS control circuitry for the common CLEAR, STROBE, and OUTPUT ENABLE functions. Similar to the MIC5801, additional protection circuitry supplied on this device includes thermal shutdown, under voltage lockout (UVLO), and over-current shutdown.

The bipolar/CMOS combination provides an extremely low-power latch with maximum interface flexibility. The MIC58P01 has open-collector outputs capable of sinking 500 mA and integral diodes for inductive load transient suppression with a minimum output breakdown voltage rating of 80V (50V sustaining). The drivers may be paralleled for higher load current capability.

With a 5V logic supply, the MIC58P01 will typically operate at better than 5MHz. With a 12V logic supply, significantly higher speeds are obtained. The CMOS inputs are compatible with standard CMOS, PMOS, and NMOS circuits. TTL circuits may require pull-up resistors.

Each of these eight outputs has an independent over-current shutdown of 500mA. Upon current shutdown, the affected channel will turn OFF until V_{DD} is cycled or the ENABLE/RESET pin is pulsed high. Current pulses less than 2µs will not activate current shutdown. Temperatures above 165°C will shut down all outputs. The UVLO circuit disables the outputs at low V_{DD}; hysteresis of 0.5V is provided.

Features

- 4.4MHz Minimum Data Input Rate
- High-Voltage, High-Current Outputs
- Per-Output Over-Current Shutdown (500mA typical)
- Under Voltage Lockout
- Thermal Shutdown
- Output Transient Protection Diodes
- CMOS, PMOS, NMOS, and TTL Compatible Inputs
- Internal Pull-Down Resistors
- Low-Power CMOS Latches

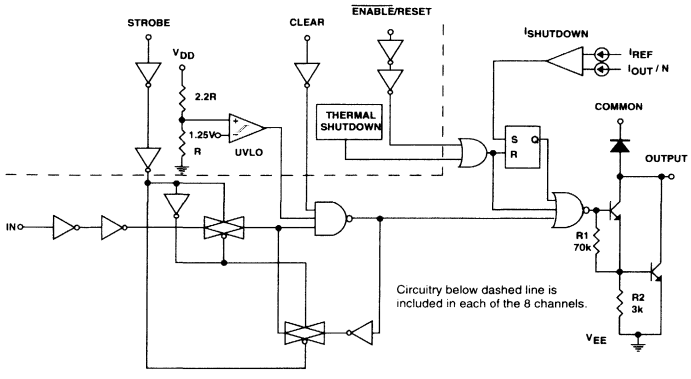
3

Ordering Information

Part Number	Temperature Range	Package
MIC58P01AJ	–55°C to +125°C	22-Pin Ceramic DIP
MIC58P01AJB*	–55°C to +125°C	22-Pin Ceramic DIP
MIC58P01BN	–40°C to +85°C	22-Pin Plastic DIP
MIC58P01BV	–40°C to +85°C	28-Pin PLCC
MIC58P01BWM	–40°C to +85°C	24-Pin Wide SOIC

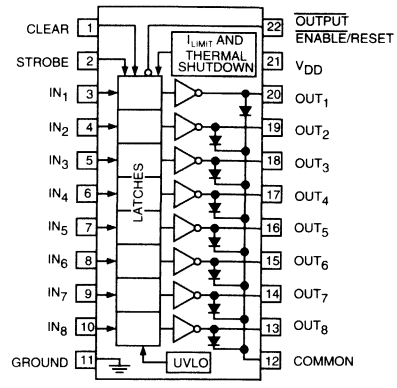
* AJB indicates units screened to MIL-STD 883, Method 5004, condition B, and burned-in for 1 week.

Functional Diagram

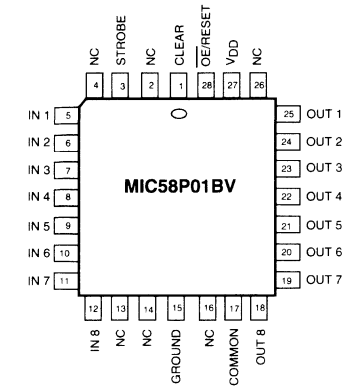


Pin Configuration

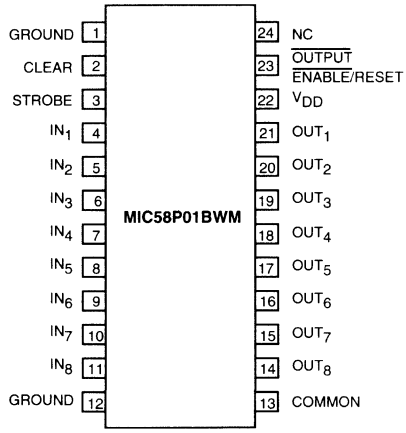
(Ceramic or Plastic DIP)



Pin Configuration, Continued



MIC58P01BV, 28–pin PLCC



MIC58P01BWM, 24–pin SOIC

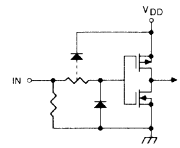
Absolute Maximum Ratings: (Note 1)

at +25°C Free-Air Temperature

Output Voltage, V_{CE}	80V
Supply Voltage, V_{DD}	15V
Input Voltage Range, V_{IN}	–0.3V to V_{DD} + 0.3V
Package Power Dissipation:	
MIC58P01BN	2.25W
Derate above T_A = +25°C	22.5mW/°C
MIC58P01AJ/AJB	2.0W
Derate above T_A = +25°C	20mW/°C
MIC58P01BV	1.6W
Derate above T_A = +25°C	16mW/°C
MIC58P01BWM	1.4W
Derate above T_A = +25°C	14mW/°C
Operating Temperature Range, T_A	–55°C to +125°C
Storage Temperature Range, T_S	–65°C to +125°C

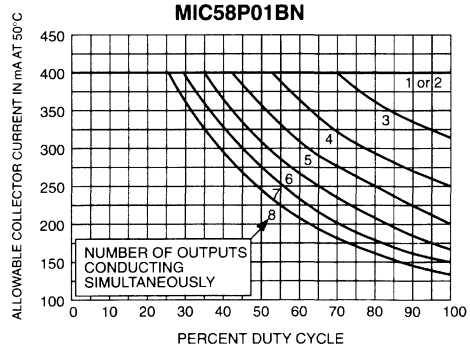
Note 1: Micrel CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.

Typical Input



Allowable Output Current As A Function of Duty Cycle

MIC58P01BN



Pin Description

Pin (DIP)	Name	Description
1	CLEAR	Resets all Latches and turns all outputs OFF (open).
2	STROBE	Input Strobe Pin. Loads output latches when High.
3–10	INPUT	Parallel Inputs, 1 through 8
11	GROUND	Logic and Output Ground pin.
12	COMMON	Transient suppression diode common cathode pin.
13–20	OUTPUT	Parallel Outputs, 8 through 1.
21	V_{DD}	Logic Supply voltage.
22	$\overline{\text{OUTPUT}}$ $\overline{\text{ENABLE}}$/RESET	When Low, Outputs are active. When High, outputs are inactive and the device is reset from a fault condition. An undervoltage condition emulates a high $\overline{\text{OE}}$ input.

Electrical Characteristics: at T_A = +25°C, V_{DD} = 5V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Output Leakage Current	I_{CEX}	V_{CE} = 80V, T_A = +25°C			50	µA
		V_{CE} = 80V, T_A = +70°C			100	
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 100mA		0.9	1.1	V
		I_C = 200mA		1.1	1.3	
		I_C = 350mA		1.3	1.6	
Input Voltage	$V_{IN(0)}$				1.0	V
	$V_{IN(1)}$	V_{DD} = 12V	10.5			
		V_{DD} = 10V	8.5			
		V_{DD} = 5.0V (See Note)	3.5			
Input Resistance	R_{IN}	V_{DD} = 12V	50	200		kΩ
		V_{DD} = 10V	50	300		
		V_{DD} = 5.0V	50	600		
Supply Current	$I_{DD(ON)}$ (One output active)	V_{DD} = 12V, Outputs Open		3.3	4.5	mA
		V_{DD} = 10V, Outputs Open		3.1	4.5	
		V_{DD} = 5.0V, Outputs Open		2.4	3.6	
	$I_{DD(ON)}$ (All outputs active)	V_{DD} = 12V, Outputs Open		6.4	10.0	mA
		V_{DD} = 10V, Outputs Open		6.0	9.0	
		V_{DD} = 5.0V, Outputs Open		4.7	7.5	
	$I_{DD(OFF)}$ (Total)	V_{DD} = 12V, Outputs Open, Inputs = 0V		3.0	4.5	mA
		V_{DD} = 5.0V, Outputs Open, Inputs = 0V		2.2	3.6	
Clamp Diode Leakage Current	I_R	V_R = 80V, T_A = +25°C			50	µA
		V_R = 80V, T_A = +70°C			100	
Over-Current Threshold	I_{LIM}	Per Output		500		mA
Start-Up Voltage	V_{SU}	Note 2.	3.5	4.0	4.5	V
Minimum Operating V_{DD}	$V_{DD\ MIN}$		3.0	3.5	4.0	V
Clamp Diode Forward Voltage	V_F	I_F = 350mA		1.7	2.0	V
Thermal Shutdown				165		°C
Thermal Shutdown Hystersis				10		°C

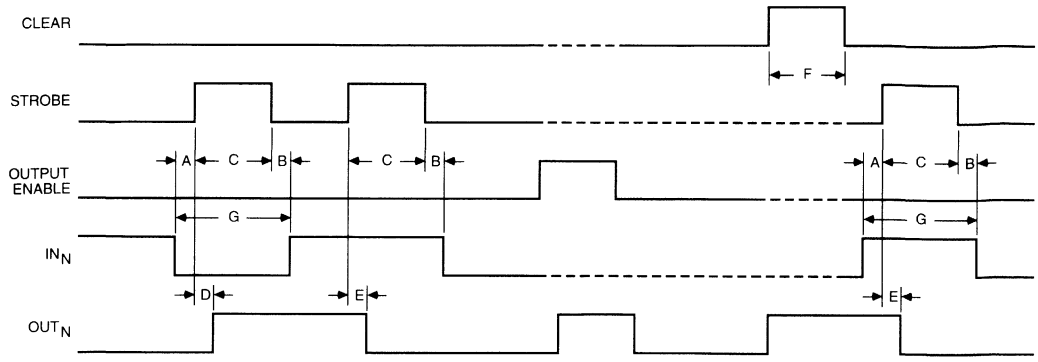
NOTE 1: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to insure a minimum logic "1".
NOTE 2: Under-Voltage Lockout is guaranteed to release device at no more than 4.5V, and disable the device at no less than 3.0V.

Truth Table

IN_N	Strobe	Clear	$\overline{\text{Output}}$ Enable	OUT_N	
				t–1	t
0	1	0	0	X	OFF
1	1	0	0	X	ON
X	X	1	X	X	OFF
X	X	X	1	X	OFF
X	0	0	0	ON	ON
X	0	0	0	OFF	OFF

X = Irrelevant
t–1 = previous output state
t = present output state

Information present at an input is transferred to its latch when the STROBE is high. A high CLEAR input will set all latches to the output OFF condition regardless of the Data or STROBE input levels. A high OUTPUT ENABLE will set all outputs to the OFF condition, regardless of any other input conditions. When the OUTPUT ENABLE is low, the outputs depend on the state of their respective latches. If current shutdown is activated, the OUTPUT ENABLE must be pulsed high to restore operation. Over temperature faults are not latched and require no reset pulse.



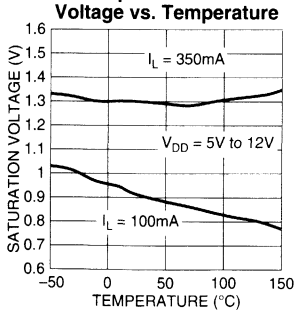
Timing Conditions

(T_A = +25°C, Logic Levels are V_{DD} and Ground, V_{DD} = 5V)

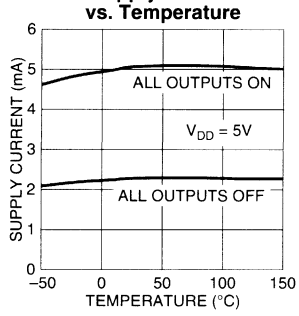
A. Minimum data active time before strobe enabled (data set-up time) ..... 50 ns
B. Minimum data active time after strobe disabled (data hold time) ..... 50 ns
C. Minimum strobe pulse width ..... 125 ns
D. Typical time between strobe activation and output on to off transition ..... 500 ns
E. Typical time between strobe activation and output off to on transition ..... 500 ns
F. Minimum clear pulse width ..... 300 ns
G. Minimum data pulse width ..... 225 ns

Typical Characteristic Curves

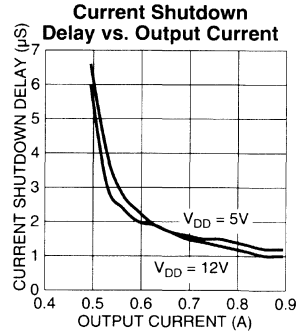
Output Saturation Voltage vs. Temperature



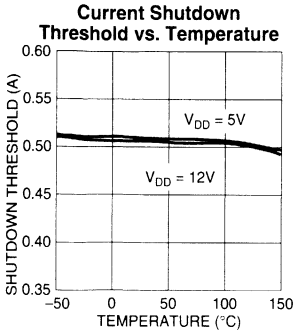
Supply Current vs. Temperature



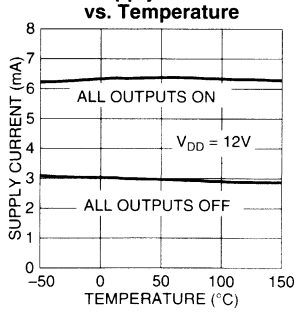
Current Shutdown Delay vs. Output Current



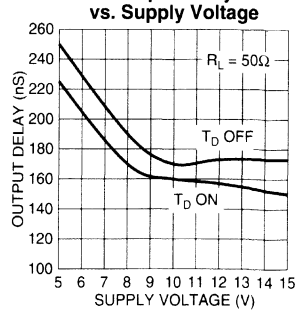
Current Shutdown Threshold vs. Temperature



Supply Current vs. Temperature

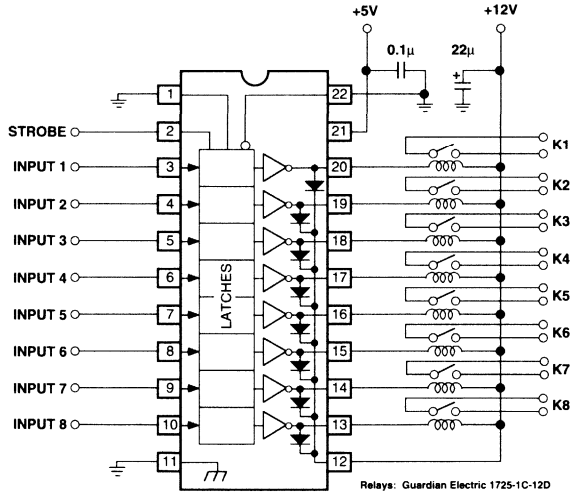


Output Delay vs. Supply Voltage



Typical Application

MIC58P01 Protected Relay Driver



3

MIC5821/5822 Family

8-Bit Serial-Input Latched Drivers

General Description

BiCMOS technology gives the MIC5821/5822 family flexibility beyond the reach of standard logic buffers and power driver arrays. These devices each have an eight-bit CMOS shift register, CMOS control circuitry, eight CMOS data latches, and eight bipolar current-sink Darlington output drivers. The 500mA outputs are suitable for use with incandescent bulbs and other moderate to high current loads. The drivers can be operated with a split supply where the negative supply is down to –20V. Except for maximum driver output voltage ratings, the MIC5821 and MIC5822 are identical.

These devices have greatly improved data-input rates. With a 5V logic supply they will typically operate faster than 5 MHz. With a 12V supply significantly higher speeds are obtained. The CMOS inputs are compatible with standard CMOS, PMOS, and NMOS logic levels. TTL and DTL circuits may require the use of appropriate pull-up resistors. By using the serial data output, the drivers can be cascaded for interface applications requiring additional drive lines.

Features

- 3.3 MHz Minimum Data-Input Rate
- CMOS, PMOS, NMOS, TTL Compatible
- Internal Pull-Down or Pull-Up Resistors
- Low-Power CMOS Logic and Latches
- High-Voltage Current-Sink Outputs
- Single or Split Supply Operation

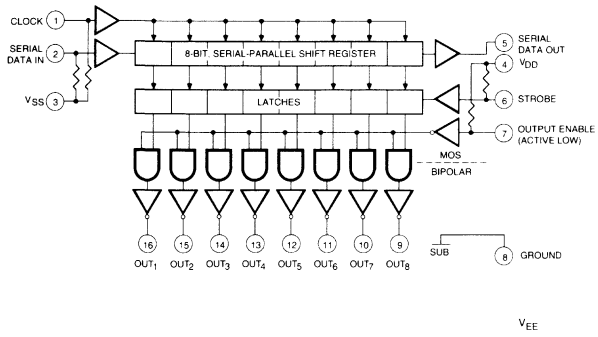
Ordering Information

Part Number	Temperature Range	Package
MIC5821CN*	0°C to +70°C	16-Pin Plastic DIP
MIC5821BN	–40°C to +85°C	16-Pin Plastic DIP
MIC5822BN	–40°C to +85°C	16-Pin Plastic DIP
MIC5822AJ	–55°C to +125°C	16-Pin Ceramic DIP
MIC5822AJB†	–55°C to +125°C	16-Pin Ceramic DIP

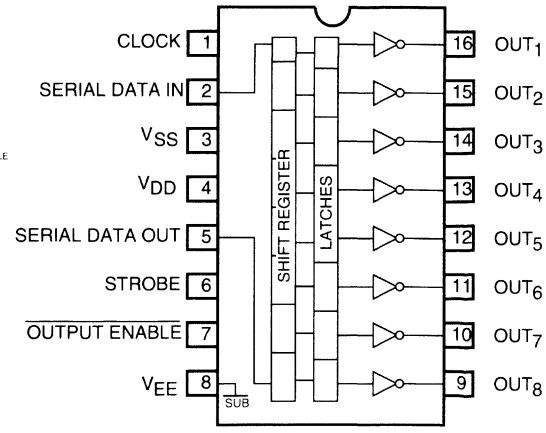
* Micrel reserves the right to substitute MIC5821BN grade devices for the MIC5821CN

† AJB indicates units screened to MIL-STD 883, Method 5004, condition B, and burned-in for 1-week.

Functional Diagram

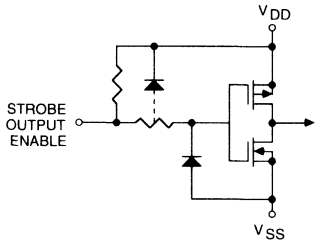


Pin Configuration



(Plastic and Ceramic DIP)

Typical Input Circuits



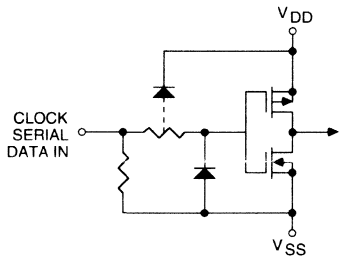
Absolute Maximum Ratings (Note 1)

at 25°C Free-Air Temperature and V_{SS} = 0V

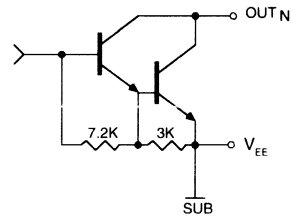
Output Voltage, V_{CE}	(MIC5821)	50V
	(MIC5822)	80V
Output Voltage, $V_{CE\ SUS}$	(MIC5821)(Note 3)	35V
	(MIC5822)(Note 3)	50V
Logic Supply Voltage, V_{DD}		15V
Input Voltage Range, V_{IN}		−0.3V to V_{DD} + 0.3V
$V_{DD} - V_{EE}$		25V
Emitter Supply Voltage, V_{EE}		−20V
Continuous Output Current, I_{OUT}		500mA
Package Power Dissipation, $P_{D(\text{Note 1})}$		1.67W
Operating Temperature Range, T_A		−55°C to +125°C
Storage Temperature Range, T_S		−65°C to +150°C

Note 1: Derate at the rate of 16.7mW/°C above T_A = 25°C (Plastic DIP).
Note 2: CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.
Note 3: For inductive load applications.

3



Typical Output Driver



Maximum Allowable Duty Cycle (Plastic DIP)

Number of Outputs ON (I_{OUT} = 200mA V_{DD} = 12V)	Maximum Allowable Duty Cycle at Ambient Temperature of				
	25°C	40°C	50°C	60°C	70°C
8	73%	62%	55%	47%	40%
7	83%	71%	62%	54%	46%
6	97%	82%	72%	63%	53%
5	100%	98%	87%	75%	63%
4	100%	100%	100%	93%	79%
3	100%	100%	100%	100%	100%
2	100%	100%	100%	100%	100%
1	100%	100%	100%	100%	100%

Electrical Characteristics at T_A = 25°C V_{DD} = 5V, V_{EE} = V_{SS} = 0V (unless otherwise specified)

Characteristic	Symbol	Applicable Devices	Test Conditions	Limits Min.	Limits Max.	Unit
Output Leakage Current	I_{CEX}	MIC5821	V_{OUT} = 50V		50	µA
			V_{OUT} = 50V, T_A = +70°C		100	
		MIC5822	V_{OUT} = 80V		50	
			V_{OUT} = 80V, T_A = +70°C		100	
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	Both	I_{OUT} = 100mA		1.1	V
			I_{OUT} = 200mA		1.3	
			I_{OUT} = 350mA, V_{DD} = 7.0V		1.6	
Input Voltage	$V_{IN(0)}$	Both			0.8	V
	$V_{IN(1)}$	Both	V_{DD} = 12V	10.5		
			V_{DD} = 10V	8.5		
			V_{DD} = 5.0V	3.5		
Input Resistance	R_{IN}	Both	V_{DD} = 12V	50		kΩ
			V_{DD} = 10V	50		
			V_{DD} = 5.0V	50		
Supply Current	$I_{DD(ON)}$	Both	One Driver ON, V_{DD} = 12V		4.5	mA
			One Driver ON, V_{DD} = 10V		3.9	
			One Driver ON, V_{DD} = 5.0V		2.4	
			All Drivers ON, V_{DD} = 12V		16	
			All Drivers ON, V_{DD} = 10V		14	
			All Drivers ON, V_{DD} = 5.0V		8	
	$I_{DD(OFF)}$	Both	All Drivers OFF, V_{DD} = 5.0V, All Inputs = 0V		1.6	
			All Drivers OFF, V_{DD} = 12V, All Inputs= 0V		2.9	

Electrical Characteristics MIC5822AJ/AJB at T_A = –55°C, V_{DD} = 5V, V_{SS} = V_{EE} = 0V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits Min.	Limits Max.	Unit
Output Leakage Current	I_{CEX}	V_{OUT} = 80V		50	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_{OUT} = 100mA		1.3	V
		I_{OUT} = 200mA		1.5	
		I_{OUT} = 350mA, V_{DD} = 7.0V		1.8	
Input Voltage	$V_{IN0)}$			0.8	V
	$V_{IN(1)}$	V_{DD} = 12V	10.5		
		V_{DD} = 5.0V	3.5		
Input Resistance	RIN	V_{DD} = 12V	35		kΩ
		V_{DD} = 10V	35		
		V_{DD} = 5.0V	35		
Supply Current	$I_{DD(ON)}$	One Driver ON, V_{DD} = 12V		5.5	mA
		One Driver ON, V_{DD} = 10V		4.5	
		One Driver ON, V_{DD} = 5.0V		3.0	
		All Drivers ON, V_{DD} = 12V		16	
		All Drivers ON, V_{DD} = 10V		14	
		All Drivers ON, V_{DD} = 5.0V		10	
	$I_{DD(OFF)}$	All Drivers OFF, V_{DD} = 12V		3.5	
		All Drivers OFF, V_{DD} = 5.0V		2.0	

Electrical Characteristics MIC5822AJ/AJB at T_A = +125°C, V_{DD} = 5V, V_{SS} = V_{EE} = 0V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Unit
Output Leakage Current	I_{CEX}	V_{OUT} = 80V		500	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_{OUT} = 100mA		1.3	V
		I_{OUT} = 200mA		1.5	
		I_{OUT} = 350mA, V_{DD} = 7.0V		1.8	
Input Voltage	$V_{IN(0)}$			0.8	V
	$V_{IN(1)}$	V_{DD} = 12V	10.5		
		V_{DD} = 5.0V	3.5		
Input Resistance	R_{IN}	V_{DD} = 12V	50		kΩ
		V_{DD} = 10V	50		
		V_{DD} = 5.0V	50		
Supply Current	$I_{DD(ON)}$	One Driver ON, V_{DD} = 12V		4.5	mA
		One Driver ON, V_{DD} = 10V		3.9	
		One Driver ON, V_{DD} = 5.0V		2.4	
		All Drivers ON, V_{DD} = 12V		16	
		All Drivers ON, V_{DD} = 10V		14	
		All Drivers ON, V_{DD} = 5.0V		8	
	$I_{DD(OFF)}$	All Drivers OFF, V_{DD} = 12V		2.9	
		All Drivers OFF, V_{DD} = 5.0V		1.6	

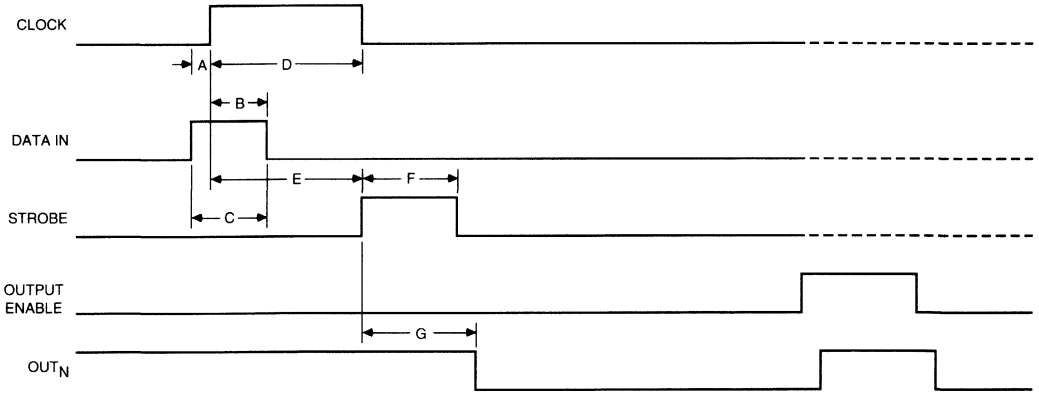
3

MIC5821/5822 Family Truth Table

Serial Data Input	Clock Input	Shift Register Contents I_1 I_2 I_3 ..... I_8	Serial Data Output	Strobe Input	Latch Contents I_1 I_2 I_3 ..... I_8	Output Enable	Output Contents I_1 I_2 I_3 ..... I_8
H	⎍	H R_1 R_2 ..... R_7	R_7				
L	⎍	L R_1 R_2 ..... R_7	R_7				
X	⎏	R_1 R_2 R_3 ..... R_8	R_8				
		X X X X	X	L	R_1 R_2 R_3 ..... R_8		
		P_1 P_2 P_3 ..... P_8	P_8	H	P_1 P_2 P_3 ..... P_8	L	P_1 P_2 P_3 ..... P_8
					X X X X	H	H H H ..... H

L = Low Logic Level H = High Logic Level X = Irrelevant P = Present State R = Previous State

Timing Diagram



Timing Conditions

(T_A = +25°C, Logic Levels are V_{DD} and V_{SS})

	V_{DD} = 5.0V
A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time)	75 ns
B. Minimum Data Active Time After Clock Pulse (Data Hold Time)	75 ns
C. Minimum Data Pulse Width	150 ns
D. Minimum Clock Pulse Width	150 ns
E. Minimum Time Between Clock Activation and Strobe	300 ns
F. Minimum Strobe Pulse Width	100 ns
G. Typical Time Between Strobe Activation and Output Transition	500 ns

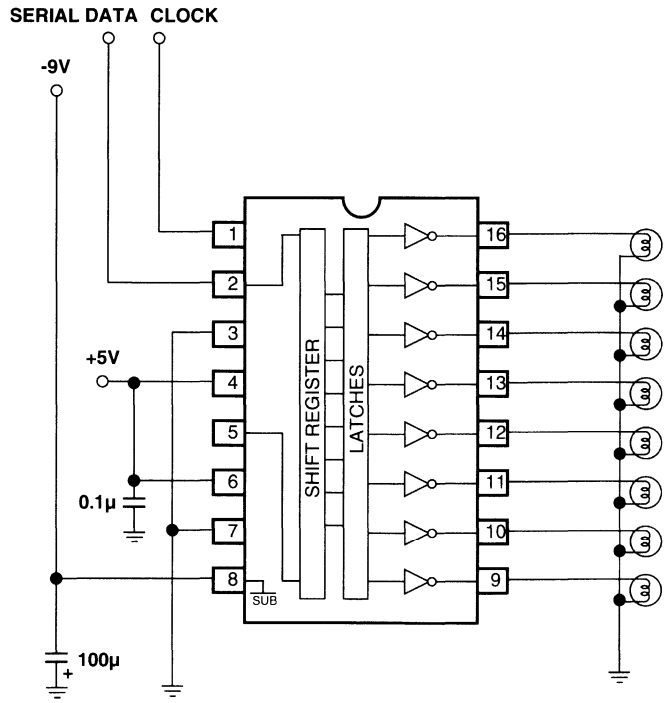
SERIAL DATA present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the ENABLE input be high during serial entry.

When the ENABLE input is high, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the ENABLE input low, the outputs are controlled by the state of the latches.

Typical Applications

MIC5822 Level Shifting Lamp Driver with Darlington Emitters Tied to a Negative Supply



MIC5841/5842 Family

8-Bit Serial-Input Latched Drivers

General Description

Using BiCMOS technology, the MIC5841/5842 integrated circuits were fabricated to be used in a wide variety of peripheral power driver applications. The devices each have an eight-bit CMOS shift register, CMOS control circuitry, eight CMOS data latches, and eight bipolar current-sink Darlington output drivers.

These two devices differ only in maximum voltage ratings. The MIC5842 offers premium performance with a minimum output breakdown voltage rating of 80V (50V sustaining). The drivers can be operated with a split supply where the negative supply is down to –20V.

The 500 mA outputs, with integral transient-suppression diodes, are suitable for use with lamps, relays, solenoids and other inductive loads.

These devices have improved speed characteristics. With a 5V logic supply, they will typically operate faster than 5 MHz. With a 12V supply, significantly higher speeds are obtained. The CMOS inputs are compatible with standard CMOS, PMOS, and NMOS logic levels. TTL or DTL circuits may require the use of appropriate pull-up resistors. By using the serial data output, the drivers can be cascaded for interface applications requiring additional drive lines.

The MIC5840 family is available in DIP, PLCC, and SOIC packages. Because of limitations on package power dissipation, the simultaneous operation of all drivers at maximum rated current might require a reduction in duty cycle. A copper-alloy lead frame provides for maximum package power dissipation.

Features

- 3.3 MHz Minimum Data-Input Rate
- CMOS, PMOS, NMOS, TTL Compatible
- Internal Pull-Up/Pull-Down Resistors
- Low-Power CMOS Logic and Latches
- High-Voltage Current-Sink Outputs
- Output Transient-Protection Diodes
- Single or Split Supply Operation

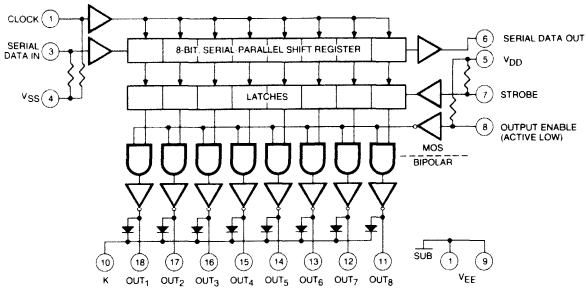
Ordering Information

Part Number	Temperature Range	Package
MIC5841BN	–40°C to +85°C	18-Pin Plastic DIP
MIC5841BV	–40°C to +85°C	20-Pin PLCC
MIC5841BWM	–40°C to +85°C	18-Pin Wide SOIC
MIC5841AJ	–55°C to +125°C	18-Pin Ceramic DIP
MIC5841AJB*	–55°C to +125°C	18-Pin Ceramic DIP
MIC5842BN	–40°C to +85°C	18-Pin Plastic DIP
MIC5842BV	–40°C to +85°C	20-Pin PLCC
MIC5842BWM	–40°C to +85°C	18-Pin Wide SOIC
MIC5842AJ	–55°C to +125°C	18-Pin Ceramic DIP
MIC5842AJB*	–55°C to +125°C	18-Pin Ceramic DIP

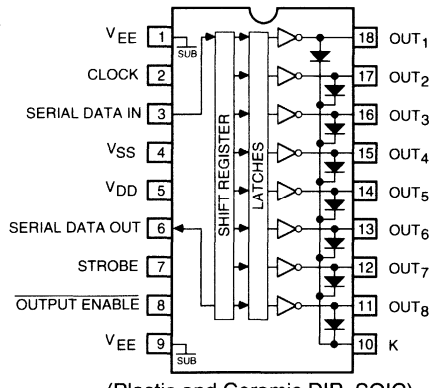
* AJB indicates units screened to MIL-STD 883, Method 5004, condition B, and burned-in for 1-week.

3

Functional Diagram



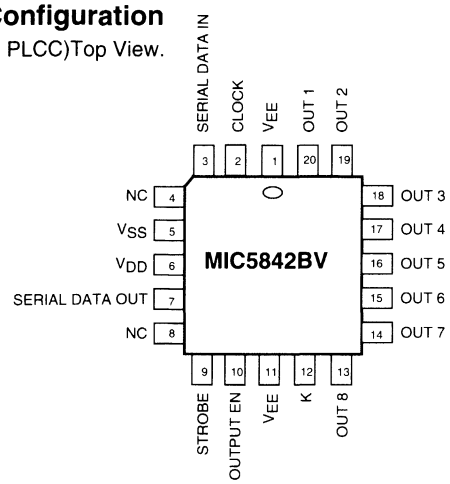
Pin Configuration



(Plastic and Ceramic DIP, SOIC)

Pin Configuration

(20-Pin PLCC)Top View.



Absolute Maximum Ratings (Note 1, 2, 3)

at 25°C Free-Air Temperature and V_{SS} = 0V

Output Voltage, V_{CE} (MIC5841)	50V
(MIC5842)	80V
Output Voltage, $V_{CE(SUS)}$ (MIC5841) (Note 1)	35V
(MIC5842)	50V
Logic Supply Voltage, V_{DD}	15V
V_{DD} with Reference to V_{EE}	25V
Emitter Supply Voltage, V_{EE}	–20V
Input Voltage Range, V_{IN}	–0.3V to V_{DD} + 0.3V
Continuous Output Current, I_{OUT}	500mA
Package Power Dissipation, P_D (Note 2)	1.82W
Operating Temperature Range, T_A	–55°C to +125°C
Storage Temperature Range, T_S	–65°C to +150°C

Note 1: For Inductive load applications.
Note 2: Derate at the rate of 18.2mW/°C above T_A = 25°C (Plastic DIP)
Note 3: CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.

Electrical Characteristics at T_A = 25°C V_{DD} = 5V, V_{SS} = V_{EE} = 0V (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions	Limits Min.	Limits Max.	Limits Unit
Output Leakage Current	I_{CEX}	MIC5841	V_{OUT} = 50V		50	µA
			V_{OUT} = 50V, T_A = +70°C		100	
		MIC5842	V_{OUT} = 80V		50	
			V_{OUT} = 80V, T_A = +70°C		100	
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	Both	I_{OUT} = 100mA		1.1	V
			I_{OUT} = 200mA		1.3	
			I_{OUT} = 350mA, V_{DD} = 7.0V		1.6	
Collector-Emitter Sustaining Voltage	$V_{CE(SUS)}$ (Note 5)	MIC5841	I_{OUT} = 350mA, L = 2mH	35		V
		MIC5842	I_{OUT} = 350mA, L = 2mH	50		
Input Voltage	$V_{IN(0)}$	Both			0.8	V
	$V_{IN(1)}$	Both	V_{DD} = 12V	10.5		
			V_{DD} = 10V	8.5		
			V_{DD} = 5.0V (See Note 4)	3.5		
Input Resistance	R_{IN}	Both	V_{DD} = 12V	50		kΩ
			V_{DD} = 10V	50		
			V_{DD} = 5.0V	50		
Supply Current	$I_{DD(ON)}$	Both	All Drivers ON, V_{DD} = 12V		16	mA
			All Drivers ON, V_{DD} = 10V		14	
			All Drivers ON, V_{DD} = 5.0V		8.0	
	$I_{DD(OFF)}$	Both	All Drivers OFF, V_{DD} = 12V		2.9	
			All Drivers OFF, V_{DD} = 10V		2.5	
			All Drivers OFF, V_{DD} = 5.0V		1.6	
Clamp Diode Leakage Current	I_R	MIC5841	V_R = 50V		50	µA
		MIC5842	V_R = 80V		50	
Clamp Diode Forward Voltage	V_F	Both	I_F = 350mA		2.0	V

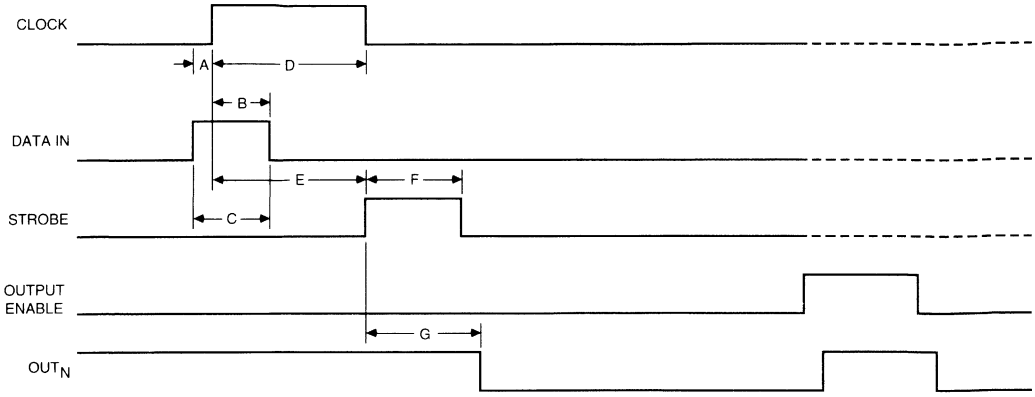
Note 4: Operation of these devices with standard TTL may require the use of appropriate pull-up resistors to insure an input logic HIGH.
Note 5: Not 100% tested. Guaranteed by design.

Electrical Characteristics MIC5841AJ/AJB and MIC5842AJ/AJB at T_A = –55°C, V_{DD} = 5V, V_{SS} = V_{EE} = 0V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Unit
Output Leakage Current	I_{CEX}	V_{OUT} = 80V		50	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_{OUT} = 100mA		1.3	V
		I_{OUT} = 200mA		1.5	
		I_{OUT} = 350mA, V_{DD} = 7.0V		1.8	
Input Voltage	$V_{IN(0)}$			0.8	V
	$V_{IN(1)}$	V_{DD} = 12V	10.5		
		V_{DD} = 5.0V	3.5		
Input Resistance	R_{IN}	V_{DD} = 12V	35		kΩ
		V_{DD} = 10V	35		
		V_{DD} = 5.0V	35		
Supply Current	$I_{DD(ON)}$	All Drivers ON, V_{DD} = 12V		16	mA
		All Drivers ON, V_{DD} = 10V		14	
		All Drivers ON, V_{DD} = 5.0V		10	
	$I_{DD(OFF)}$	All Drivers OFF, V_{DD} = 12V		3.5	
		All Drivers OFF, V_{DD} = 5.0V		2.0	

Electrical Characteristics MIC5841AJ/AJB and MIC5842AJ/AJB at T_A = +125°C, V_{DD} = 5V, V_{SS} = V_{EE} = 0V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Unit
Output Leakage Current	I_{CEX}	V_{OUT} = 80V		500	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_{OUT} = 100mA		1.3	V
		I_{OUT} = 200mA		1.5	
		I_{OUT} = 350mA, V_{DD} = 7.0V		1.8	
Input Voltage	$V_{IN(0)}$			0.8	V
	$V_{IN(1)}$	V_{DD} = 12V	10.5		
		V_{DD} = 5.0V	3.5		
Input Resistance	R_{IN}	V_{DD} = 12V	50		kΩ
		V_{DD} = 10V	50		
		V_{DD} = 5.0V	50		
Supply Current	$I_{DD(ON)}$	All Drivers ON, V_{DD} = 12V		16	mA
		All Drivers ON, V_{DD} = 10V		14	
		All Drivers ON, V_{DD} = 5.0V		8	
	$I_{DD(OFF)}$	All Drivers OFF, V_{DD} = 12V		2.9	
		All Drivers OFF, V_{DD} = 5.0V		1.6	
Clamp Diode Leakage Current	I_R	MIC5841A V_R = 50V		100	µA
		MIC5842A V_R = 80V		100	



Timing Conditions

(T_A = 25°C Logic Levels are V_{DD} and V_{SS}) V_{DD} = 5V

A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time) ..... 75 ns
B. Minimum Data Active Time After Clock Pulse (Data Hold Time) ..... 75 ns
C. Minimum Data Pulse Width ..... 150 ns
D. Minimum Clock Pulse Width ..... 150 ns
E. Minimum Time Between Clock Activation and Strobe ..... 300 ns
F. Minimum Strobe Pulse Width ..... 100 ns
G. Typical Time Between Strobe Activation and Output Transition ..... 500 ns

SERIAL DATA present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the ENABLE input be high during serial data entry.

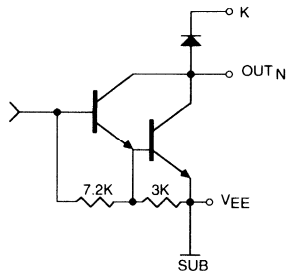
When the ENABLE input is high, all of the output buffers are disabled (OFF) without affecting information stored in the latches or shift register. With the ENABLE input low, the outputs are controlled by the state of the latches.

MIC5840 Family Truth Table

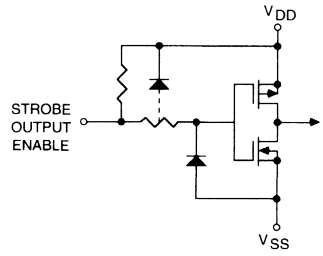
Serial Data Input	Clock Input	Shift Register Contents					Serial Data Output	Strobe Input	Latch Contents					Output Enable	Output Contents				
		I_1	I_2	I_3	.....	I_8			I_1	I_2	I_3	.....	I_8		I_1	I_2	I_3	.....	I_8
H	⎍	H	R_1	R_2	.....	R_7	R_7												
L	⎍	L	R_1	R_2	.....	R_7	R_7												
X	⎎	R_1	R_2	R_3	.....	R_8	R_8												
		X	X	X	.....	X	X	L	R_1	R_2	R_3	.....	R_8						
		P_1	P_2	P_3	.....	P_8	P_8	H	P_1	P_2	P_3	.....	P_8	L	P_1	P_2	P_3	.....	P_8
									X	X	X	.....	X	H	H	H	H	.....	H

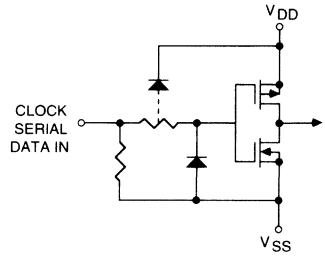
L = Low Logic Level
H = High Logic Level
X = Irrelevant
P = Present State
R = Previous State

Typical Output Driver



Typical Input Circuits





3

Maximum Allowable Duty Cycle (Plastic DIP)

V_{DD} = 5.0V

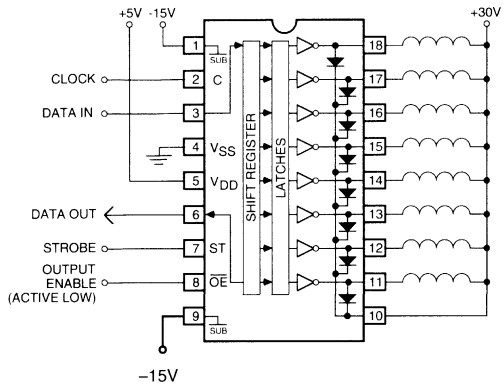
Number of Outputs ON (I_{OUT} = 200mA V_{DD} = 5.0V)	Max. Allowable Duty Cycle at Ambient Temperature of				
	25°C	40°C	50°C	60°C	70°C
8	85%	72%	64%	55%	46%
7	97%	82%	73%	63%	53%
6	100%	96%	85%	73%	62%
5	100%	100%	100%	88%	75%
4	100%	100%	100%	100%	93%
3	100%	100%	100%	100%	100%
2	100%	100%	100%	100%	100%
1	100%	100%	100%	100%	100%

V_{DD} = 12V

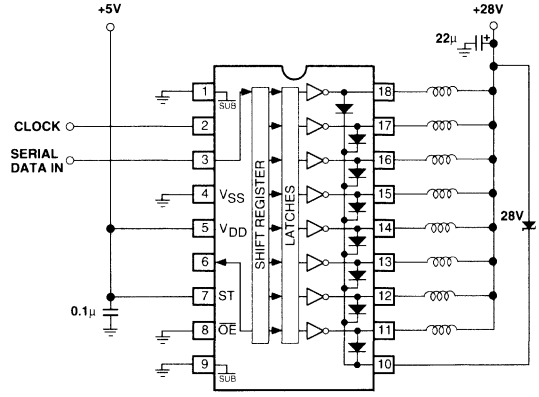
Number of Outputs ON (I_{OUT} = 200mA V_{DD} = 12V)	Max. Allowable Duty Cycle at Ambient Temperature of				
	25°C	40°C	50°C	60°C	70°C
8	80%	68%	60%	52%	44%
7	91%	77%	68%	59%	50%
6	100%	90%	79%	69%	58%
5	100%	100%	95%	82%	69%
4	100%	100%	100%	100%	86%
3	100%	100%	100%	100%	100%
2	100%	100%	100%	100%	100%
1	100%	100%	100%	100%	100%

Typical Applications

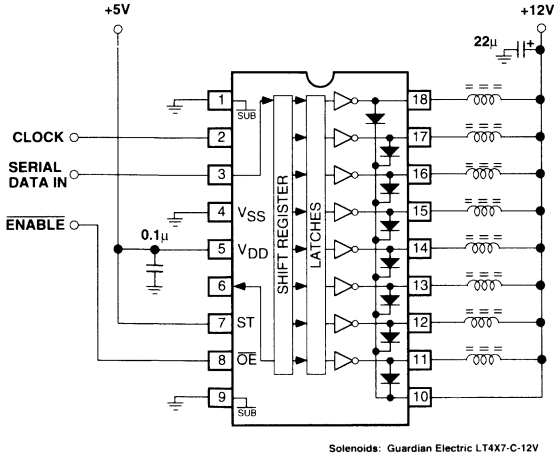
Relay/Solenoid Driver MIC5842



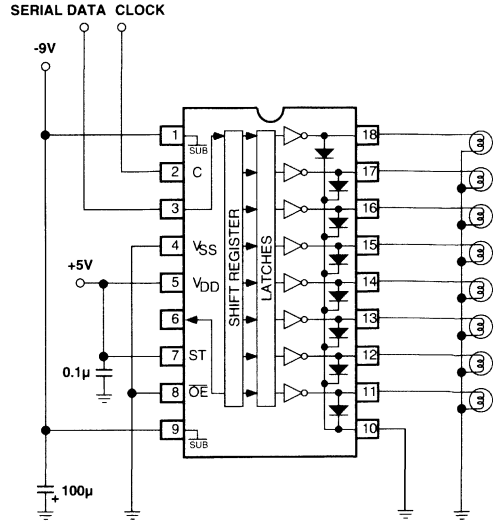
MIC5841 Hammer Driver



MIC5841 Solenoid Driver with Output Enable

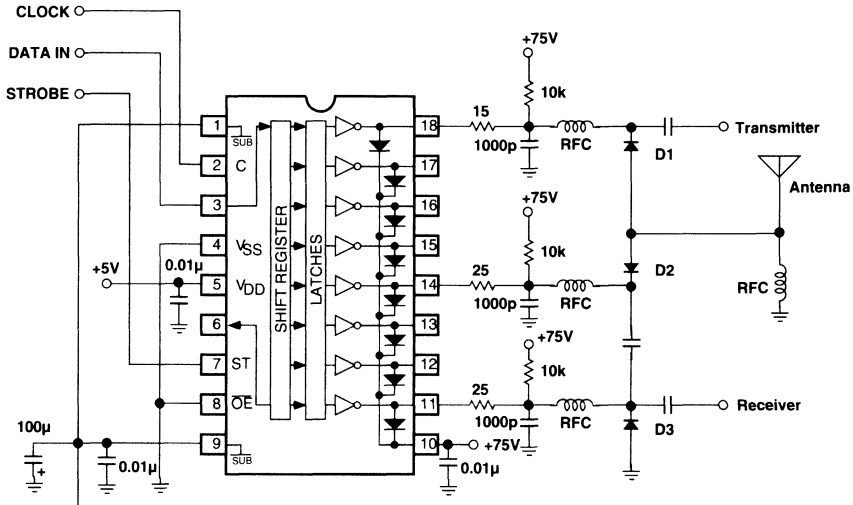


MIC5841 Level Shifting Lamp Driver with Darlington Emitters Tied to a Negative Supply



Typical Applications, Continued

MIC5842 Negative/Positive Supply PIN Diode Driver Transmit/Receive Switch



	Diode D1 (Latch 1)	D2 (Latch 5)	D3 (Latch 8)
Receive	OFF	ACTIVE	OFF
Transmit	ACTIVE	OFF	ACTIVE

PIN Diodes: UM9651

3

MIC58P42

8-Bit Serial-Input Protected Latched Driver

Preliminary Information

General Description

The MIC58P42 serial-input latched driver is a high-voltage (80V), high-current (500mA) integrated circuit comprised of eight CMOS data latches, a bipolar Darlington transistor driver for each latch, and CMOS control circuitry for the common STROBE, CLOCK, SERIAL DATA INPUT, and OUTPUT ENABLE functions. Similar to the MIC5842, additional protection circuitry supplied on this device includes thermal shutdown, under voltage lockout (UVLO), and over-current shutdown.

The bipolar/CMOS combination provides an extremely low-power latch with maximum interface flexibility. The MIC58P42 has open-collector outputs capable of sinking 500 mA and integral diodes for inductive load transient suppression with a minimum output breakdown voltage rating of 80V (50V sustaining). The drivers can be operated with a split supply, where the negative supply is down to –20V and may be paralleled for higher load current capability.

With a 5V logic supply, the MIC58P42 will typically operate at better than 5MHz. With a 12V logic supply, significantly higher speeds are obtained. The CMOS inputs are compatible with standard CMOS, PMOS, and NMOS circuits. TTL circuits may require pull-up resistors. By using the serial data output, drivers may be cascaded for interface applications requiring additional drive lines.

Each of these eight outputs has an independent over current shutdown of 500 mA. Upon over-current detection, the affected channel will turn OFF until V_{DD} is cycled or the ENABLE/RESET pin is pulsed high. Current pulses less than 2µs will not activate current shutdown. Temperatures above 165°C will shut down the device. The UVLO circuit prevents operation at low V_{DD}; hysteresis of 0.5V is provided. See the MIC59P60 for a similar device that additionally provides an error flag output.

Features

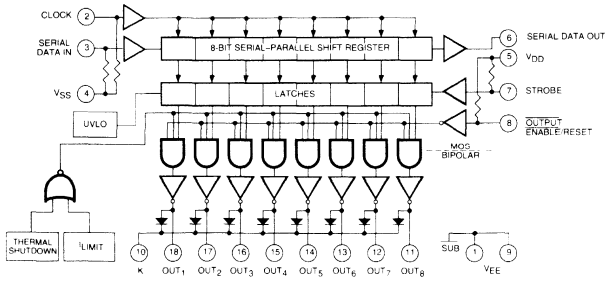
- 3.3 MHz Minimum Data-Input Rate
- CMOS, PMOS, NMOS, and TTL Compatible
- Internal Pull-Up/Pull-Down Resistors
- Low Power CMOS Logic and Latches
- High Voltage (80V) Current-Sink Outputs
- Output Transient-Protection Diodes
- Single or Split Supply Operation
- Thermal Shutdown
- Under-Voltage Lockout
- Per-Output Over-Current Shutdown (500mA typical)

Ordering Information

Part Number	Temperature Range	Package
MIC58P42AJ	–55°C to +125°C	18-Pin Ceramic DIP
MIC58P42AJB†	–55°C to +125°C	18-Pin Ceramic DIP
MIC58P42BN	–40°C to +85°C	18-Pin Plastic DIP
MIC58P42BV	–40°C to +85°C	20-Pin PLCC
MIC58P42BWM	–40°C to +85°C	18-Pin Wide SOIC

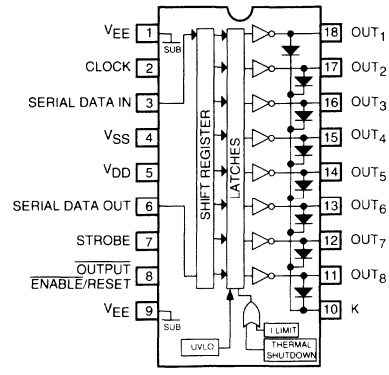
† AJB indicates units screened to MIL-STD 883, Method 5004, condition B, and burned-in for 1 week.

Functional Diagram

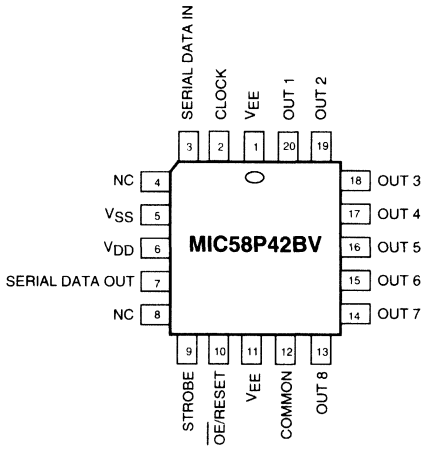


Pin Configuration

(Ceramic and Plastic DIP and SOIC)



PLCC Pin Configuration



Absolute Maximum Ratings (Note 1, 2)

at 25°C Free-Air Temperature and V_{SS} = 0V

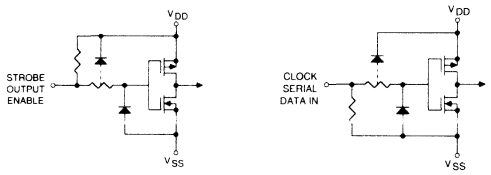
Output Voltage	80V
Output Voltage, $V_{CE(SUS)}$ (Note 1)	50V
Logic Supply Voltage Range, V_{DD}	4.5V to 15V
V_{DD} with Reference to V_{EE}	25V
Emitter Supply Voltage (Substrate), V_{EE}	–20V
Input Voltage Range, V_{IN}	–0.3V to V_{DD} + 0.3V
Package Power Dissipation, P_D	
MIC58P42BN	1.82W
Derate above T_A = +25°C	18mW/°C
MIC58P42AJ/AJB	1.6W
Derate above T_A = +25°C	16mW/°C
MIC58P42BV	1.4W
Derate above T_A = +25°C	14mW/°C
MIC58P42BWM	1.2W
Derate above T_A = +25°C	12mW/°C
Operating Temperature Range, T_A	–55°C to +125°C
Storage Temperature Range, T_S	–65°C to +150°C

Note 1: For Inductive load applications.

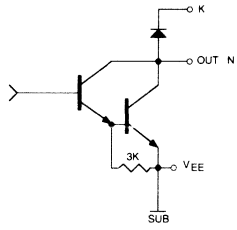
Note 2: CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.

3

Typical Input Circuits



Typical Output Driver



Pin Description

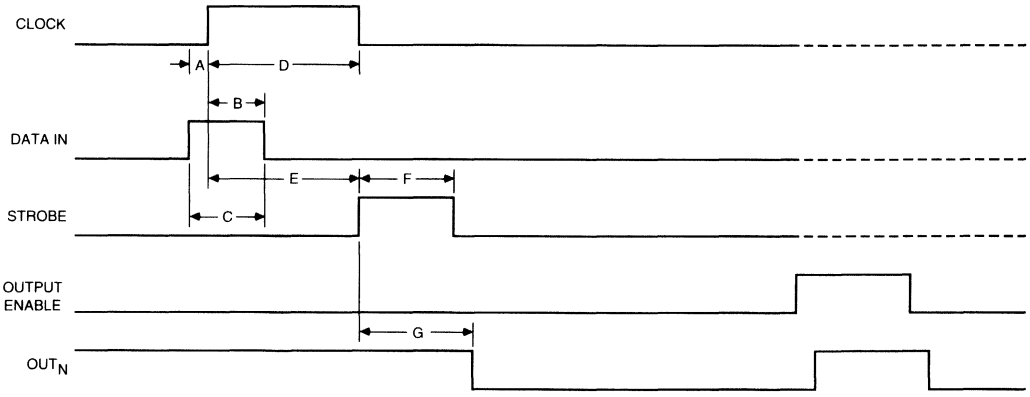
Pin (DIP & S.O.)	Name	Description
1,9	V_{EE}	Substrate. Most Negative voltage in the system connects here.
2	CLOCK	Serial Data Clock. A CLEAR input must also be clocked into the latches.
3	SERIAL DATA IN	Serial Data Input pin.
4	V_{SS}	Logic reference (Ground) pin.
5	V_{DD}	Logic Positive Supply voltage.
6	SERIAL DATA OUT	Serial Data Output pin. (Flow–through).
7	STROBE	Output Strobe pin. Loads output latches when high. Strobe is needed to clear latch.
8	$\overline{\text{OUTPUT}}$ $\overline{\text{ENABLE/RESET}}$	When Low, Outputs are active. When High, device is reset from a fault condition.
10	K	Transient suppression diode's cathode common pin.
11—18	OUTPUT N	Open Collector outputs 8 through 1.

Electrical Characteristics at T_A = +25°C, V_{DD} = 5V, V_{SS} = V_{EE} = 0V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Unit
Output Leakage Current	I_{CEX}	V_{OUT} = 80V			50	µA
		V_{OUT} = 80V, T_A = +70°C			100	
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_{OUT} = 100mA		0.9	1.1	V
		I_{OUT} = 200mA		1.1	1.3	
		I_{OUT} = 350mA		1.3	1.6	
Collector-Emitter Sustaining Voltage	$V_{CE(SUS)}$	I_{OUT} = 350mA, L = 2mH	50			V
Input Voltage	$V_{IN(0)}$				1.0	V
	$V_{IN(1)}$	V_{DD} = 12V	10.5			
		V_{DD} = 10V	8.5			
		V_{DD} = 5.0V	3.5			
Input Resistance	R_{IN}	V_{DD} = 12V	50	200		kΩ
		V_{DD} = 10V	50	300		
		V_{DD} = 5.0V	50	600		
Supply Current	$I_{DD(ON)}$	All Drivers ON, V_{DD} = 12V		6.4	10.0	mA
		All Drivers ON, V_{DD} = 10V		6.0	9.0	
		All Drivers ON, V_{DD} = 5.0V		4.6	7.5	
	$I_{DD\ (1\ ON)}$	One Driver ON, All others OFF, V_{DD} = 12V		3.1	4.5	
		One Driver ON, All others OFF, V_{DD} = 10V		2.9	4.5	
		One Driver ON, All others OFF, V_{DD} = 5V		2.3	3.6	
	$I_{DD(OFF)}$	All Drivers OFF, V_{DD} = 12V		2.6	4.2	
		All Drivers OFF, V_{DD} = 10V		2.4	3.6	
		All Drivers OFF, V_{DD} = 5.0V		1.9	3.0	
Clamp Diode Leakage Current	I_R	V_R = 80V			50	µA
Clamp Diode Forward Voltage	V_F	I_F = 350mA		1.7	2.0	V
Output Current Shutdown Threshold	I_{LIM}			500		mA
Start Up Voltage	V_{SU}	Note 1.	3.5	4.0	4.5	V
Minimum Supply (V_{DD})	$V_{DD\ MIN}$		3.0	3.5	4.0	V
Thermal Shutdown				165		°C
Thermal Shutdown Hysteresis				10		

Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to insure a minimum logic "1".

Note 1: Under-voltage lockout is guaranteed to release device at no more than 4.5V, and disable the device at no less than 3.0V



Timing Conditions

(T_A = +25°C, Logic Levels are V_{DD} and V_{SS}), V_{DD} = 5V

A. Typical Data Active Time Before Clock Pulse (Data Set-Up Time) ..... 75 ns
B. Minimum Data Active Time After Clock Pulse (Data Hold Time) ..... 75 ns
C. Minimum Data Pulse Width ..... 150 ns
D. Minimum Clock Pulse Width ..... 150 ns
E. Minimum Time Between Clock Activation and Strobe ..... 300 ns
F. Minimum Strobe Pulse Width ..... 100 ns
G. Typical Time Between Strobe Activation and Output Transition ..... 500 ns

SERIAL DATA present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the ENABLE input be high to prevent invalid output states.

When the ENABLE input is high, all of the output buffers are disabled (OFF) without affecting information stored in the latches or shift register. With the ENABLE input low, the outputs are controlled by the state of the latches. A positive OUTPUT ENABLE/ RESET pulse resets the output after a current shutdown fault. Thermal limit faults are not latched and require no reset pulse.

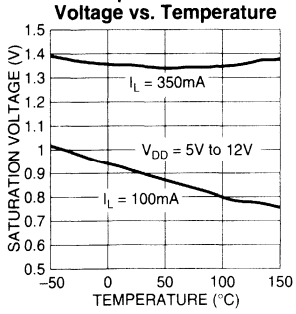
MIC58P42 Truth Table

Serial Data Input	Clock Input	Shift Register Contents I_1	I_2	I_3	I_8	Serial Data Output	Strobe Input	Latch Contents I_1	I_2	I_3	I_8	Output Enable	Output Contents I_1	I_2	I_3	I_8
H	⎍	H	R_1	R_2	R_7	R_7										
L	⎍	L	R_1	R_2	R_7	R_7										
X	⎎	R1	R2	R_3	R_8	R_8										
	⎍	O	O	O	O	L										
		X	X	X	X	X	L	R_1	R_2	R_3	R_8					
		P_1	P_2	P_3	P_8	P_8	H	P_1	P_2	P_3	P_8	L	P_1	P_2	P_3	P_8
								X	X	X	X	H	H	H	H	H

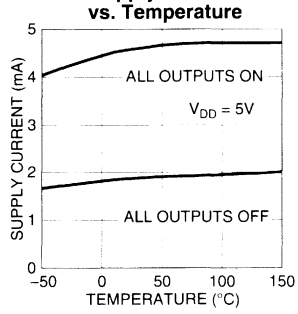
L = Low Logic Level
H = High Logic Level
X = Irrelevant
P = Present State
R = Previous State
O = Output OFF

Typical Characteristic Curves

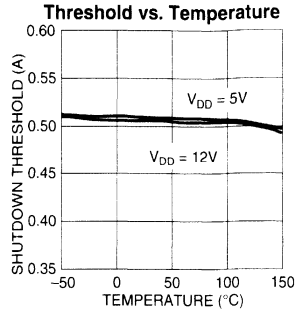
Output Saturation Voltage vs. Temperature



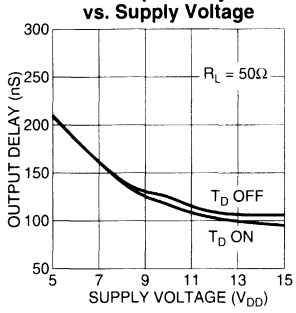
Supply Current vs. Temperature



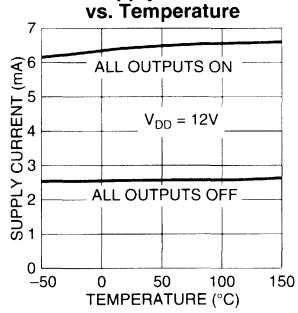
Current Shutdown Threshold vs. Temperature



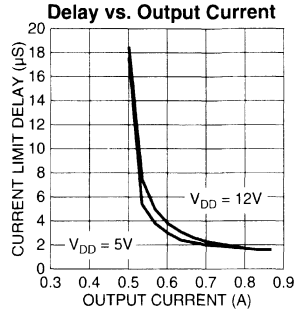
Output Delay vs. Supply Voltage



Supply Current vs. Temperature



Current Shutdown Delay vs. Output Current



Maximum Allowable Duty Cycle, Plastic DIP

V_{DD} = 5.0V

Number of Outputs ON (I_{OUT} = 200mA V_{DD} = 5.0V)	Max. Allowable Duty Cycle at Ambient Temperature of:				
	25°C	40°C	50°C	60°C	70°C
8	85%	72%	64%	55%	46%
7	97%	82%	73%	63%	53%
6	100%	96%	85%	73%	62%
5	100%	100%	100%	88%	75%
4	100%	100%	100%	100%	93%
3	100%	100%	100%	100%	100%
2	100%	100%	100%	100%	100%
1	100%	100%	100%	100%	100%

V_{DD} = 12V

Number of Outputs ON (I_{OUT} = 200mA V_{DD} = 12V)	Max. Allowable Duty Cycle at Ambient Temperature of:				
	25°C	40°C	50°C	60°C	70°C
8	80%	68%	60%	52%	44%
7	91%	77%	68%	59%	50%
6	100%	90%	79%	69%	58%
5	100%	100%	95%	82%	69%
4	100%	100%	100%	100%	86%
3	100%	100%	100%	100%	100%
2	100%	100%	100%	100%	100%
1	100%	100%	100%	100%	100%

MIC5891

8-Bit Serial Input Latched Source Driver

Preliminary Information

General Description

The MIC5891 latched driver is a high-voltage, high current integrated circuits comprised of eight CMOS data latches, CMOS control circuitry for the common STROBE and OUTPUT ENABLE, and bipolar Darlington transistor drivers for each latch.

Bipolar/MOS construction provides extremely low power latches with maximum interface flexibility.

The MIC5891 will typically operate at better than 5MHz with a 5V logic supply.

The CMOS inputs are compatible with standard CMOS, PMOS and NMOS logic levels. TTL circuits may be used with appropriate pull-up resistors to ensure a proper logic-high input.

A CMOS serial data output allows additional drivers to be cascaded when more than 8 bits are required.

The MIC5891 has open-emitter outputs with suppression diodes for protection against inductive load transients. The output transistors are capable of sourcing 500mA and will sustain at least 35V in the ON state.

Simultaneous operation of all drivers at maximum rated current requires a reduction in duty cycle due to package power limitations. Outputs may be paralleled for higher load current capability.

The MIC5891 is available in a 16-pin plastic DIP package (N), 16-pin CerDIP package (J), and 16-pin wide SOIC package (WM).

Features

- High-Voltage, High-Current Outputs
- Output Transient Protection Diodes
- CMOS, PMOS, NMOS, TTL Compatible Inputs
- 10MHz Minimum Data Input Rate
- Low-Power CMOS Latches

Applications

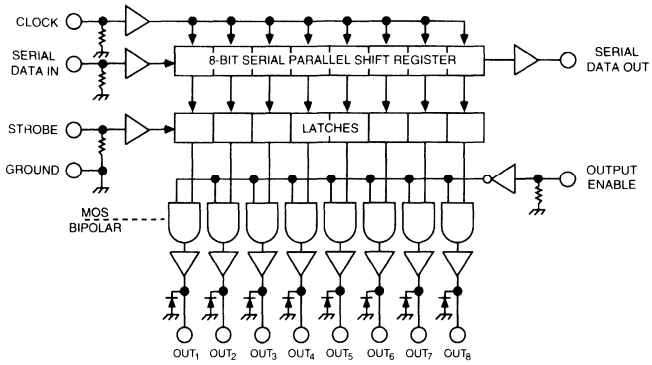
- Alphanumeric and Bar Graph Displays
- LED and Incandescent Displays
- Relay and Solenoid Drivers
- Other High Power Loads

3

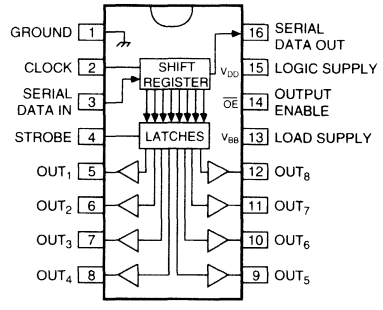
Ordering Information

Part Number	Temperature Range	Package
MIC5891AJ	–55°C to +125°C	16-Pin CerDIP
MIC5891BJ	–40°C to +85°C	16-Pin CerDIP
MIC5891BN	–40°C to +85°C	16-Pin Plastic DIP
MIC5891BWM	–40°C to +85°C	16-pin Wide SOIC

Functional Diagram

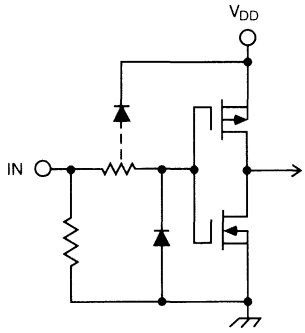


Pin Configurations

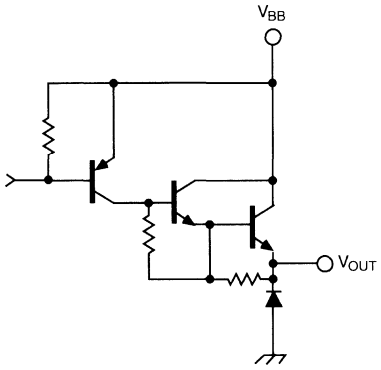


MIC5891

Typical Circuits

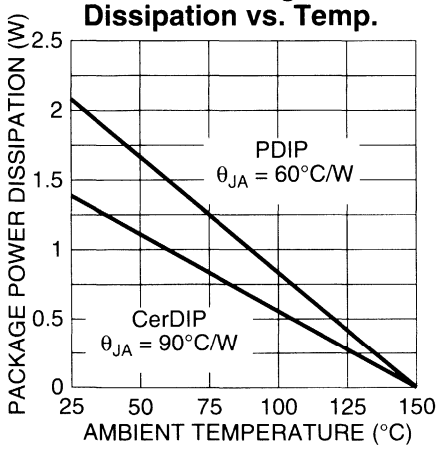


Typical Input Circuit



Typical Output Circuit

Allowable Package Power Dissipation vs. Temp.



Absolute Maximum Ratings: (Notes 1, 2)

at T_A = +25°C

Output Voltage, V_{OUT}	50V
Logic Supply Voltage Range, V_{DD}	4.5V to 15V
Load Supply Voltage Range, V_{BB}	5.0V to 50V
Input Voltage Range, V_{IN}	−0.3 V to V_{DD} + 0.3 V
Continuous Collector Current, I_C	500mA
Package Power Dissipation	See graph
Operating Temperature Range, T_A	−55°C to +125°C
Storage Temperature Range, T_S	−65°C to +150°C

Note 1: Derate at the rate of 20 mW/°C above T_A = 25°C

Note 2: Micrel CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges

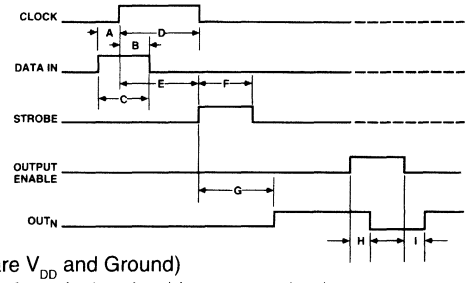
Allowable Duty Cycles

Number of Outputs ON at I_{OUT} = −200 mA	Max. Allowable Duty Cycles at T_A of:		
	50°C	60°C	70°C
8	53%	47%	41%
7	60%	54%	48%
6	70%	64%	56%
5	83%	75%	67%
4	100%	94%	84%
3	100%	100%	100%
2	100%	100%	100%
1	100%	100%	100%

Electrical Characteristics: at T_A = +25°C, V_{BB} = 50V, V_{DD} = 5V to 12V (unless otherwise noted).

Characteristic	Symbol	V_{BB}	Test Conditions	Limits		
				Min.	Max.	Units
Output Leakage Current	I_{CEX}	50V	T_A = +25°C		–50	µA
			T_A = +70°C		–100	µA
Output Saturation Voltage	$V_{CE(SAT)}$	50V	I_{OUT} = –100mA		1.8	V
			I_{OUT} = –225mA		1.9	V
			I_{OUT} = –350mA,		2.0	V
Output Sustaining Voltage	$V_{CE(SUS)}$	50V	I_{OUT} = –350mA, L = 2mH	35		V
Input Voltage	$V_{IN(1)}$	50V	V_{DD} = 5.0V	3.5	V_{DD}+0.3	V
			V_{DD} = 12V	10.5	V_{DD}+0.3	V
	$V_{IN(0)}$	50V	V_{DD} = 5V to 12V	V_{SS}–0.3	0.8	V
Input Current	$I_{IN(1)}$	50V	V_{DD} = V_{IN} = 5.0V		50	µA
			V_{DD} = 12V		240	µA
Input Impedance	Z_{IN}	50V	V_{DD} = 5.0V	100		kΩ
			V_{DD} = 12V	50		kΩ
Maximum Clock Frequency	f_c	50V		10		MHz
Serial Data Output Resistance	R_{OUT}	50V	V_{DD} = 5.0V		20	kΩ
			V_{DD} = 12V		6.0	kΩ
Turn-ON Delay	t_{PLH}	50V	Output Enable to Output, I_{OUT} = –350mA		2.0	µs
Turn-OFF Delay	t_{PHL}	50V	Output Enable to Output, I_{OUT} = –350mA		10	µs
Supply Current	I_{BB}	50V	All outputs ON, All outputs open		10	mA
			All outputs OFF		200	µA
	I_{DD}	50V	V_{DD} = 5V, All outputs OFF, Inputs = 0V		100	µA
			V_{DD} = 12V, All outputs OFF, Inputs = 0V		200	µA
			V_{DD} = 5V, One output ON, All Inputs = 0V		1.0	mA
			V_{DD} = 12V, One output ON, All Inputs = 0V		3.0	mA
Diode Leakage Current	I_H	Max	T_A = +25°C		50	µA
			T_A = +70°C		100	µA
Diode Forward Voltage	V_F	Open	I_F = 350mA		2.0	V

NOTE 1: Positive (negative) current is defined as going into (coming out of) the specified device pin.
NOTE 2: Operation of these devices with standard TTL may require the use of appropriate pull-up resistors.



Timing Conditions

(V_{DD} = 5.0V, Logic Levels are V_{DD} and Ground)

A. Minimum data active time before clock pulse (data set-up time) 75ns
B. Minimum data active time after clock pulse (data hold time) 75ns
C. Minimum data pulse width 150ns
D. Minimum clock pulse width 150ns
E. Minimum time between clock activation and strobe 300ns
F. Minimum strobe pulse width 100ns
G. Typical time between strobe activation and output transition 1.0µs
H. Turn-OFF Delay ..... see Electrical Characteristics
I Turn-ON Delay ..... see Electrical Characteristics

Serial data present at the input is transferred into the shift register on the rising edge of the CLOCK input pulse. Additional CLOCK pulses shift data information towards the SERIAL DATA OUTPUT. The serial data must appear at the input prior to the rising edge of the CLOCK input waveform.

The 8 bits present in the shift register are transferred to the respective latches when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Most applications where the latching feature is not used (STROBE tied high) require the OUTPUT ENABLE input to be high during serial data entry.

Outputs are active (controlled by the latch state) when the OUTPUT ENABLE is low. All Outputs are low (disabled) when the OUTPUT ENABLE is high. OUTPUT ENABLE does not affect the data in the shift register or latch.

Truth Table

Serial Data Input	Clock Input	Shift Register Contents						Serial Data Output	Strobe Input	Latch Contents						Output Enable	Output Content					
		I_1	I_2	I_3	...	I_{N-1}	I_N			I_1	I_2	I_3	...	I_{N-1}	I_n		I_1	I_2	I_3	...	I_{N-1}	I_n
H	⎍	H	R_1	R_2	...	R_{N-2}	R_{N-1}	R_{N-1}														
L	⎍	L	R_1	R_2	...	R_{N-2}	R_{N-1}	R_{N-1}														
X	⎎	R_1	R_2	R_3	...	R_{N-1}	R_N	R_N														
		X	X	X	...	X	X	X	L	R_1	R_2	R_3	...	R_{N-1}	R_N							
		P_1	P_2	P_3	...	P_{N-1}	P_N	P_N	H	P_1	P_2	P_3	...	P_{N-1}	P_N	L	P_1	P_2	P_3	...	P_{N-1}	P_N
										X	X	X	...	X	X	H	L	L	L	...	L	L

L = Low Logic Level
H = High Logic Level
X = Irrelevant
P = Present State
R = Previous State

MIC59P50

8-Bit Parallel Input Protected Latched Driver

General Description

The MIC59P50 parallel-input latched driver is a high-voltage (80V), high-current (500mA) integrated circuit comprised of eight CMOS data latches, a bipolar Darlington transistor driver for each latch, and CMOS control circuitry for the common CLEAR, STROBE, and OUTPUT ENABLE functions. Similar to the MIC5801, additional protection circuitry supplied on this device includes thermal shutdown, under voltage lockout (UVLO), and over-current shutdown.

The bipolar/MOS combination provides an extremely low-power latch with maximum interface flexibility. The MIC59P50 has open-collector outputs capable of sinking 500mA and integral diodes for inductive load transient suppression with a minimum output breakdown voltage rating of 80V above V_{EE} (50V sustaining). The drivers can be operated with a split supply, where the negative supply is down to –20V and may be paralleled for higher load current capability.

With a 5V logic supply, the MIC59P50 will typically operate at better than 5MHz. With a 12V logic supply, significantly higher speeds are obtained. The CMOS inputs are compatible with standard CMOS, PMOS, and NMOS circuits. TTL circuits may require pull-up resistors.

Each of these eight outputs has an independent over-current shutdown at 500 mA. Upon current shutdown, the affected channel will turn OFF and the flag will go low until V_{DD} is cycled or the $\overline{\text{ENABLE}}$/RESET pin is pulsed high. Current pulses less than 2µs will not activate over-current shutdown. Temperatures above 165°C will shut down the device and activate the open collector FLAG output at pin 1. The UVLO circuit disables the outputs at low V_{DD}; hysteresis of 0.5V is provided.

Features

- 4.4 MHz Minimum Data Input Rate
- High-Voltage, High-Current Outputs
- Per-Output Over-Current Shutdown (500mA Typical)
- Undervoltage Lockout
- Thermal Shutdown
- Output Fault Flag
- Output Transient Protection Diodes
- CMOS, PMOS, NMOS, and TTL Compatible Inputs
- Internal Pull-Down Resistors
- Low-Power CMOS Latches
- Single or Split Supply Operation

3

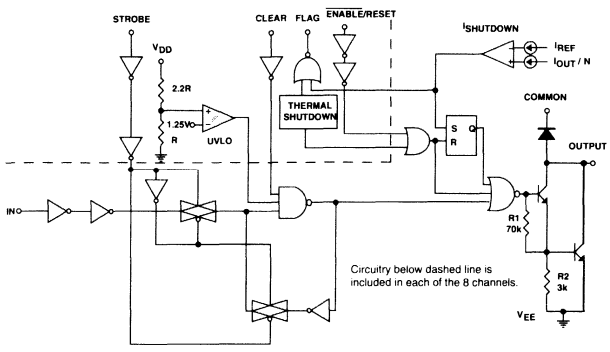
Ordering Information

Part Number	Temperature Range	Package
MIC59P50AJ	–55°C to +125°C	24-Pin Ceramic DIP*
MIC59P50AJB†	–55°C to +125°C	24-Pin Ceramic DIP*
MIC59P50BN	–40°C to +85°C	24-Pin Plastic DIP*
MIC59P50BV	–40°C to +85°C	28-Pin PLCC
MIC59P50BWM	–40°C to +85°C	24-Pin Wide SOIC

* 300-mil "skinny-DIP"

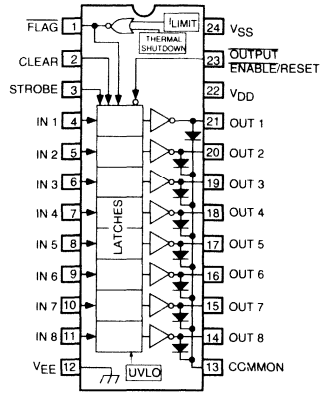
† AJB indicates units screened to MIL-STD 883, Method 5004, condition B, and burned-in for 1-week.

Functional Diagram



Pin Configuration

(Ceramic and Plastic DIP and SOIC)



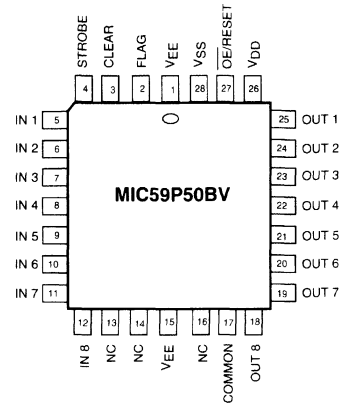
Absolute Maximum Ratings: (Note 1)

at +25°C Free-Air Temperature

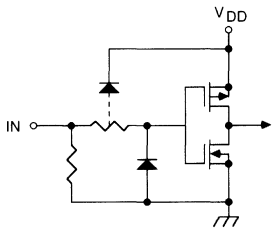
Output Voltage, V_{CE}	80V
Supply Voltage, V_{DD}	15V
$V_{DD} - V_{EE}$	25V
Input Voltage Range, V_{IN}	–0.3V to V_{DD} + 0.3V
Continuous Collector Current, I_C	500mA
Package Power Dissipation	
MIC59P50BN	2.4W
Derate above T_A = +25°C	24mW/°C
MIC59P50AJ	2.2W
Derate above T_A = +25°C	22mW/°C
MIC59P50BV	1.6W
Derate above T_A = +25°C	16mW/°C
MIC59P50BWM	1.4W
Derate above T_A = +25°C	14mW/°C
Operating Temperature Range, T_A	–40°C to +85°C
Storage Temperature Range, T_S	–65°C to +125°C

Note 1: Micrel CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.

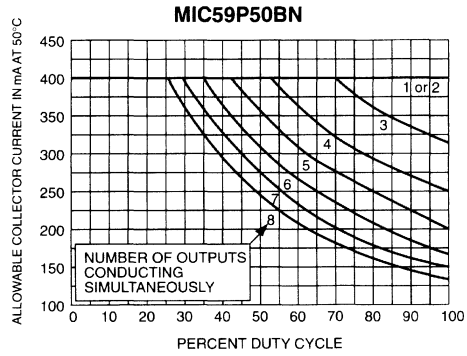
PLCC Pin Configuration



Typical Input



Allowable Output Current As A Function of Duty Cycle



Pin Description

Pin (DIP & SO)	Name	Description
1	FLAG	Error Flag. Open Collector Output is Low upon Overcurrent Fault or Overtemperature Fault. OUTPUT ENABLE/RESET must be pulled high to reset the flag and fault condition.
2	CLEAR	Sets All Latches OFF (open).
3	STROBE	Input Strobe Pin. Loads output latches when High.
4–11	INPUT	Parallel Inputs, 1 through 8
12	V_{EE}	Output Ground (Substrate). Most negative voltage in the system connects here.
13	COMMON	Transient suppression diodes cathode common pin.
14–21	OUTPUT	Parallel Outputs, 8 through 1.
22	V_{DD}	Logic Positive Supply voltage.
23	$\overline{\text{OUTPUT}}$ $\overline{\text{ENABLE}}$/RESET	When Low, Outputs are active. When High, outputs are inactive and the Flag and outputs are reset from a fault condition. An undervoltage condition emulates a high $\overline{\text{OE}}$ input.
24	V_{SS}	Logic reference (Ground) pin.

Electrical Characteristics: at T_A = +25°C, V_{DD} = 5V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Output Leakage Current	I_{CEX}	V_{CE} = 80V, T_A = +25°C			50	µA
		V_{CE} = 80V, T_A = +70°C			100	
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 100 mA		0.9	1.1	V
		I_C = 200 mA		1.1	1.3	
		I_C = 350 mA		1.3	1.6	
Input Voltage	$V_{IN(0)}$				1.0	V
	$V_{IN(1)}$	V_{DD} = 12V	10.5			
		V_{DD} = 10V	8.5			
		V_{DD} = 5.0V (See Note)	3.5			
Input Resistance	R_{IN}	V_{DD} = 12V	50	200		kΩ
		V_{DD} = 10V	50	300		
		V_{DD} = 5.0V	50	600		
Supply Current	$I_{DD(ON)}$ (One output active)	V_{DD} = 12V, Outputs Open		3.3	4.5	mA
		V_{DD} = 10V, Outputs Open		3.1	4.5	
		V_{DD} = 5.0V, Outputs Open		2.4	3.6	
	$I_{DD(ON)}$ (All outputs active)	V_{DD} = 12V, Outputs Open		6.4	10.0	mA
		V_{DD} = 10V, Outputs Open		6.0	9.0	
		V_{DD} = 5.0V, Outputs Open		4.7	7.5	
	$I_{DD(OFF)}$ (Total)	V_{DD} = 12V, Outputs Open, Inputs = 0V		3.0	4.5	mA
		V_{DD} = 5.0V, Outputs Open, Inputs = 0V		2.2	3.6	
Clamp Diode Leakage Current	I_R	V_R = 80V, T_A = +25°C			50	µA
		V_R = 80V, T_A = +70°C			100	
Over-Current Threshold	I_{LIM}	Each Output		500		mA
Start-Up Voltage	V_{SU}	Note 2	3.5	4.0	4.5	V
Minimum Operating V_{DD}	$V_{DD\ MIN}$		3.0	3.5	4.0	V
Clamp Diode Forward Voltage	V_F	I_F = 350 mA		1.7	2.0	V
Thermal Shutdown				165		°C
Thermal Shutdown Hysteresis				10		

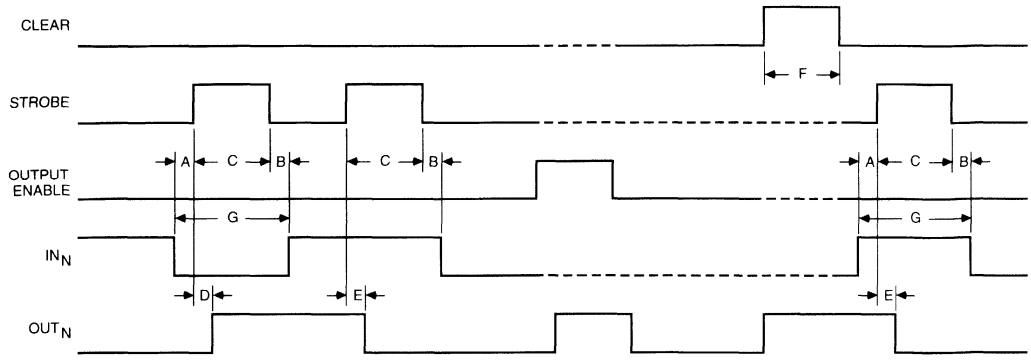
NOTE 1: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to insure a minimum logic "1".
NOTE 2: Under-Voltage Lockout is guaranteed to release device at no more than 4.5V, and disable the device at no less than 3.0V.

Truth Table

IN_N	Strobe	Clear	Output Enable	OUT_N	
				t–1	t
0	1	0	0	X	OFF
1	1	0	0	X	ON
X	X	1	X	X	OFF
X	X	X	1	X	OFF
X	0	0	0	ON	ON
X	0	0	0	OFF	OFF

X = Irrelevant
t–1 = previous output state
t = present output state

Information present at an input is transferred to its latch when the STROBE is high. A high CLEAR input will set all latches to the output OFF condition regardless of the data or STROBE input levels. A high OUTPUT ENABLE will set all outputs to the off condition, regardless of any other input conditions. When the OUTPUT ENABLE is low, the outputs depend on the state of their respective latches. If current shutdown is activated, the OUTPUT ENABLE must be pulsed high to restore operation and reset the Flag. Over temperature faults are not latched and require no reset pulse.



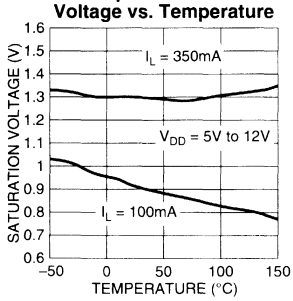
Timing Conditions

(T_A = +25°C, Logic Levels are V_{DD} and V_{SS}, V_{DD} = 5V).

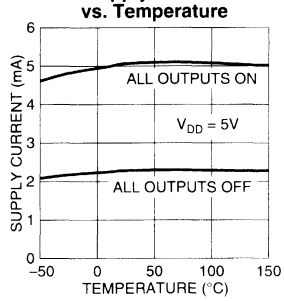
A. Minimum data active time before strobe enabled (data set-up time) ..... 50 ns
B. Minimum data active time after strobe disabled (data hold time) ..... 50 ns
C. Minimum strobe pulse width ..... 125 ns
D. Typical time between strobe activation and output on to off transition ..... 500 ns
E. Typical time between strobe activation and output off to on transition ..... 500 ns
F. Minimum clear pulse width ..... 300 ns
G. Minimum data pulse width ..... 225 ns

Typical Characteristic Curves

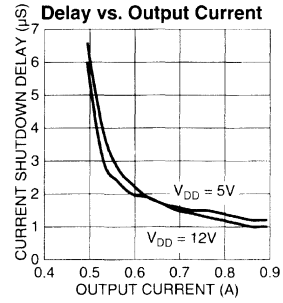
Output Saturation Voltage vs. Temperature



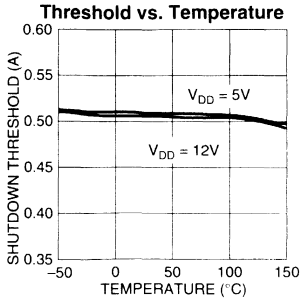
Supply Current vs. Temperature



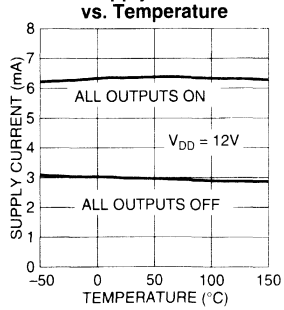
Current Shutdown Delay vs. Output Current



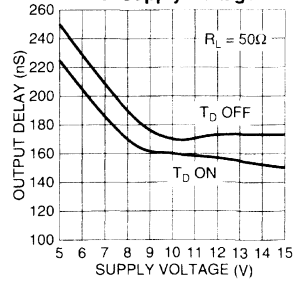
Current Shutdown Threshold vs. Temperature



Supply Current vs. Temperature

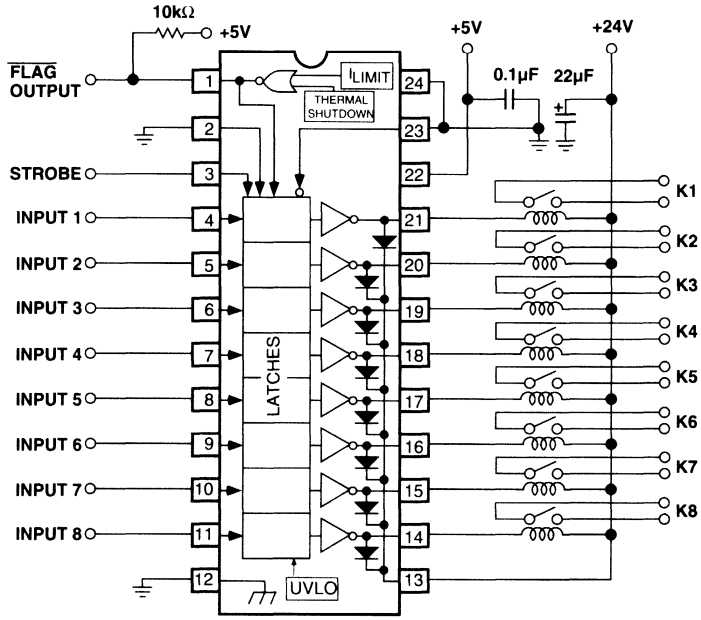


Output Enable Delay vs. Supply Voltage

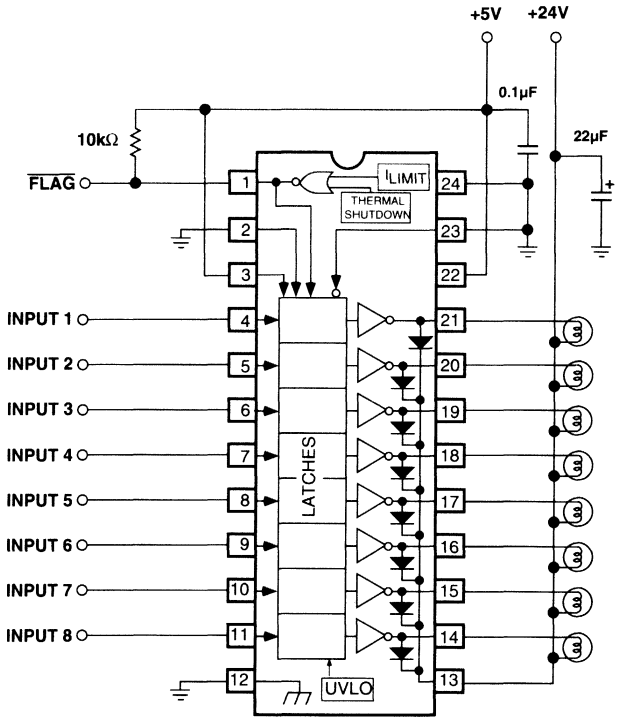


Typical Applications

MIC59P50 Protected Relay Driver



MIC59P50 Protected Lamp Driver



MIC59P60

8-Bit Serial-Input Protected Latched Driver

Preliminary Information

General Description

The MIC59P60 serial-input latched driver is a high-voltage (80V), high-current (500mA) integrated circuit comprised of eight CMOS data latches, a bipolar Darlington transistor driver for each latch, and CMOS control circuitry for the common CLEAR, STROBE, CLOCK, SERIAL DATA INPUT, and OUTPUT ENABLE functions. Similar to the MIC5842, additional protection circuitry supplied on this device includes thermal shutdown, under voltage lockout (UVLO), and over-current shutdown.

The bipolar/CMOS combination provides an extremely low-power latch with maximum interface flexibility. The MIC59P60 has open-collector outputs capable of sinking 500mA and integral diodes for inductive load transient suppression with a minimum output breakdown voltage rating of 80V (50V sustaining). The drivers can be operated with a split supply, where the negative supply is down to –20V and may be paralleled for higher load current capability.

Using a 5V logic supply, the MIC59P60 will typically operate at better than 5MHz. With a 12V logic supply, significantly higher speeds are obtained. The CMOS inputs are compatible with standard CMOS, PMOS, and NMOS circuits. TTL circuits may require pull-up resistors. By using the serial data output, drivers may be cascaded for interface applications requiring additional drive lines.

Each of these eight outputs has an independent over current shutdown of 500 mA. Upon over-current shutdown, the affected channel will turn OFF and the flag will go low until V_{DD} is cycled or the ENABLE/RESET pin is pulsed high. Current pulses less than 2µs will not activate current shutdown. Temperatures above 165°C will shut down the device and activate the error flag. The UVLO circuit prevents operation at low V_{DD}; hysteresis of 0.5V is provided.

Features

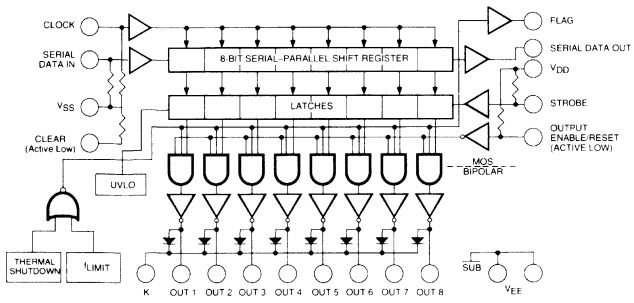
- 3.3 MHz Minimum Data-Input Rate
- Output Current Shutdown (500mA Typical)
- Under Voltage Lockout
- Thermal Shutdown
- Output Fault Flag
- CMOS, PMOS, NMOS, and TTL Compatible
- Internal Pull-Up/Pull-Down Resistors
- Low Power CMOS Logic and Latches
- High Voltage Current Sink Outputs
- Output Transient-Protection Diodes
- Single or Split Supply Operation

Ordering Information

Part Number	Temperature Range	Package
MIC59P60AJ	–55°C to +125°C	20-Pin Ceramic DIP
MIC59P60AJB†	–55°C to +125°C	20-Pin Ceramic DIP
MIC59P60BN	–40°C to +85°C	20-Pin Plastic DIP
MIC59P60BV	–40°C to +85°C	20-Pin PLCC
MIC59P60BWM	–40°C to +85°C	20-Pin Wide SOIC

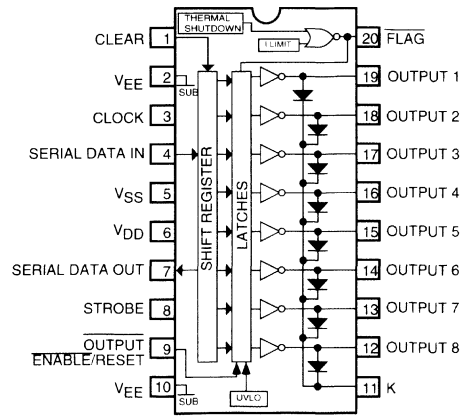
† AJB indicates units screened to MIL-STD 883, Method 5004, condition B, and burned-in for 1 week.

Functional Diagram

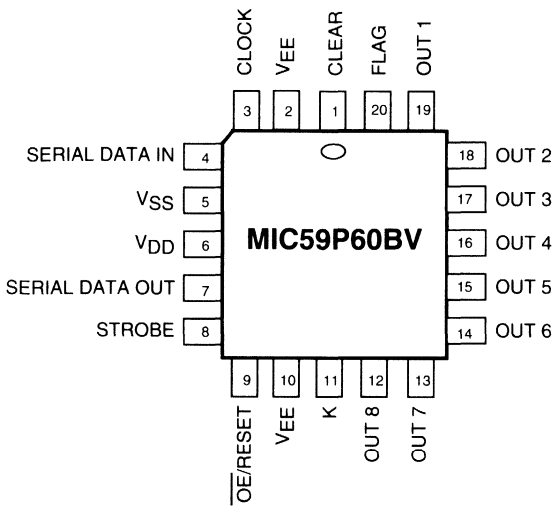


Pin Configuration

(Ceramic and Plastic DIP and SOIC)



PLCC Pin Configuration



Absolute Maximum Ratings (Note 1, 2)

at 25°C Free-Air Temperature and V_{SS} = 0V

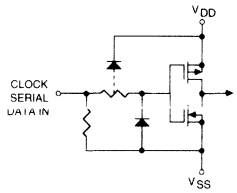
Output Voltage, V_{CE}	80V
Output Voltage, $V_{CE(SUS)}$ (Note 1)	50V
V_{DD} with Reference to V_{SS}	15V
V_{DD} with Reference to V_{EE}	25V
Emitter Supply Voltage, V_{EE}	–20V
Input Voltage Range, V_{IN}	–0.3V to V_{DD} + 0.3V
Package Power Dissipation:	
MIC59P60BN	2.0W
Derate above T_A = +25°C	20mW/°C
MIC59P60AJ/AJB	1.8W
Derate above T_A = +25°C	18mW/°C
MIC59P60BV	1.4W
Derate above T_A = +25°C	14mW/°C
MIC59P60BWM	1.2W
Derate above T_A = +25°C	12mW/°C
Operating Temperature Range, T_A	–55°C to +125°C
Storage Temperature Range, T_S	–65°C to +125°C

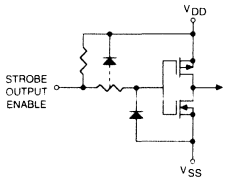
Note 1: For Inductive load applications.

Note 2: CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.

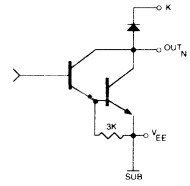
3

Typical Input Circuits





Typical Output Driver



Pin Description

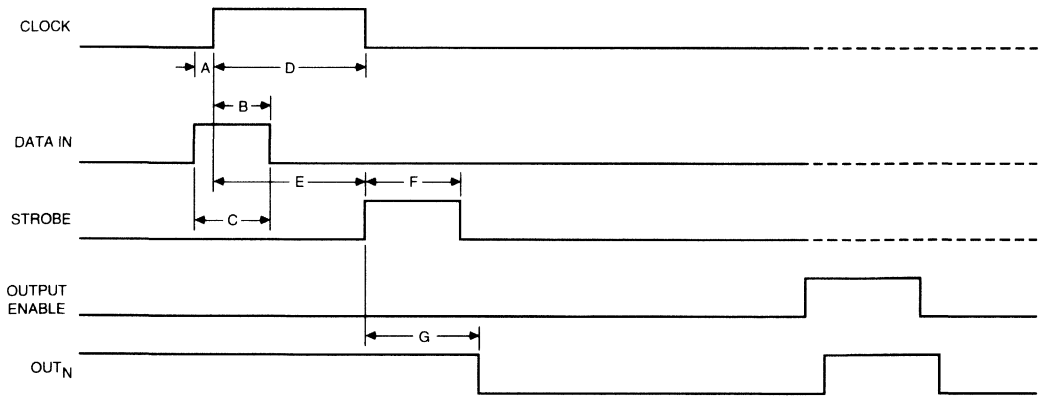
Pin	Name	Description
1	CLEAR	Sets All Latches OFF (open).
2,10	V_{EE}	Output Ground (Substrate). Most negative voltage in the system connects here.
3	CLOCK	Serial Data Clock. A CLEAR must also be clocked into the latches.
4	SERIAL DATA IN	Serial Data Input pin.
5	V_{SS}	Logic reference (Ground) pin.
6	V_{DD}	Logic Positive Supply voltage.
7	SERIAL DATA OUT	Serial Data Output pin. (Flow through).
8	STROBE	Output Strobe pin. Loads output latches when High. A STROBE is needed to CLEAR latches.
9	$\overline{\text{OUTPUT}}$ $\overline{\text{ENABLE}}$/RESET	When Low, Outputs are active. When High, device is inactive andreset from a fault . condition. An under voltage condition emulates a high $\overline{\text{OE}}$/RESET input.
11	K	Transient suppression diode's cathode common pin.
12—19	OUTPUT N	Open Collector outputs 8 through 1.
20	$\overline{\text{FLAG}}$	Error Flag. Flag is Low upon Overcurrent Fault or Overtemperature fault. $\overline{\text{OUTPUT ENABLE}}$/RESET must be pulled high to reset the flag and fault condition.

Electrical Characteristics at T_A = +25°C, V_{DD} = 5V, V_{SS} = V_{EE} = 0V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Unit
Output Leakage Current	I_{CEX}	V_{OUT} = 80V			50	µA
		V_{OUT} = 80V, T_A = +70°C			100	
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_{OUT} = 100mA		0.9	1.1	V
		I_{OUT} = 200mA		1.1	1.3	
		I_{OUT} = 350mA		1.3	1.6	
Collector-Emitter Sustaining Voltage	$V_{CE(SUS)}$	I_{OUT} = 350mA, L = 2mH	50			V
Input Voltage	$V_{IN(0)}$				1.0	V
	$V_{IN(1)}$	V_{DD} = 12V	10.5			
		V_{DD} = 10V	8.5			
		V_{DD} = 5.0V	3.5			
Input Resistance	R_{IN}	V_{DD} = 12V	50	200		kΩ
		V_{DD} = 10V	50	300		
		V_{DD} = 5.0V	50	600		
Supply Current	$I_{DD(ON)}$	All Drivers ON, V_{DD} = 12V		6.4	10.0	mA
		All Drivers ON, V_{DD} = 10V		6.0	9.0	
		All Drivers ON, V_{DD} = 5.0V		4.6	7.5	
	I_{DD} (1 OUTPUT)	One Driver ON, All others OFF, V_{DD} = 12V		3.1	4.5	
		One Driver ON, All others OFF, V_{DD} = 10V		2.9	4.5	
		One Driver ON, All others OFF, V_{DD} = 5V		2.3	3.6	
	$I_{DD(OFF)}$	All Drivers OFF, V_{DD} = 12V		2.6	4.2	
		All Drivers OFF, V_{DD} = 10V		2.4	3.6	
		All Drivers OFF, V_{DD} = 5.0V		1.9	3.0	
Clamp Diode Leakage Current	I_R	V_R = 80V			50	µA
Clamp Diode Forward Voltage	V_F	I_F = 350mA		1.7	2.0	V
Over Current Shutdown Threshold	I_{LIM}			500		mA
Start Up Voltage	V_{SU}	Note 1.	3.5	4.0	4.5	V
Minimum Supply (V_{DD})	$V_{DD\ MIN}$		3.0	3.5	4.0	V
Thermal Shutdown				165		°C
Thermal Shutdown Hysteresis				10		

Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to insure a minimum logic "1".

Note 1: Under-voltage lockout is guaranteed to release device at no more than 4.5V, and disable the device at no less than 3.0V



Timing Conditions

(T_A = +25°C, Logic Levels are V_{DD} and V_{SS}, V_{DD} = 5V)

A. Typical Data Active Time Before Clock Pulse (Data Set-Up Time) ..... 75 ns
B. Minimum Data Active Time After Clock Pulse (Data Hold Time) ..... 75 ns
C. Minimum Data Pulse Width ..... 150 ns
D. Minimum Clock Pulse Width ..... 150 ns
E. Minimum Time Between Clock Activation and Strobe ..... 300 ns
F. Minimum Strobe Pulse Width ..... 100 ns
G. Typical Time Between Strobe Activation and Output Transition ..... 500 ns

3

SERIAL DATA present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform. Holding CLEAR high results in a data logic "0" being clocked into the shift register, turning off respective channels.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the ENABLE input be high to prevent invalid output states.

When the ENABLE input is high, all of the output buffers are disabled (OFF) without affecting information stored in the latches or shift register. With the ENABLE input low, the outputs are controlled by the state of the latches. A positive OE/RESET pulse resets the FLAG and the output after a current shutdown fault. Over-temperature faults are not latched and require no reset pulse.

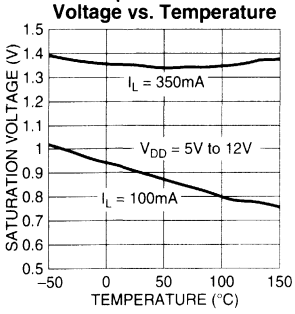
MIC59P60 Truth Table

Serial Data Input	Clear Input	Clock Input	Shift Register Contents I_1	I_2	I_3	I_8	Serial Data Output	Strobe Input	Latch Contents I_1	I_2	I_3	I_8	Output Enable	Output Contents I_1	I_2	I_3	I_8
H		↑	H	R_1	R_2	R_7	R_7										
L		↑	L	R_1	R_2	R_7	R_7										
X		↓	R1	R2	R_3	R_8	R_8										
	H	↑	O	O	O	O	L										
			X	X	X	X	X	L	R_1	R_2	R_3	R_8					
			P_1	P_2	P_3	P_8	P_8	H	P_1	P_2	P_3	P_8	L	P_1	P_2	P_3	P_8
									X	X	X	X	H	H	H	H	H

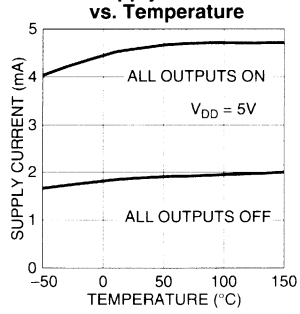
L = Low Logic Level
H = High Logic Level
X = Irrelevant
P = Present State
R = Previous State
O = Output OFF

Typical Characteristic Curves

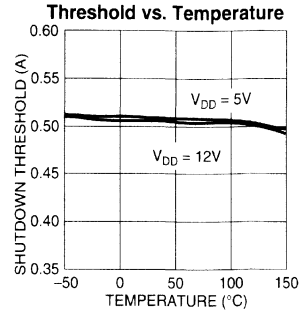
Output Saturation Voltage vs. Temperature



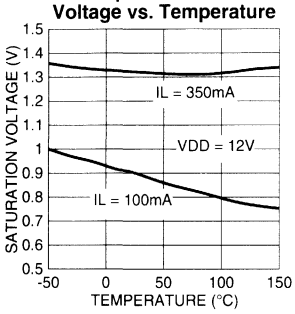
Supply Current vs. Temperature



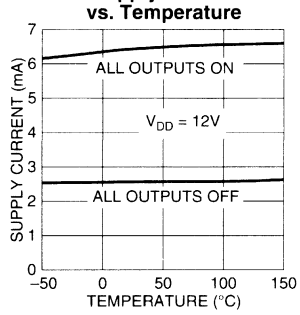
Current Shutdown Threshold vs. Temperature



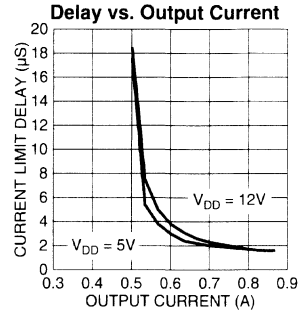
Output Saturation Voltage vs. Temperature



Supply Current vs. Temperature



Current Shutdown Delay vs. Output Current



Maximum Allowable Duty Cycle (Plastic DIP)

V_{DD} = 5.0V

Number of Outputs ON (I_{OUT} = 200mA V_{DD} = 5.0V)	Max. Allowable Duty Cycle at Ambient Temperature of				
	25°C	40°C	50°C	60°C	70°C
8	85%	72%	64%	55%	46%
7	97%	82%	73%	63%	53%
6	100%	96%	85%	73%	62%
5	100%	100%	100%	88%	75%
4	100%	100%	100%	100%	93%
3	100%	100%	100%	100%	100%
2	100%	100%	100%	100%	100%
1	100%	100%	100%	100%	100%

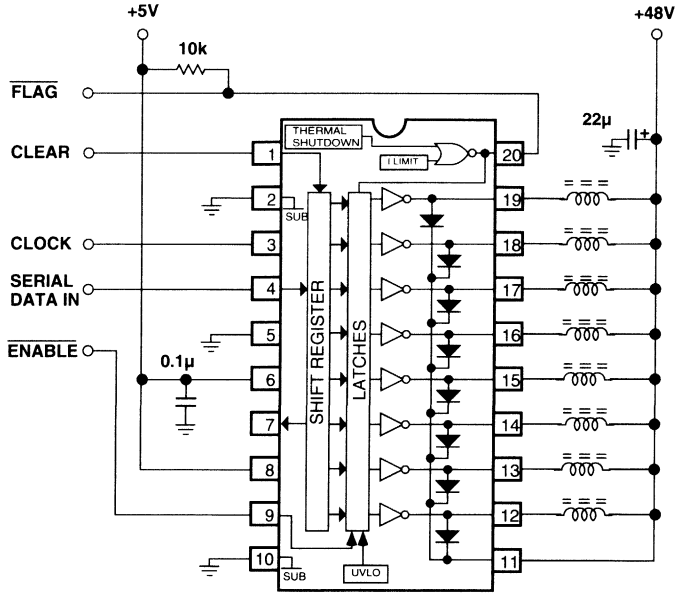
V_{DD} = 12V

Number of Outputs ON (I_{OUT} = 200mA V_{DD} = 12V)	Max. Allowable Duty Cycle at Ambient Temperature of				
	25°C	40°C	50°C	60°C	70°C
8	80%	68%	60%	52%	44%
7	91%	77%	68%	59%	50%
6	100%	90%	79%	69%	58%
5	100%	100%	95%	82%	69%
4	100%	100%	100%	100%	86%
3	100%	100%	100%	100%	100%
2	100%	100%	100%	100%	100%
1	100%	100%	100%	100%	100%

3

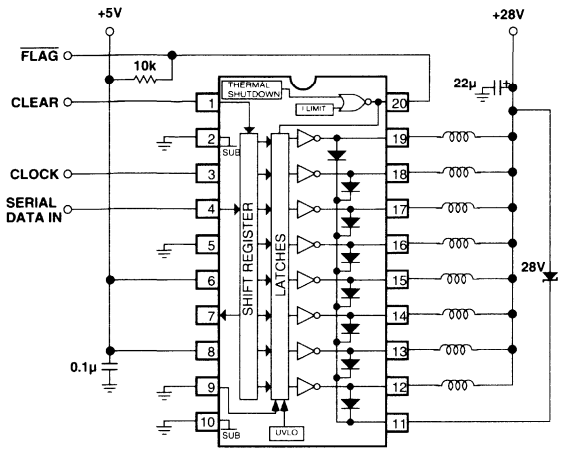
Typical Applications

Protected Solenoid Driver with Output Enable

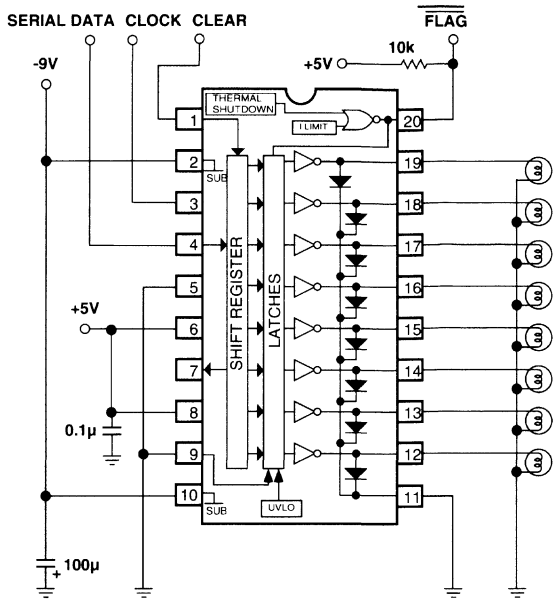


Typical Applications, continued

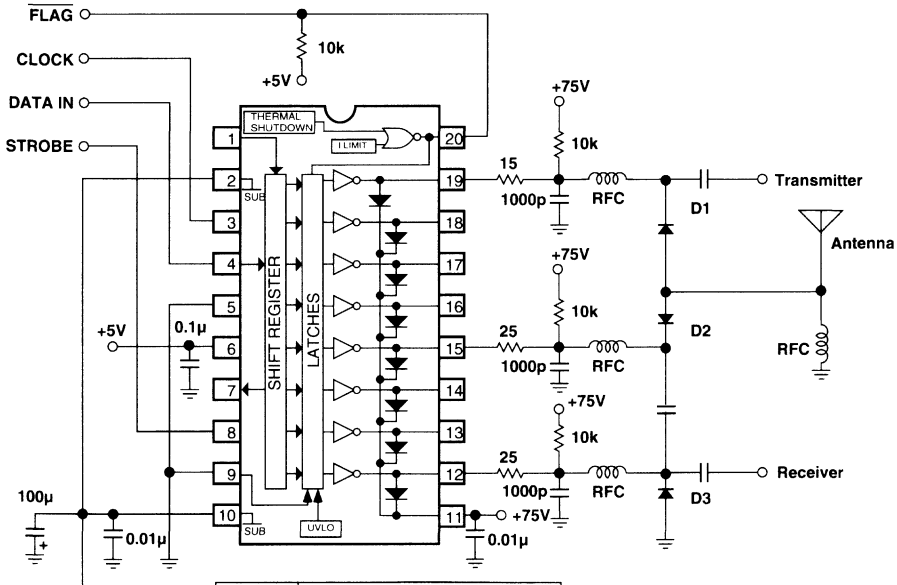
Hammer Driver



Protected Level Shifting Lamp Driver with Darlington Emitters Tied To a Negative Supply



Protected Negative/Positive PIN Diode Driver Transmit/Receive Switch



	Diode		
	D1 (Latch 1)	D2 (Latch 5)	D3 (Latch 8)
Receive	OFF	ACTIVE	OFF
Transmit	ACTIVE	OFF	ACTIVE

PIN Diodes: UM9651

Application Note 2

MIC4807 Display Dimmer

by Mitchell Lee

Abstract

The MIC4807 is an 8 channel, addressable low side driver and is guaranteed to deliver 100mA minimum at up to 80V per channel. This note discusses the operation of the MIC4807 and shows how it can be used as a display driver with dimming for incandescent indicators.

Introduction

The MIC4807 contains 8 low side drivers that are controlled by addressable latches (see Figure 1). Open-drain, N-channel MOSFETs of approximately 5.1Ω "on" resistance are used as output devices. The MOSFETs are designed for operation to 80V.

Each output is controlled by its own addressable latch; the latches are selected by a 3-bit parallel address (A_{in}, B_{in}, and C_{in}). A "1" at the data input turns the corresponding MOSFET on.

Power ICs demand protection from excessive current and dissipation, and to this end the MIC4807 includes short-circuit current limiting and thermal shutdown. In fact, the chip can withstand a dead short to 80V without damage. The output limits at typically 200mA, and the chip is guaranteed to deliver 100mA minimum over temperature. While current limiting provides short-term protection from load faults, thermal shutdown protects against sustained fault conditions by shutting off all outputs when the die temperature exceeds 150°C. Current limiting and thermal shutdown are indispensable, yet they are sorely lacking in many other functionally similar ICs where the implementation of protection circuits is left as an exercise for the user.

Incandescent Lamp Characteristics

Owing to their superior light output, incandescent lamps are preferred over other display devices for use in bright environments. Unfortunately, incandescent lamps have a number of characteristics that make them difficult to work with in practical applications. For example, lamps do not lend themselves to multiplexing. It is technically possible to multiplex lamps by a higher-than-rated supply voltage in conjunction with PWM techniques to control filament power dissipation.

A major pitfall of multiplexing is reliability. If the multiplex circuit fails to advance for any reason (power-up phenomenon, slow or stuck oscillator, etc.) the lamps will burn out instantly. In addition, the switched current increases proportionally with the supply voltage, necessitating larger switches.

Since multiplexing is impractical, each lamp must have its own dedicated driver. This adds circuit overhead not only in the number of drivers, but also in terms of communicating with the drivers.

The brightness of an incandescent lamp is an asset in brightly illuminated environments, but what happens at night? Under contrasting conditions of low ambient light levels, the bright display can temporarily blind persons viewing it. Examples of environments with wide-ranging light levels include the cockpit of an airplane, or the operator's cab on farm or construction machinery. A dimming feature is highly desirable for any incandescent display.

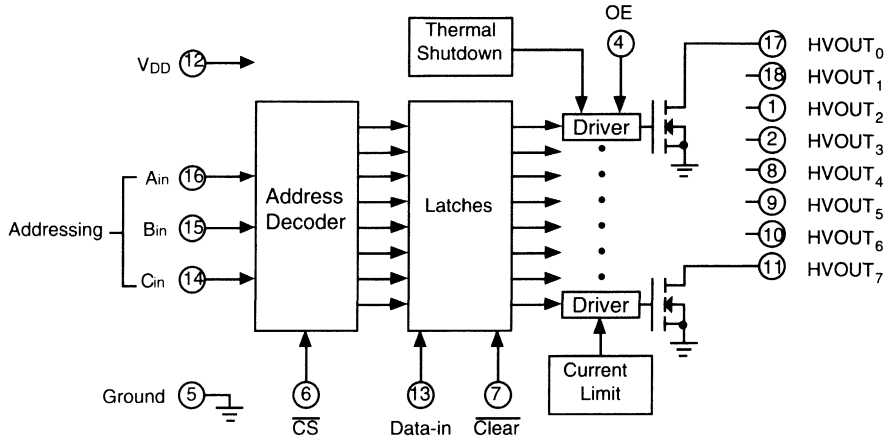


Figure 1. MIC4807 Block Diagram

Unlike LEDs, incandescent lamps require more current and voltage than 5V digital logic circuits can deliver. In particular, lamps draw an appreciable inrush current because the filament resistance is much lower when cold than when hot. Inrush currents of 10 times rated operating current are not uncommon. This impacts both the current rating of the driver and the lifetime of the lamp. Among other contributing factors, lamp lifetime is limited by the severe thermal shock experienced at turn-on.

Display Driver

Figure 2 shows a practical display driver circuit using the MIC4807. #1835 miniature lamps were selected for use on a loosely regulated "48V" system supply, which normally ran about 110% rated voltage. The #1835 lamp is specified at 55V and 50mA, and it can easily withstand ±15% variations in a 48V supply without loss of rated life. The lamps are housed in #31099 (GTE/Sylvania) indicator assemblies. Output current limit precludes the possibility of chip destruction from short circuit conditions such as arise when a lamp socket is "tested" for power with the conductive end of a screwdriver. Long-term short circuits (wiring faults) are handled by the MIC4807's thermal shutdown circuit.

When the MIC4807 cold-starts a #1835 lamp, the output is immediately driven into current limit since it cannot deliver the full inrush current. The cold resistance of a #1835 lamp is approximately 94Ω; an initial current of 585mA would flow if connected directly to 55V. The MIC4807 current limit is typically 200mA at room temperature, which reduces the thermal shock at turn-on and increases lamp lifetime. Note that applying 200mA to the cold filament is equivalent to an initial lamp voltage of only 18.8V.

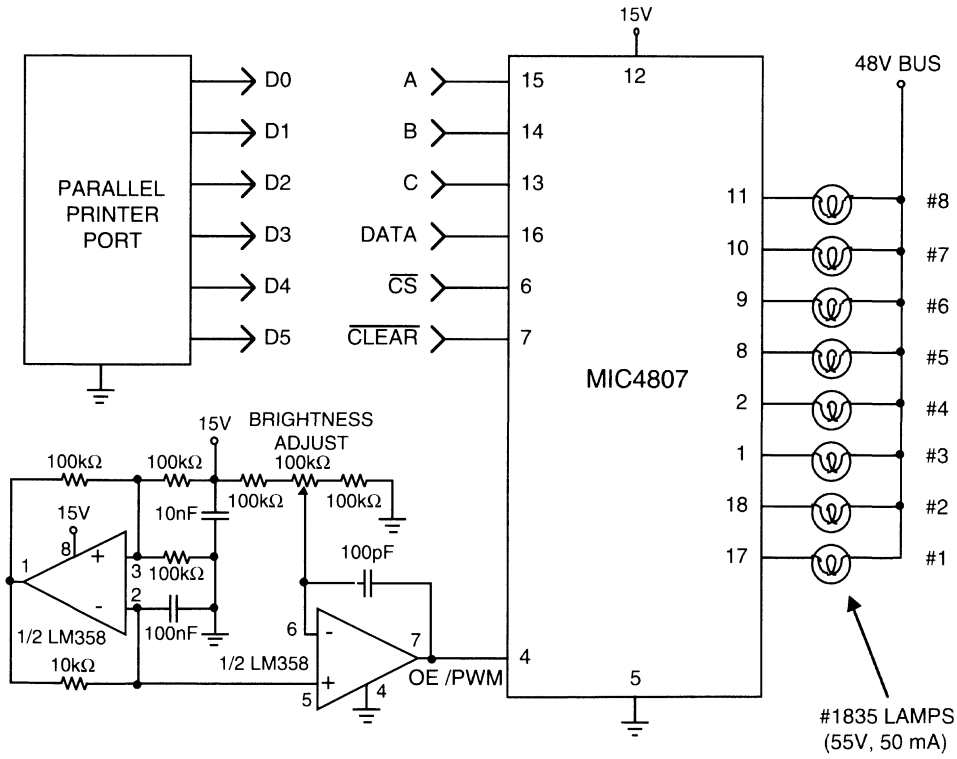


Figure 2. MIC4807 Display Controller with PWM Dimming

Display Dimming

Dimming is achieved by pulse-width modulation applied to the OUTPUT ENABLE (OE) pin. Since OUTPUT ENABLE acts on all 8 channels, the lamps are simultaneously dimmed by one control signal and maintain equal brightness, regardless of the dimming level.

An LM358 dual op-amp forms the basis of a variable PWM. The control range extends from completely off to completely on, and to any intermediate brightness level.

The PWM frequency (400Hz) is considerably higher than the filament's thermal time constant, so the filament's resistance (and temperature) changes very little between "on" and "off" periods. Figure 3 shows the pulsed filament current in a PWM application for a single #1835 lamp as a function of duty cycle. Lamp manufacturers recommend a PWM frequency of at least 400Hz to eliminate aging effects associated with thermal cycling. At an extremely dim 10% duty cycle, a #1835 lamp accepts current pulses of 90mA on a 55V supply, exhibiting a filament resistance of 611Ω. At 100% duty cycle the current falls to 50mA, at a resistance of 1100Ω. In any dimming circuit the driver circuitry must be sized to deliver the pulsed, low duty cycle current required by the relatively cool filament. This is typically twice the rated (100% duty cycle) lamp current.

MIC4807 Programming

The MIC4807 programming interface consists of a 3-bit address, a data line, and two control lines (see Figure 2). $\overline{\text{CLEAR}}$ is straightforward; a low on this pin asynchronously clears the internal latches to turn all outputs off. Programming is accomplished by addressing an output, presenting the desired data (1 = ON, 0 = OFF), and strobing $\overline{\text{CHIP SELECT}}$ with a logic low. DATA is transferred to the addressed output on the falling edge of $\overline{\text{CHIP SELECT}}$, and is latched in place when $\overline{\text{CHIP SELECT}}$ returns to a high state. In larger displays, $\overline{\text{CHIP SELECT}}$ serves as a means of controlling several MIC4807s while the address, OUTPUT ENABLE, $\overline{\text{CLEAR}}$, and DATA lines are paralleled.

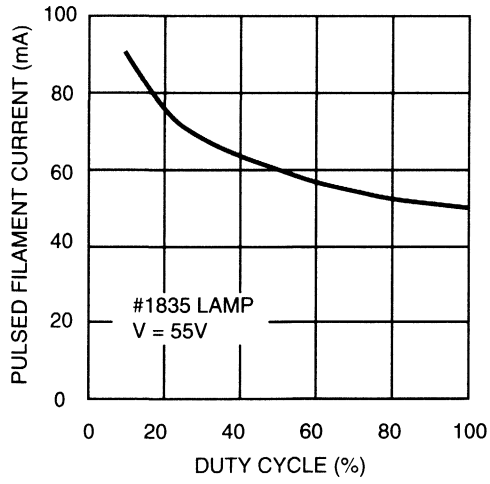


Figure 3. Pulsed Filament Current vs. Duty Cycle

For bench testing purposes a personal or laptop/portable computer is quite useful. A parallel printer port is commonly available and serves as a convenient means of programming one or more MIC4807s. Software changes can be made quickly and easily and, depending on the programming language used, the program can be stepped manually so that each bit can be checked "on the fly." This presents no problems because the MIC4807 is fully static.

An evaluation program written in BASIC is listed in Figure 4. The program consists of 5 parts. The control/input section is lines 100 through 130. This portion scans the keyboard, and branches to other parts of the program depending on which key is pressed. A "line return" branches to lines 3000 through 3030 where the MIC4807 is cleared and the computer's record of the MIC4807 latch states [8-element array D(A)] is cleared. Execution then returns to lines 100 through 130. A "?" invokes a lamp test function—all of the outputs are turned on by lines 2000 through 2060. Pressing any other key reprograms the MIC4807 with the original data, and returns execution to lines 100 through 130. Pressing any number from 1 to 8 toggles the associated output on or off (lines 1000 through 1020). Lines 4000 through 4020 are accessed from several points in the program; these lines write data to a given address by toggling $\overline{\text{CHIP SELECT}}$.

The parallel output word is given a value according to which MIC4807 pins should be high or low at any given time. A_{in} has a numeric (decimal) value of 1, B_{in} = 2, C_{in} = 4, DATA = 8, $\overline{\text{CHIP SELECT}}$ = 16, and $\overline{\text{CLEAR}}$ = 32 to represent a logical "1" at each pin. The port number (8) specified in the "OUT" statements will vary from computer to computer. While final evaluation of data communications must be carried out with the actual host processor, using a computer during the debugging phase of the display design is most helpful.

An equivalent block diagram of the MIC4807 logic circuitry is shown in Figure 5. Note that $\overline{\text{CHIP SELECT}}$, DATA, $\overline{\text{CLEAR}}$, AND OUTPUT ENABLE operate on all channels in parallel. The address decoder determines to which latch $\overline{\text{CHIP SELECT}}$ is directed. DATA has no effect on the other latches as their clocking signals remain low.

3

```
10 REM  MIC4807 CONTROL PROGRAM
20 GOSUB 3000
30 REM A=1,B=2,C=4,DATA=8,CS=16,CLR=32
100 A$=INKEY$:IF A$="" THEN GOTO 100 ELSE
    LET A=ASC(A$)-49
110 IF A=-36 THEN GOSUB 3000
120 IF A=14 THEN GOSUB 2000
130 IF A<0 OR A>7 THEN GOTO 100
1000 D(A)=8-D(A)+2*A+96:REM TOGGLE OUTPUT
1010 GOSUB 4000
1020 GOTO 100
2000 REM "?" TURNS ON ALL OUTPUTS FOR TEST
2010 FOR A=0 TO 7
2020 OUT 8,A+56:OUT 8,A+40:OUT 8,A+56
2030 NEXT A
2040 IF INKEY$="" THEN GOTO 2040
2050 FOR A=0 TO 7:GOSUB 4000:NEXT A
2060 RETURN
3000 REM  CLEAR DISPLAY AND MEMORY
3010 OUT 8,16:OUT 8,48
3020 FOR A=0 TO 7:D(A)=A+48:NEXT A
3030 RETURN
4000 REM  COMMUNICATIONS DRIVER
4010 OUT 8,D(A):OUT 8,D(A)-16:OUT 8,D(A)
4020 RETURN
9999 END
```

Figure 4. MIC4807 Control Program Listing

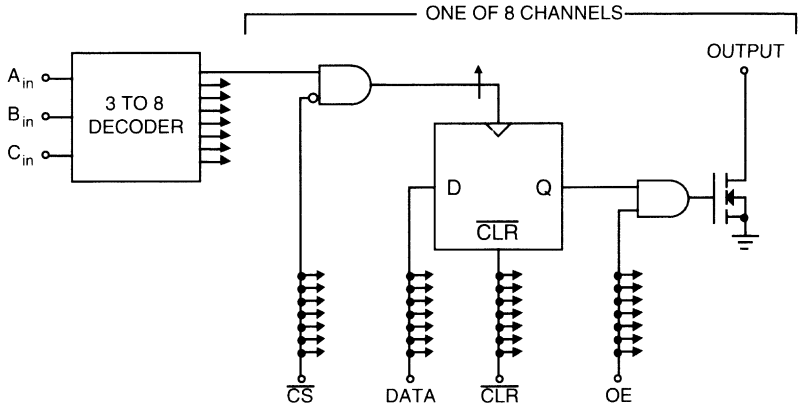


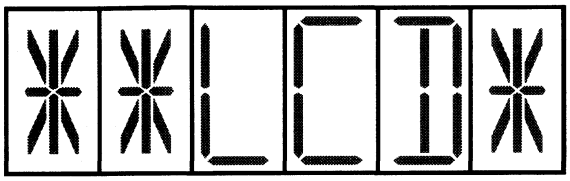
Figure 5. Block Diagram of Logic Circuitry

SECTION 4: DISPLAY DRIVERS

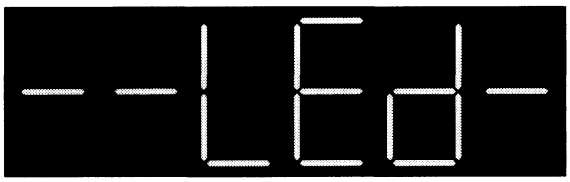
Display Driver Selection Guide

If your product's display is:

Consider:



MIC8010
MIC8011
MIC8012
MIC8013
MIC8014
MIC8030
MIC8031



MIC4350
MIC4807
MIC5002
MIC5005
MIC5007
MIC50395
MIC50396
MIC50397
MIC50398
MIC50399
MM5450
MM5451

Vacuum Fluorescent

MIC4807
MIC8010
MIC8012
MIC8013
MIC10937/10957
MIC10938/10939
MIC10939/10942/10943
MIC10951
MIC8014
MIC8030
MIC8031
MIC10955

NUMERICAL
MIC4350
MIC4807
MIC5002
MIC5005
MIC5007
MIC50395
MIC50396
MIC50397
MIC50398
MIC50399
MIC10951

ALPHANUMERIC
MIC8010
MIC8011
MIC8012
MIC8013
MIC8014
MIC8030
MIC8031
MM5450
MM5451
MIC10937/10957
MIC10938/10939
MIC10939/10942/10943
MIC10941/10939
MIC10955

DOT MATRIX
MIC8010
MIC8011
MIC8012
MIC8013
MIC8014
MIC8030
MIC8031
MM5450
MM5451
MIC10938/10939
MIC10939/10942/10943

Display Driver Selection Guide

All Micrel Display Drivers are available in die form. Special package options are available on most display drivers: please contact factory for details.

DEVICE	Number of Segments	Serial Input/Latched Output	Counter	7 Segment Decoder	BCD Output	LED Driver	LCD Driver	Vacuum Fluorescent Driver	Single Supply Capability	Multiple Supply Capability	PACKAGE
MIC4350 Counter/Latch	7	•	•	•		•			•	•	16-pin PDIP
Decoder & Driver	7	•	•	•		•			•	•	16-pin CerDIP
MIC4807 Protected Addres-	8					•		•	•	•	See "Latched Dri-
sable Low Side Driver	8					•		•	•	•	ver" Section.
MIC5002 4 Digit Counter	4x7	•	•	•	•	•			•	•	28-pin DIP
Decoder											
MIC5005 4 Digit Counter	4x7	•	•	•		•			•	•	24-pin PDIP
Decoder											
MIC5007 4 Digit Counter	4x4	•	•		•	•			•	•	16-pin PDIP
Decoder											
MIC50395 6 Decade Counter	6x7	•	•	•	•	•			•		40-pin PDIP
Decoder to 9999.99											
MIC50396 6 Decade Counter	6x7	•	•	•	•	•			•		40-pin PDIP
Decoder to 99:59:59											
MIC50397 6 Decade Counter	6x7	•	•	•	•	•			•		40-pin PDIP
Decoder to 59:59.99											
MIC50398 6 Decade Counter	6x7		•	•		•			•		28-pin PDIP
Decoder											
MIC50399 6 Decade Counter	6x7		•		•	•			•		28-pin PDIP
Decoder											
MIC8010 Dichroic LCD Driver	30	•					•	•	•	•	40-pin PDIP
	30	•					•	•	•	•	40-pin LCC
MIC8011 Dichroic LCD Driver	38	•					•	•	•	•	48-pin PDIP
	38	•					•	•	•	•	52-pin QFP
MIC8012 Dichroic LCD Driver	30	•					•	•	•	•	40-pin PDIP
With Switching Regulator	30	•					•	•	•	•	
MIC8013 Dichroic LCD Driver	30	•					•	•	•	•	40-pin DIP /LCC
MIC8014 Dichroic LCD Driver	32	•					•	•	•	•	44-pin PLCC
	32	•					•	•	•	•	44-pin Cer Quad
MIC8030 50V LCD Driver	32	•					•	•		•	44-pin LCC/PLCC
	38	•					•	•		•	48-pin PDIP
MIC8031 100V LCD Driver	32	•					•	•		•	44-pin LCC/PLCC
	38	•					•	•		•	48-pin PDIP
MM5450 LED Display Driver	34	•				•			•		40-pin PDIP
	34	•				•			•		44-pin PLCC
MM5451 LED Display Driver	35	•				•			•		40-pin PDIP
	35	•				•			•		44-pin PLCC

4

Display Driver Selection Guide

Micrel Intelligent Vacuum Fluorescent Display Controllers
(formerly from Rockwell International)

MIC10937 ..... **Display Controller-Alphanumeric**

MIC10938 ..... **Display Controller-Anode Drive (5x7)**

MIC10939 ..... **Display Controller-Grid Drive**

MIC10941 ..... **Display Controller-Anode Drive (16 segment)**

MIC10942 ..... **Display Controller-Anode Drive**

MIC10943 ..... **Display Controller-Anode Drive**

MIC10951 ..... **Display Controller-Numeric/Bargraph**

MIC10955 ..... **Segmented Display Controller/Driver**

MIC10957 ..... **Display Controller-Alphanumeric**

Ordering Information

Micrel Intelligent Display Controller Driver Configuration

MIC 109 *ww x y - zz*

MIC = Micrel

Configuration (*ww*)

Package (*x*):		P =	Plastic DIP
		J =	44 Pin PLCC
Temperature (*y*):	Commercial	(no letter)	0°C to +70°C
	Extended	E =	–40°C to +85°C
Voltage Drive (*zz*):		40 =	40V
		50 =	50V

Typical applications require one or more MIC10939 with each MIC10938, MIC10941, or MIC10942/10943 set.

For full datasheets, please call Micrel Semiconductor, (408) 944-0800.

MIC4350

CMOS Counter/Latch Decoder/Driver

Summary Information*

General Description

The MIC4350 is a CMOS device combining the functions of an NBCD counter, four-bit latch, and a seven-segment decoder/driver. It provides up to 25 mA drive/segment capability for displays which require current sinking in the active mode. A lamp blanking input is provided for intensity modulation. A lamp test feature is also available. Synchronous or asynchronous operation is available when the high driving serial output is used in conjunction with the Enable input and some external gating. Automatic suppression of leading zeros in the display is provided by the counter Reset.

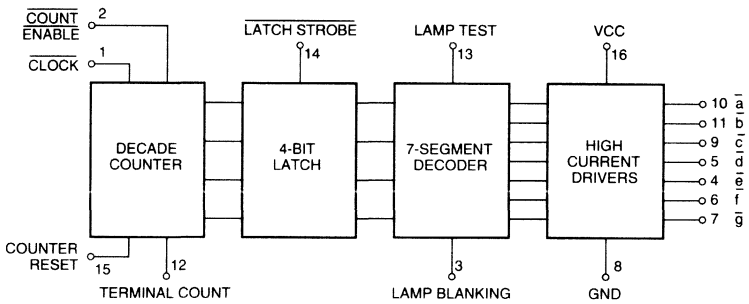
Features

- CMOS version of TTL equivalent MC4350L, 4350P
- 25 mA driver/segment for current sinking
- Synchronous or asynchronous operation
- Lamp blanking for intensity modulation
- Leading zero suppression

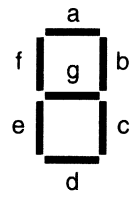
Applications

- Incandescent lamp drivers
- Panel displays
- Modulated intensity functions

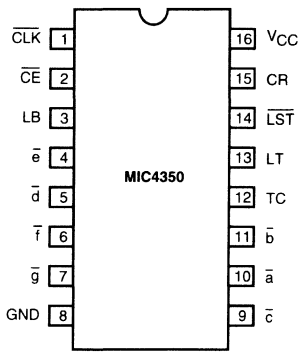
Functional Diagram



Segment Identification



Pin Configuration



Ordering Information*

Part Number	Temperature Range	Package
MIC4350AJ	–55°C to +125°C	16-pin Ceramic DIP
MIC4350CN	0°C to +70°C	16-pin Plastic DIP

* Contact Micrel for more information.

MIC5002CN/5005CN/5007CN

4-Digit Counter/Display Decoder

Summary Information*

General Description

The MIC5002/5/7 is an ion-implanted, P-channel MOS, four-decade synchronous counter with latches, multiplexing circuits, and a read-only memory programmed for seven-segment outputs and BCD outputs. In addition, many on-chip control circuits provide flexibility of use with a minimum of external components.

The MIC5002/5/7 provides a means of counting up to 9999, transferring the count into latches without interrupting the counting operation, and supplying the latched information to the outputs one decade at a time. Scanning is controlled by the SCAN input which increments a one-of-four counter on its negative edge, thereby scanning the latches from MSD (Most Significant Digit) to LSD (Least Significant Digit).

Low-threshold voltages for input DTL/TTL compatibility are achieved through an ion-implementation process. Enhancement mode devices, as well as depletion-mode devices, are fabricated on the chip, allowing it to operate from a single +5V power supply. Depletion-mode technology also allows the entire circuit to operate on less than 25mW of power.

The block diagram, Figure 1, shows all options available on the MIC5002 MOS/LSI. Other members of this family which

Features

- Single-supply operation or double-supply for higher output drive
- Multiplexed seven-segment and/or BCD outputs
- TTL-compatible inputs
- Four decades of synchronous counting
- Minimum external component count
- Low power consumption

Ordering Information

Part Number	Temperature Range	Package
MIC5002CN	0°C to +70°C	28-Pin Plastic DIP
MIC5005CN	0°C to +70°C	24-Pin Plastic DIP
MIC5007CN	0°C to +70°C	16-Pin Plastic DIP

Functional Diagram

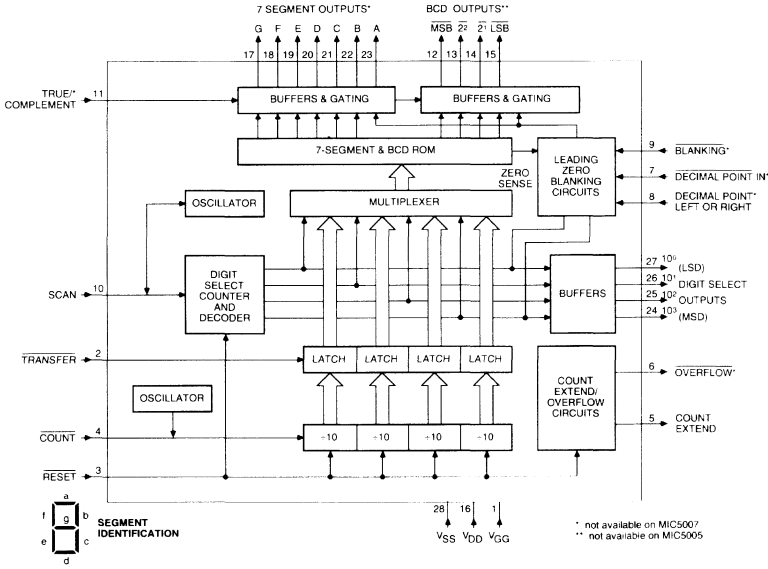


Figure 1

* Contact Micrel for more information.

MIC50395/50396/50397

Six Decade Counter / Display Decoder

General Description

The MIC50395 is an ion-implanted, P-channel MOS six-decade synchronous up/down-counter/display driver with compare-register and storage-latches. The counter as well as the register can be loaded digit-by-digit with BCD data. The counter has an asynchronous-clear function.

Scanning is controlled by the scan oscillator input which is self-oscillating or can be driven by an external signal. The six-decade register is constantly compared to the state of the six-decade counter and when both the register and the counter have the same content, an EQUAL signal is generated. The contents of the counter can be transferred into the 6-digit latch which is then multiplexed from MSD to LSD in BCD and 7-segment format to the output. The seven-segment decoder incorporates a leading-zero blanking circuit which can be disabled by an external signal. This device is intended to interface directly with the standard CMOS logic families.

The MIC50396 and MIC50397 operate identically to the MIC50395 except that two digits in each were reprogrammed to provide divide by six circuitry instead of divide by ten. The MIC50396 is well suited for industrial timer applications while the MIC50397 is best suited for stop watch or real time computer clock applications.

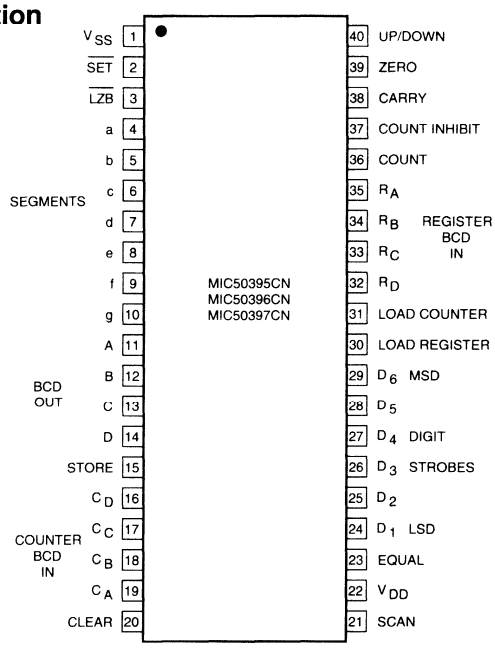
Features

- Single power supply
- Schmitt-Trigger on the count-input
- Drives common anode or cathode displays (CA with buffer)
- Six decades of synchronous up/down counting
- Look-ahead carry or borrow
- Loadable counter
- Loadable compare-register with comparator output
- Multiplexed BCD and seven-segment outputs
- Internal scan oscillator
- Direct LED segment drive
- Interfaces directly with CMOS logic
- Leading zero blanking
- MIC50396 programmed to count time:
  - 99 hrs. 59 min. 59 sec.
- MIC50397 programmed to count time:
  - 59 hrs. 59 min. 99/100 min.

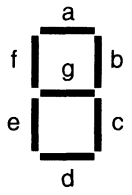
Ordering Information

Part Number	Temp. Range	Package
MIC50395CN	0°C to 70°C	40-pin Plastic DIP
MIC50396CN	0°C to 70°C	40-pin Plastic DIP
MIC50397CN	0°C to 70°C	40-pin Plastic DIP

Pin Connection



Segment Identification



Operations:

Six Decade Counter, Latch

The six decade counter is synchronously incremented or decremented on the positive edge of the count input signal. A Schmitt trigger on this input provides hysteresis for protection against both a noisy environment and double triggering due to a slow rising edge at the count input.

The count inhibit can be changed in coincidence with the positive transition of the count input; the count input is inhibited when the count inhibit is high.

The counter will increment when up/down input is high (V_{SS}) and will decrement when up/down input is low. The up/down input can be changed 0.75 µs prior to the positive transition of the count input.

The clear input is asynchronous and will reset all decades to zero when brought high but does not affect the six digit latch or the scan counter.

As long as store input is low, data is continuously transferred from the counter to the display. Data in the counter will be latched and displayed when store input is high. Store can be changed in coincidence with the positive transition of the count input.

The counter is loaded digit by digit corresponding to the digit strobe outputs. BCD thumb wheel switches with four diodes per decade connected between the digit strobe outputs and the BCD inputs is one method to supply BCD data for loading the counter decades.

The load counter pulse must be at V_{SS} 2 µs prior to the positive transition of the digit strobe of the digit to be loaded. The load counter pulse may be removed after the positive transition of the digit strobe since the chip internally latches this signal. The BCD data to be loaded must be valid through the negative transition of the digit strobe.

Inputs, Outputs

The seven segment outputs are open drain capable of sourcing 10mA average current per segment over one digit cycle. Segments are on when at V_{SS}. The Carry, Equal, Zero, BCD and digit strobe outputs are push pull and are on when at V_{SS}. All inputs except Counter BCD, Register BCD, and SCAN inputs are high impedance CMOS compatible.

Three basic outputs originate from the counter: zero output, equal output, and carry output. Each output goes high on the positive (V_{SS}) going edge of the count input under the following conditions:

Zero output goes high for one count period when all decades contain zero. During a load counter operation the zero output is inhibited.

Equal output goes high for one count period when the contents of the counter and compare register are equal. The equal output is inhibited by a load counter or load register operation, which lasts until the next interdigit blanking period following a negative transition of Load Counter or Load Register.

The carry output goes high with the leading edge of the count input at the count of 000000 when counting up or at 999999* when counting down and goes low with the negative going edge of the same count input.

A count frequency of 1 MHz can be achieved if the equal output, zero output and carry output are not used. These outputs do not respond at this frequency due to their output delay illustrated on the timing diagram.

Six Decade Compare Register

The register is loaded identically to the load counter paragraph described previously. The register may be loaded independently of the counter, however, the clear input will not remove the register contents. Contents of the register are not displayed by the BCD or seven segment outputs.

BCD Seven Segment Outputs

BCD or seven segment outputs are available. Digit strobes are decoded internally by a divide by six Johnson counter. This counter scans from MSD to LSD. By bringing the $\overline{SET}$ input low, this counter will be forced to the MSD decade count. During this time the segment outputs are blanked to protect against display burn out.

BCD outputs are valid for MSD when $\overline{SET}$ is low. Applying V_{SS} to $\overline{SET}$ allows normal scan to resume. Digit 6 output is active (V_{SS}) until the next scan clock pulse brings up digit 5 output.

The segment outputs and digit strobes are blanked during the interdigit blanking time. Leading zero blanking affects only the segment outputs. This option is disabled by bringing the $\overline{LZB}$ input high. Typically the interdigit blanking time is 5 to 25 µs when using the internal scan oscillator.

BCD output data changes at the beginning of the interdigit blanking time. Therefore the BCD output data is valid when the positive transition of a digit output occurs.

Scan Oscillator

The MIC50395 has an internal scan oscillator. The frequency of the scan oscillator is determined by an external capacitor between V_{SS} or V_{DD} and scan input. The wave form present on the scan oscillator input is triangular in the self oscillate mode.

An external oscillator may also be used to drive the scan input. In either case, external capacitors of 150pF each will be required from V_{SS} to Counter BCD inputs and register BCD inputs. This will allow asynchronous loading of the BCD inputs.

In the internal drive mode the interdigit blanking time will be the sum of the negative dwell period of the external oscillator and the normal self oscillate blanking time. (5→25 µs). Display brightness can be controlled by the duty cycle of the external scan oscillator.

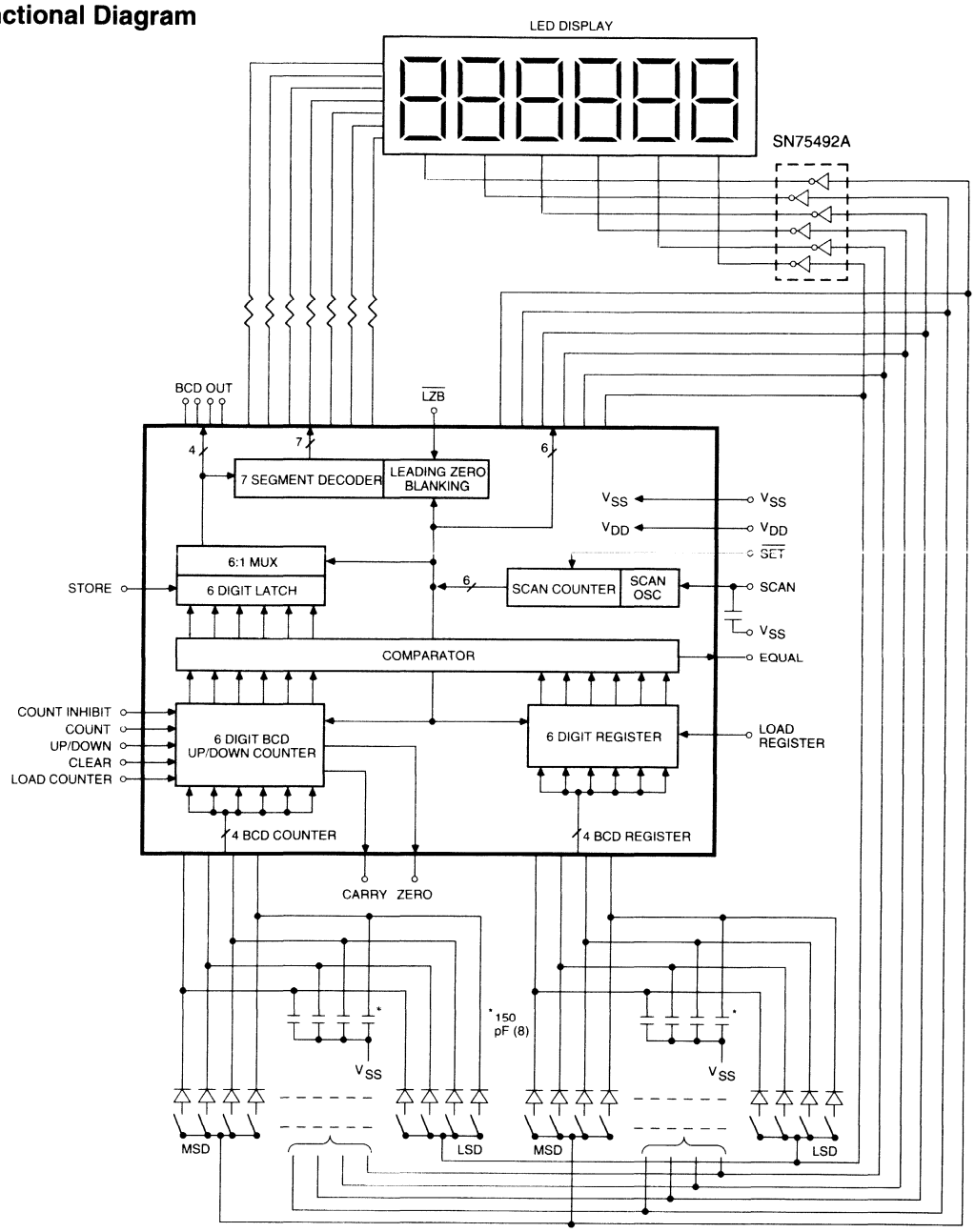
*Carry occurs at 99:59:59 for the 50396 and 59:59:99 for the 50397

If external capacitors on the BCD inputs are undesirable, it will be necessary to synchronize the negative going edge of the load register and/or load counter command to coincide with the positive going edge of the scan input signal. Also the V_{SS} range should be limited from 10.8 to 13.2 Volts.

Typically, the scan oscillator will oscillate at the following frequencies with these nominal capacitor values from V_{SS} to scan input.

C_{IN}	Min	Max
820 pF	1.4 kHz	4.8 kHz
470 pF	2.0 kHz	6.8 kHz
120 pF	7.0 kHz	20 kHz

Functional Diagram



Absolute Maximum Ratings

Voltage on Any Terminal Relative to V_{SS} +0.3V to –20V
Operating Temperature Range (Ambient) 0°C to +70°C
Storage Temperature Range (Ambient) –40°C to +100°C

Maximum Operating Conditions

Symbol	Parameter	Min	Max	Units	Notes
T_A	Operating Temperature	0	70	C	
V_{SS}	Supply voltage (V_{DD} = 0V)	10	15	V	1
I_{SS}	Supply Current		35	mA	2
B_V	Break Down Voltage (Segment only @ 10 µA)		V_{SS} – 26	V	
P_D	Power Dissipation		670	mW	3

Electrical Characteristics

(V_{DD} = 0V, V_{SS} = +10.0V to +15.0, 0°C ≤ T_A ≤ 70°C)

Static Operating Conditions

Symbol	Parameter	Min	Max	Units	Notes
V_{IL}	Input Low Voltage, "0"	V_{DD}	0.2 V_{SS}	V	
V_{IH}	Input High Voltage, "1"	V_{SS} – 1	V_{SS}	V	4
V_{OL}	Output Voltage "0" @ 30 µA		0.2 V_{SS}	V	5
V_{OH}	Output Voltage "1" @ 1.5 mA	0.8 V_{SS}		V	5
I_{OH}	Output Current "1" Digit strobes Segment outputs	 3.0 10.0		 mA mA	 6 7
I_{SCAN}	Scan Input Pullup Current @ 0 V		5.5	mA	
I_{SCAN}	Scan Input Pulldown Current @ 15 V	2	40	µA	
$I_{\overline{SET}}$	$\overline{SET}$ Input Pullup Current @ 0V	5	60	µA	

Note 1: With 150 pF capacitor to V_{SS} from counter BCD and register BCD inputs.

Note 2: I_{SS} with inputs and outputs open at 0°C. 33 mA at 25°C and 28 mA at 70°C. This does not include segment current. Total power per segment must be limited not to exceed power dissipation of package. (θ_{JA} = 100 C/Watt)

Note 3: All outputs loaded.

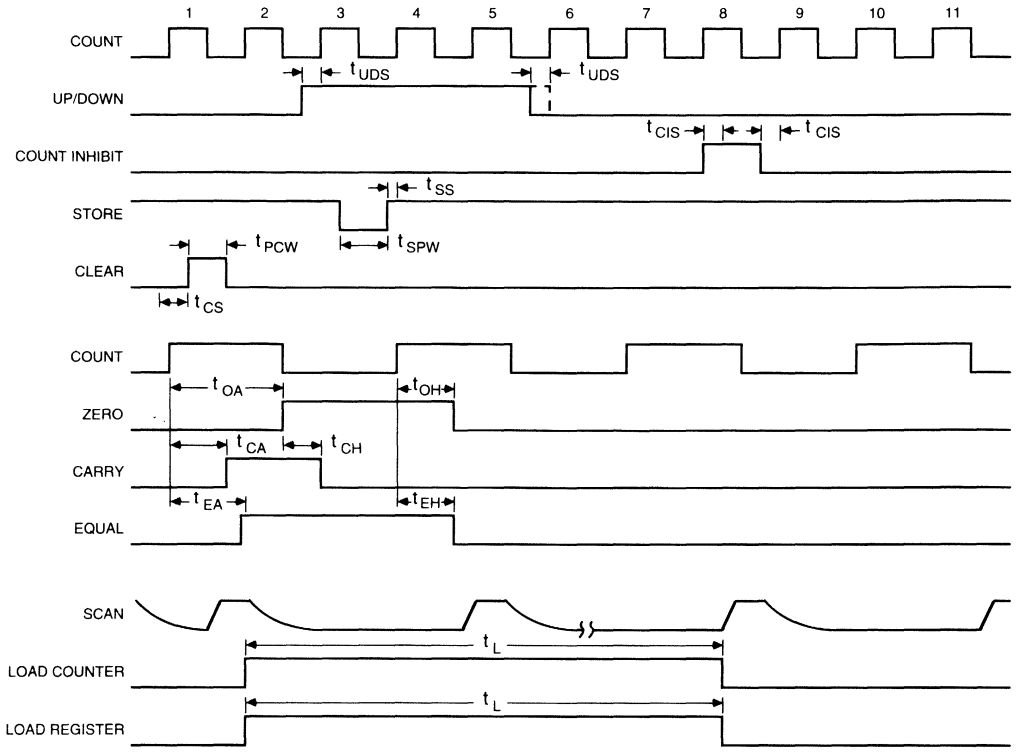
Note 4: MIN V_{IH} from R_A R_B R_C R_D C_A C_B C_C C_D inputs is V_{SS} – 2.5 V. Those inputs have internal pulldown resistors to V_{DD}.

Note 5: This applied to the push pull CMOS compatible outputs. Does not include digit strobes or segment outputs.

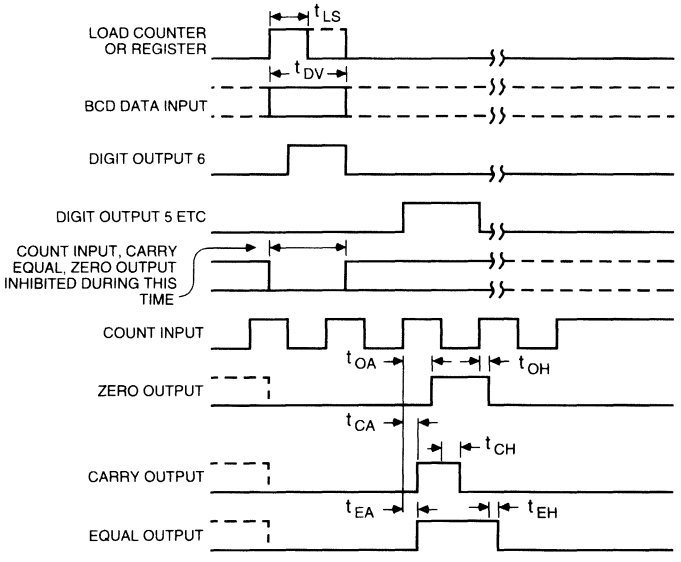
Note 6: For V_{OUT} = V_{SS} – 2.0 Volts. Average value over one digit cycle.

Note 7: For V_{OUT} = V_{SS} – 3.0 Volts. Average value over one digit cycle.

Timing



Loading Counter, Register (1 Digit)



t_{LS} 2.0 µs min NOTE: REF. TO POSITIVE TRANSITION OF DIGIT OUTPUT

t_{DV} 2.0 µs min NOTE: REF. TO NEGATIVE EDGE OF DIGIT OUTPUT

NOTE:
The inhibit function of the zero or equal outputs does not end when the Load Counter input goes to a "0" unless that transition occurs during interdigit blanking period at least 2.0 µs prior to a positive transition of a digit output. This same timing restriction holds for Equal and Load Register.

Dynamic Operating Conditions

Symbol	Parameter	Min	Max	Units	Notes
f_{CI}	Count Input Frequency	0	1.00	MHz	8,9
f_{SI}	Scan Input Frequency	0	20	kHz	
t_{CPW}	Count Pulse Width	400		ns	10
t_{SPW}	Store Pulse Width	2.0		µs	
t_{SS}	Store Setup Time	0		µs	11
t_{CIS}	Count Inhibit Setup Time	0		µs	11
t_{UDS}	Up/Down Setup Time	–0.75		µs	11
t_{CPW}	Clear Pulse Width	2.0		µs	11
t_{CS}	Clear Setup Time	–0.5		µs	11
t_{OA}	Zero Access Time		3.0	µs	11
t_{OH}	Zero Hold Time		1.5	µs	11
t_{CA}	Carry Access Time		1.5	µs	11
t_{CH}	Carry Hold Time	0.9		µs	12
t_{EA}	Equal Access Time	2.0		µs	11
t_{EH}	Equal Hold Time	1.5		µs	11
t_L	Load Time	$1/6\ f_{SI}$			

Note 8: Measured at 50% duty cycle.

Note 9: If carry, equal, or zero outputs are used, the count frequency will be limited by their respective output times.

Note 10: The count pulse width must be greater than the carry access time when using the carry output.

Note 11: The positive edge of the count input is the t = 0 reference.

Note 12: Measured from negative edge of count input.

MIC50398/MIC50399

Six Decade Counter / Display Decoder

General Description

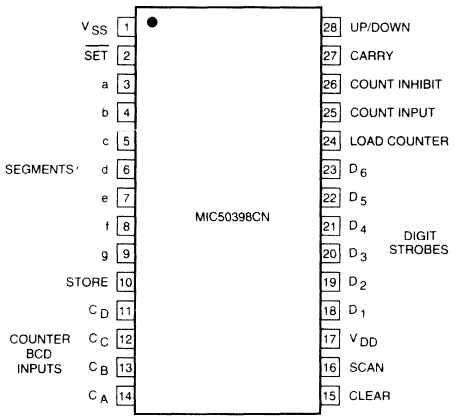
The MIC50398/9 is an ion-implanted, P-channel MOS six-decade synchronous up/down-counter/display driver with storage latches. The counter can be loaded digit-by-digit with BCD data. The counter has an asynchronous-clear function.

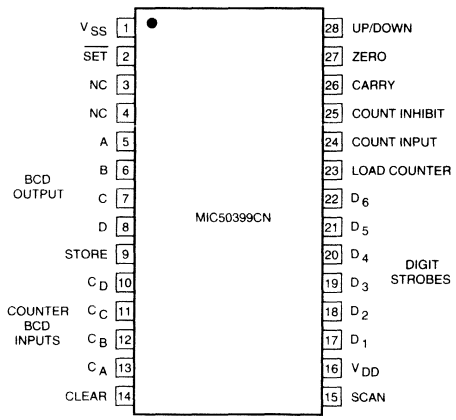
Scanning is controlled by the scan oscillator input which is self-oscillating or can be driven by an external signal. The contents of the counter can be transferred into the 6-digit latch which is then multiplexed from MSD to LSD in BCD or 7-segment format to the output. These devices are intended to interface directly with the standard CMOS logic families.

Features

- Single power supply
- Schmitt-Trigger on the count-input
- Six decades of synchronous up/down counting
- Look-ahead carry or borrow
- Loadable counter
- Multiplexed seven-segment outputs MIC50398N
- Multiplexed BCD outputs, MIC50399N
- Internal scan oscillator

Pin Connection

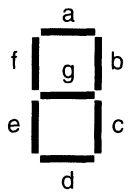




Ordering Information

Part Number	Temp. Range	Package
MIC50398CN	0°C to 70°C	28-pin Plastic DIP
MIC50399CN	0°C to 70°C	28-pin Plastic DIP

Segment Identification



Operations:

Six Decade Counter, Latch

The six decade counter is synchronously incremented or decremented on the positive edge of the count input signal. A Schmitt trigger on this input provides hysteresis for protection against both a noisy environment and double triggering due to a slow rising edge at the count input.

The count inhibit can be changed in coincidence with the positive transition of the count input. Count inhibit must remain high while the count input is high to inhibit counting.

The counter will increment when up/down input is high (V_{SS}) and will decrement when up/down input is low. The up/down input can be changed 0.75 µs prior to the positive transition of the count input.

The clear input is asynchronous and will reset all decades to zero when brought high but does not affect the six digit latch or the scan counter.

As long as store input is low, data is continuously transferred from the counter to the display. Data in the counter will be latched and displayed when store input is high. Store can be changed in coincidence with the positive transition of the count input.

The counter is loaded digit by digit corresponding to the digit strobe outputs. BCD thumb wheel switches with four diodes per decade connected between the digit strobe outputs and the BCD inputs is one method to supply BCD data for loading the counter decades.

The load counter pulse must be at V_{SS} 2 µs prior to the positive transition of the digit strobe of the digit to be loaded. The load counter pulse may be removed after the positive transition of the digit strobe since the chip internally latches this signal. The BCD data to be loaded must be valid through the negative transition of the digit strobe.

Inputs, Outputs

The seven segment outputs are open drain capable of sourcing 10mA average current per segment over one digit cycle. Segments are on when at V_{SS}. The Carry, Zero, BCD and digit strobe outputs are push pull and are on when at V_{SS}. All inputs except Counter BCD and SCAN inputs are high impedance CMOS compatible.

Two basic outputs originate from the counter: zero output, and carry output. Each output goes high on the positive (V_{SS}) going edge of the count input under the following conditions:

Zero output goes high for one count period when all decades contain zero. During a load counter operation the zero output is inhibited. Zero output is on the MIC50399 only.

The carry output goes high with the leading edge of the count input at the count of 000000 when counting up or at 999999 when counting down and goes low with the negative going edge of the same count input. During a load counter operation the carry output is inhibited.

A count frequency of 1.5 MHz can be achieved if the zero output and carry output are not used. These outputs do not respond at this frequency due to their output delay illustrated on the timing diagram.

BCD & Seven Segment Outputs

BCD or seven segment outputs are available. Digit strobes are decoded internally by a divide by six Johnson counter. This counter scans from MSD to LSD. By bringing the $\overline{SET}$ input low, this counter will be forced to the MSD decade count. During this time the segment outputs are blanked to protect against display burn out.

BCD outputs are valid for MSD when $\overline{SET}$ is low. Applying V_{SS} to $\overline{SET}$ allows normal scan to resume. Digit 6 output is active (V_{SS}) until the next scan clock pulse brings up digit 5 output.

The segment outputs and digit strobes are blanked during the interdigit blanking time. Typically the interdigit blanking time is 3 to 10 microseconds when using the internal scan oscillator.

BCD output data changes at the beginning of the interdigit blanking time. Therefore the BCD output data is valid when the positive transition of a digit output occurs. BCD outputs are on MIC50399 only.

Scan Oscillator

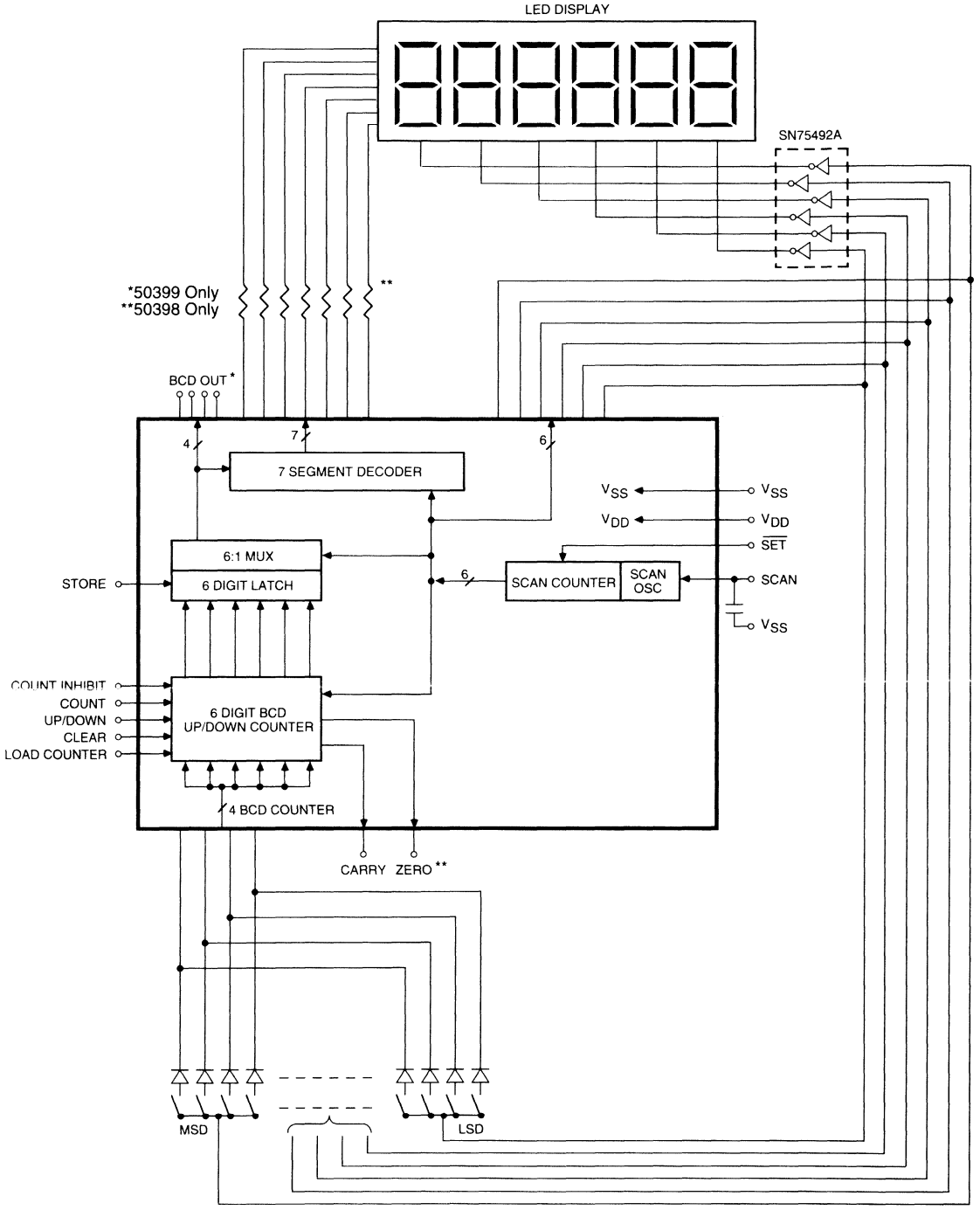
The counters have an internal scan oscillator. The frequency of the scan oscillator is determined by an external capacitor between V_{SS} or V_{DD} and scan input. The wave form present on the scan oscillator input is triangular in the self oscillate mode. An external oscillator may also be used to drive the scan input.

In the external drive mode the interdigit blanking time will be the sum of the negative dwell period of the external oscillator and the normal self oscillate blanking time. (3→10 µs). Display brightness can be controlled by the duty cycle of the external scan oscillator.

Typically, the scan oscillator will oscillate at the following frequencies with these nominal capacitor values from V_{SS} to scan input.

C_{IN}	Min	Max
820 pF	1.4 kHz	4.8 kHz
470 pF	2.0 kHz	6.8 kHz
120 pF	7.0 kHz	20 kHz

Functional Diagram



Absolute Maximum Ratings*

Voltage on Any Terminal Relative to V_{SS} +0.3V to –20V
Operating Temperature Range (Ambient) 0°C to +70°C
Storage Temperature Range (Ambient) –40°C to +100°C

*Operating above absolute maximum ratings may damage the device.

Maximum Operating Conditions

Symbol	Parameter	Min	Max	Units	Notes
T_A	Operating Temperature	0	70	°C	
V_{SS}	Supply voltage (V_{DD} = 0V)	10	15	V	
I_{SS}	Supply Current		40	mA	1
B_V	Break Down Voltage (Segment only @ 10 µA)		V_{SS} – 26	V	MIC50398 only
P_D	Power Dissipation		670	mW	2

Electrical Characteristics

(V_{DD} = 0V, V_{SS} = +10.0V to +15.0, 0°C ≤ T_A ≤ 70°C)

Static Operating Conditions

Symbol	Parameter	Min	Max	Units	Notes
V_{IL}	Input Low Voltage, "0"	V_{DD}	0.2 V_{SS}	V	
V_{IH}	Input High Voltage, "1"	V_{SS} – 1	V_{SS}	V	3
V_{OL}	Output Voltage "0" @ 30 µA		0.2 V_{SS}	V	4
V_{OH}	Output Voltage "1" @ 1.5 mA	0.8 V_{SS}		V	4
I_{OH}	Output Current "1" Digit strobes Segment outputs	 3.0 10.0		 mA mA	 5 6
I_{SCAN}	Scan Input Pullup Current @ 0 V		5.5	mA	
I_{SCAN}	Scan Input Pulldown Current @ 15 V	2	40	µA	
$I_{\overline{SET}}$	$\overline{SET}$ Input Pullup Current @ 0V	5	60	µA	

Note 1: I_{SS} with inputs and outputs open at 0°C. 33 mA at 25°C and 28 mA at 70°C. This does not include segment current. Total power per segment must be limited not to exceed power dissipation of package. (θ_{JA} = 100°C/Watt)

Note 2: All outputs loaded.

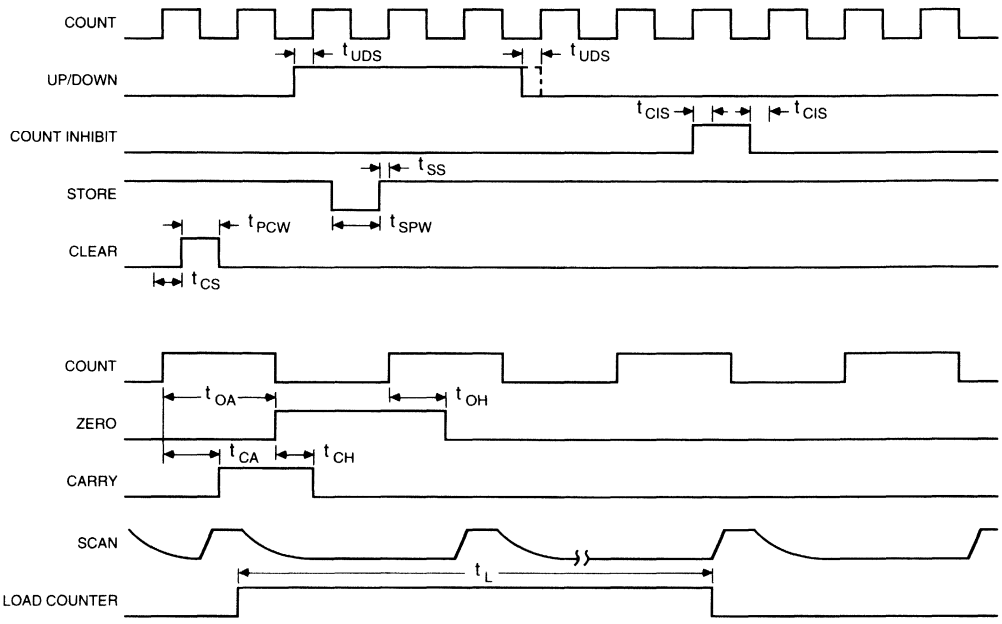
Note 3: MIN V_{IH} from C_A C_B C_C C_D inputs is V_{SS} – 3.5 V. Those inputs have internal pulldown resistors to V_{DD}.

Note 4: This applied to the push pull CMOS compatible outputs. Does not include digit strobes on segment outputs.

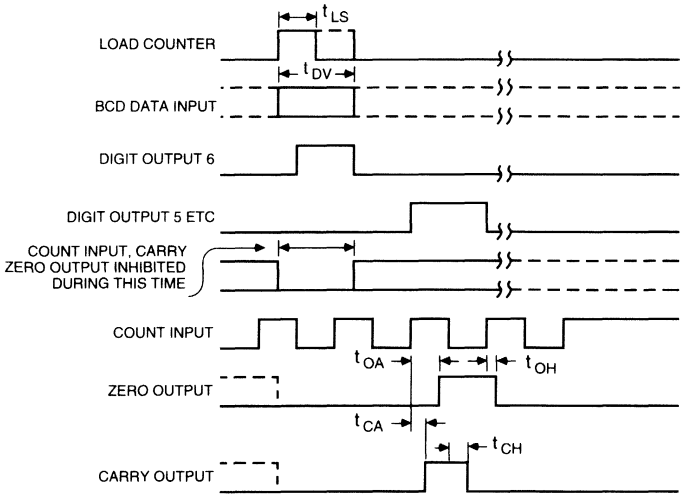
Note 5: For V_{OUT} = V_{SS} – 2.0 Volts. Average value over one digit cycle.

Note 6: For V_{OUT} = V_{SS} – 3.0 Volts. Average value over one digit cycle.

Timing



Loading Counter, Register (1 Digit)



t_{LS} 2.0 µs min NOTE: REF. TO POSITIVE TRANSITION OF DIGIT OUTPUT

t_{DV} 2.0 µS min NOTE: REF. TO NEGATIVE EDGE OF DIGIT OUTPUT

NOTE:
The inhibit function of the zero or carry outputs does not end when the Load Counter input goes to a "0" unless that transition occurs during interdigit blanking period at least 2.0 µs prior to a positive transition of a digit output.

Dynamic Operating Conditions

Symbol	Parameter	Min	Max	Units	Notes
f_{CI}	Count Input Frequency	0	1.5	MHz	7,8
f_{SI}	Scan Input Frequency	0	20	kHz	
t_{CPW}	Count Pulse Width	325		ns	9
t_{SPW}	Store Pulse Width	2.0		µs	
t_{SS}	Store Setup Time	0		µs	10
t_{CIS}	Count Inhibit Setup Time	0		µs	10
t_{UDS}	Up/Down setup Time	–0.75		µs	10
t_{CPW}	Clear Pulse Width	2.0		µs	10
t_{CS}	Clear Setup Time	–0.5		µs	10
t_{OA}	Zero Access Time		3.0	µs	10 MIC50399 only
t_{OH}	Zero Hold Time		1.5	µs	10 MIC50399 only
t_{CA}	Carry Access Time		1.5	µs	10
t_{CH}	Carry Hold Time		0.9	µs	11
t_L	Load Time	1/6 f_{SI}			12

Note 7: Measured at 50% duty cycle.

Note 8: If carry or zero outputs are used, the count frequency will be limited by their respective output times.

Note 9: The count pulse width must be greater than the carry access time when using the carry output.

Note 10: The positive edge of the count input is the t = 0 reference.

Note 11: Measured from negative edge of count input.

Note 12: Time to load one digit.

MIC8010

Liquid Crystal Display Driver

General Description

The MIC8010 driver is designed for use with liquid crystal displays. A serial data interface is used to load an internal register, which in turn controls the segment outputs. A FIFO output allows multiple chips to be cascaded and programmed via a single, serial interface. An on-chip backplane oscillator is included.

In addition to the package options shown, the MIC8010 is available in die form; contact the factory concerning dice and custom packaging requirements

Ordering Information

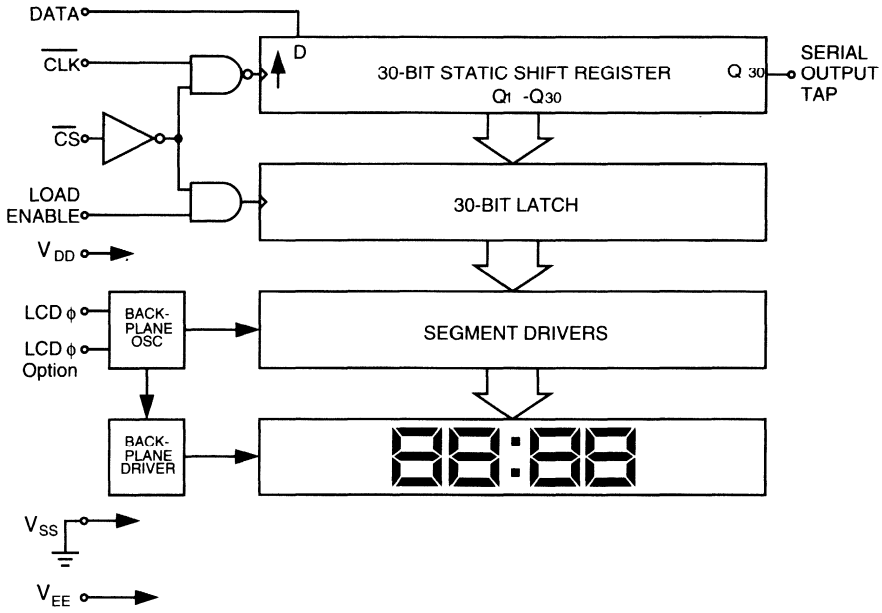
Part Number	Temperature Range	Package
MIC8010-01BN	–40°C to +85°C	40-pin Plastic DIP
MIC8010-02BN	–40°C to +85°C	40-pin Ceramic DIP
MIC8010-01AL	–55°C to +125°C	40-pin Ceramic LCC
MIC8010-02AL	–55°C to +125°C	40-pin Ceramic LCC

Features

- Pin-for-pin compatible with Holt HI8010
- Built using Micrel's proprietary rugged high voltage CMOS process for improved reliability
- Drives 30 segments
- Compatible with dichroic, midchroic, VF or TM displays
- Internal or external backplane oscillator
- 3V to 18V logic supply range
- 5V to 35V output drive swing
- Single or split power supply operation
- Mil spec or extended temperature range part available; contact factory for details
- Cascadable serial interface
- 60V extended output swing available; contact factory for details

4

Block Diagram



Note: The MIC8010 is ESD sensitive.

Absolute Maximum Ratings (Note 1, 2)

Supply Voltage:
- V_{DD} –0.3V to +18V
- V_{EE} V_{DD} – 35V to +0.3V

Input Voltage (except LCDϕ) –0.3V to V_{DD} + 0.3V
LCDϕ Input Voltage V_{DD} – 35V to V_{DD} + 0.3V
DC Current Drain per input pin 10 mA

Operating Temperature Range:
- MIC8010-01BN, -02BN –40°C to +85°C
- MIC8010-01AL, -02AL –55°C to +125°C

Storage Temperature Range –65°C to +150°C
Power Dissipation 250 mW

DC Electrical Characteristics (Notes 3 and 4) V_{DD} = 5V, V_{EE} = –25V, V_{SS} = 0V, T_A = 25°C, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Operating Voltage	V_{DD}		3		18	V
Supply Current	I_{DD}	no load			200	µA
	I_{EE}	no load, f_{BP} = 100Hz			150	µA
Input Low Voltage	V_{IL}		0		1.3	V
(excluding LCDϕ)		–55°C to +125°C, V_{DD} = 4V to 16V			$0.2V_{DD}$	V
Input High Voltage	V_{IH}		2		V_{DD}	V
(excluding LCDϕ)		–55°C to +125°C, V_{DD} = 4V to 16V	$0.5V_{DD}$			V
Input Low Voltage (LCDϕ)	V_{ILX}		V_{EE}		2	V
		–55°C to +125°C, V_{DD} = 4V to 16V			$0.1V_{DD}$	V
Input High Voltage (LCDϕ)	V_{IHX}		2.5		V_{DD}	V
		–55°C to +125°C, V_{DD} = 4V to 16V	$0.9V_{DD}$			V
Input Current	I_{IN}	V_{DD} = 0 to 5V			1	µA
Input Capacitance	C_I	Note 5			5	pF
Segment Output Impedance	R_{SEG}	I_L = 10µA			10	kΩ
Backplane Output Impedance	R_{BP}	I_L = 10µA			450	Ω
Data Out Current	I_{DOT}	Source Current, V_{OH} = 4.5V			0.6	mA
	I_{DOL}	Sink Current, V_{OL} = 0.5V	–0.6			mA

AC Electrical Characteristics (Note 3) V_{EE} = –25V, V_{SS} = 0V, T_A = 25°C, no load, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Clock Period	t_{CL}	V_{DD} = 5V	1000			ns
		V_{DD} = 10V	500			ns
Clock Pulse Width	t_{CW}	V_{DD} = 5V	450			ns
		V_{DD} = 10V	220			ns
Data-In Setup	t_{DS}	V_{DD} = 5V	300			ns
		V_{DD} = 10V	150			ns
Data-In Hold	t_{DH}	V_{DD} = 5V	10			ns
		V_{DD} = 10V	10			ns
Chip Select Setup to Clock	t_{CSS}	V_{DD} = 5V	200			ns
		V_{DD} = 10V	100			ns
Chip Select Hold to Clock	t_{CSH}	V_{DD} = 5V	450			ns
		V_{DD} = 10V	220			ns
Load Setup to Clock	t_{LS}	V_{DD} = 5V	500			ns
		V_{DD} = 10V	280			ns

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Chip Select Setup to Load	t_{CSL}		0			ns
Load Pulse Width	t_{LW}	V_{DD} = 5V	500			ns
		V_{DD} = 10	300			ns
Chip Select Hold to Load	t_{LCS}		0			ns
Data Out Valid from Clock	t_{CDO}	V_{DD} = 5V			600	ns
		V_{DD} = 10V			300	ns

Note 1 **Absolute Maximum Ratings** indicate limits beyond which damage to the device may occur. Electrical specifications do not apply when operating the device beyond its specified **Operating Ratings**.

Note 2 All voltages are referred to V_{SS} = 0V.

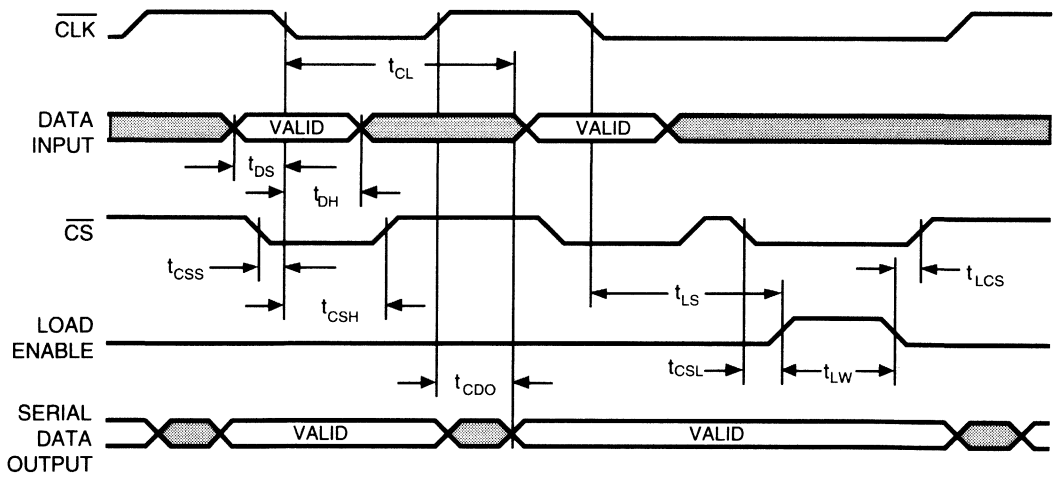
Note 3 **Minimum** and **Maximum** values are 100% tested. **Typical** values represent the most likely parametric norm.

Note 4 $V_{DD} - 32V < V_{EE} - 5V$ is required for proper device operation.

Note 5 Guaranteed by design.

4

Timing Diagram



Applications Information

The MIC8010 utilizes a serial data interface as a means of programming the LCD segment outputs. The interface protocol is compatible with software written for the Holt HI-8010.

An internal shift register is used to load segment data, and a latch is used to transfer this data to the segment drivers. The shift register can be loaded when chip select is held low (V_{SS}). DATA INPUT is shifted in on the falling edges of $\overline{CLOCK}$, and the contents of the shift register exit at SERIAL DATA OUTPUT on the rising edges of $\overline{CLOCK}$. A high level (V_{DD}) at LOAD enables the transfer of data from the shift register to the latch. The latch is transparent while LOAD is held high.

If data is shifted into the internal register but not immediately loaded into the latch, $\overline{CLOCK}$ should remain low. The driver may then be deselected without disturbing the contents of the shift register. If $\overline{CLOCK}$ is held high while $\overline{CHIP\ SELECT}$ is toggled, an extra clock pulse will be generated in the chip, thereby shifting the data.

A data "1" causes the associated segment output to operate 180° out of phase with the backplane output, thus turning the segment on (the segment becomes opaque). If a "0" is loaded, the associated segment will remain off (clear).

Several chips can be cascaded by simply connecting SERIAL DATA OUTPUT from one chip to DATA INPUT of the next. LOAD, $\overline{CLOCK}$, and $\overline{CHIP\ SELECT}$ are each paralleled to allow simultaneous control of all drivers with only 3 lines plus one data line.

Power Supplies

The MIC8010 can operate from a single supply of V_{DD} = 4 to 18V, with V_{EE} and V_{SS} at ground, or from two supplies with V_{DD} for logic voltage and V_{EE} for segment/backplane voltage. V_{EE} is then negative with respect to V_{SS}, and the potential across V_{DD} and V_{EE} must be limited to 35V. If 5V logic levels are used to program the display driver, then V_{DD} should be 5V. The segment and backplane drivers obtain maximum available output swing by switching from V_{EE} to V_{DD}. For higher output voltage swing see the MIC8030 series devices.

Internal Oscillator

The on-chip oscillator (Figure 1) is available in two configurations. Devices with the "-01" suffix feature a 1-pin oscillator (LCDϕ and LCDϕ Option tied together). An external resistor and capacitor set the operating frequency (see Figure 2), and the backplane frequency is $f_{OSC} \div 256$. With R_{OSC} = 150kΩ and C_{OSC} = 470pF, f_{OSC} = 25.6kHz and f_{BP} = 100Hz.

Devices with a "-02" suffix bring out only LCDϕ, leaving LCDϕ Option disconnected. In this case LCDϕ is driven with an external clock; in a typically application several MIC8010-02 drivers would be slaved to a master MIC8010-01 to drive a large display with a common backplane. Figure 2 shows this mode of operation. The input clock signal resets the divider shown in Figure 1 on each cycle so that the backplane operates at the external clock frequency.

The oscillator may be disabled entirely, which allows the segment and backplane outputs to operate in a static, dc manner. The feature is used in driving displays other than LCD displays, such as VF or LED. LCDϕ is connected to V_{DD} for this mode.

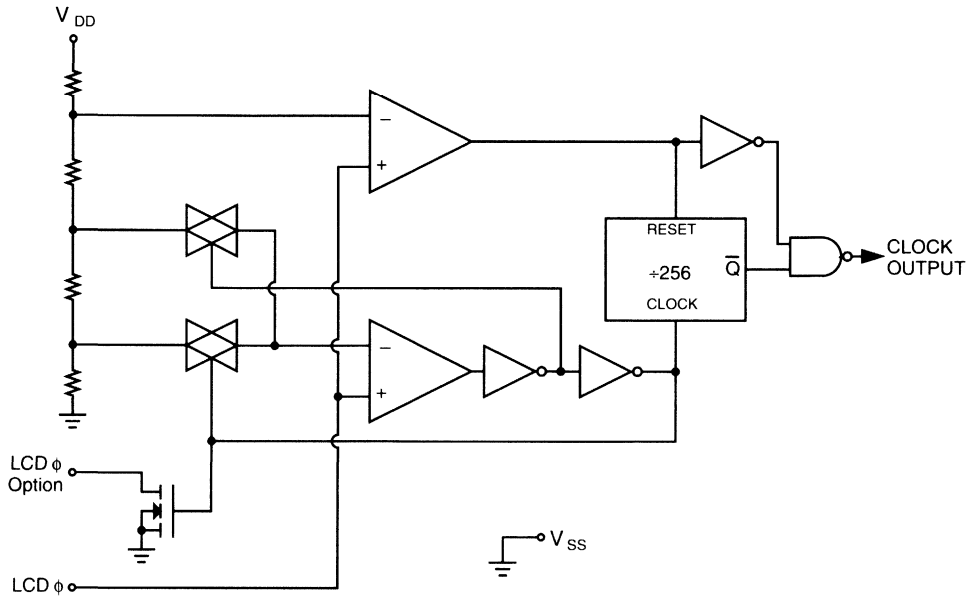


Figure 1. Internal Oscillator Circuit

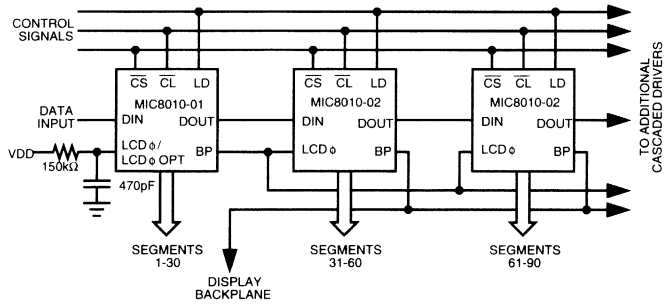


Figure 2. Cascading with Internal Clock Oscillator - 01 Configuration

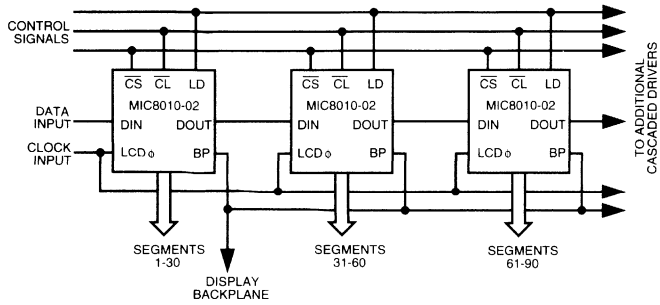


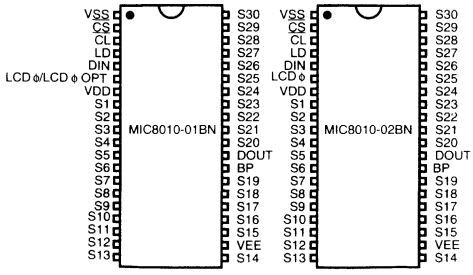
Figure 3. Cascading with External Clocking Source - 02 Configuration

Pin Assignments

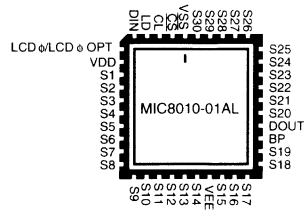
	Device Suffix	
Function	**-01**	**-02**
V_{SS} (Ground)	1	1
Chip Select	2	2
Clock	3	3
Load	4	4
Data Input	5	5
LCDϕ	6	6
LCDϕ Option	6	NC
VDD	7	7
Segment 1	8	8
Segment 2	9	9
Segment 3	10	10
Segment 4	11	11
Segment 5	12	12
Segment 6	13	13
Segment 7	14	14
Segment 8	15	15
Segment 9	16	16
Segment 10	17	17
Segment 11	18	18
Segment 12	19	19
Segment 13	20	20

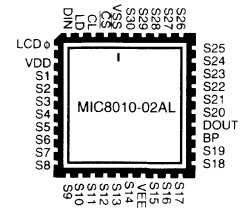
	Device Suffix	
Function	**-01**	**-02**
Segment 14	21	21
V_{EE}	22	22
Segment 15	23	23
Segment 16	24	24
Segment 17	25	25
Segment 18	26	26
Segment 19	27	27
Backplane	28	28
Data Output	29	29
Segment 20	30	30
Segment 21	31	31
Segment 22	32	32
Segment 23	33	33
Segment 24	34	34
Segment 25	35	35
Segment 26	36	36
Segment 27	37	37
Segment 28	38	38
Segment 29	39	39
Segment 30	40	40

Connection Diagrams



40-Pin Plastic DIP





40-Pin Ceramic Chip Carrier

MIC8011

Liquid Crystal Display Driver

General Description

The MIC8011 driver is designed for use with liquid crystal displays. A serial data interface is used to load an internal register, which in turn controls the segment outputs. A FIFO output allows multiple chips to be cascaded and programmed via a single, serial interface. An on-chip backplane oscillator is included.

In addition to the package options shown, the MIC8011 is available in die form; contact the factory concerning dice and custom packaging requirements.

Ordering Information

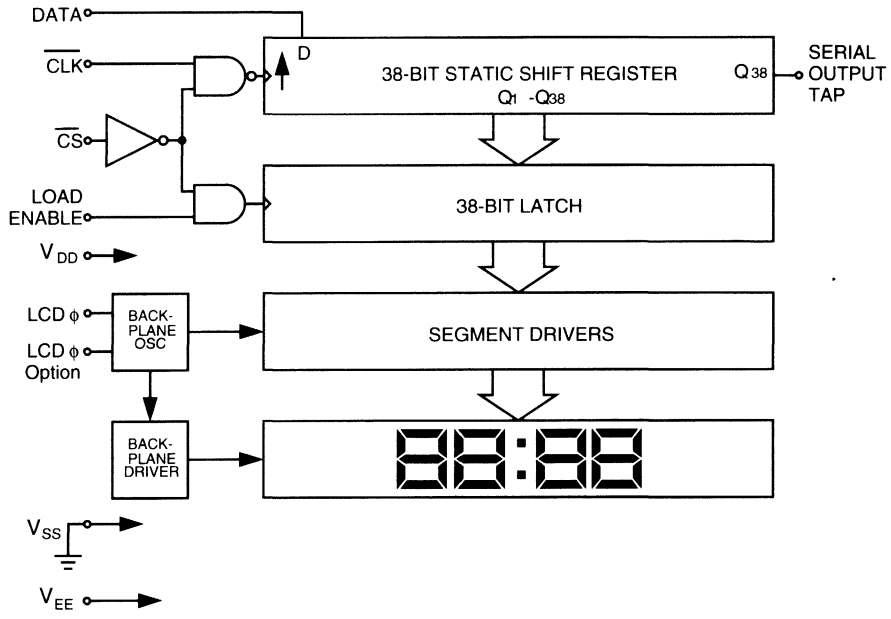
Part Number	Temperature Range	Package
MIC8011-01BN	–40°C to +85°C	48-pin Plastic DIP
MIC8011-02BJ	–40°C to +85°C	48-pin Ceramic DIP
MIC8011-03BQ	–40°C to +85°C	52-pin QFP

Features

- Cascadable serial interface
- Built using Micrel's proprietary rugged high voltage CMOS process for improved reliability
- Drives 38 segments
- Compatible with dichroic, midchroic, VF or TM displays
- Internal or external backplane oscillator
- 3V to 18V logic supply range
- 5V to 35V output drive swing
- Single or split power supply operation
- Mil spec or extended temperature range part available; contact factory for details
- 60V extended output swing available; contact factory for details

4

Block Diagram



Note: The MIC8011 is ESD sensitive.

Absolute Maximum Ratings (Note 1, 2)

Supply Voltage:
- V_{DD} –0.3V to +18V
- V_{EE} V_{DD} – 35V to +0.3V

Input Voltage (except LCDϕ) –0.3V to V_{DD} + 0.3V
LCDϕ Input Voltage V_{DD} – 35V to V_{DD} + 0.3V
DC Current Drain per input pin 10 mA

Operating Temperature Range:
- MIC8011-01BN, -02BN –40°C to +85°C
- MIC8011-01AL, -02AL –55°C to +125°C

Storage Temperature Range –65°C to +150°C
Power Dissipation 250 mW

DC Electrical Characteristics (Notes 3 and 4) V_{DD} = 5V, V_{EE} = –25V, V_{SS} = 0V, T_A = 25°C, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Operating Voltage	V_{DD}		3		18	V
Supply Current	I_{DD}	no load			200	µA
	I_{EE}	no load, f_{BP} = 100Hz			150	µA
Input Low Voltage	V_{IL}		0		1.3	V
(excluding LCDϕ)		–55°C to +125°C, V_{DD} = 4V to 16V			$0.2V_{DD}$	V
Input High Voltage	V_{IH}		2		V_{DD}	V
(excluding LCDϕ)		–55°C to +125°C, V_{DD} = 4V to 16V	$0.5V_{DD}$			V
Input Low Voltage (LCDϕ)	V_{ILX}		V_{EE}		2	V
		–55°C to +125°C, V_{DD} = 4V to 16V			$0.1V_{DD}$	V
Input High Voltage (LCDϕ)	V_{IHX}		2.5		V_{DD}	V
		–55°C to +125°C, V_{DD} = 4V to 16V	$0.9V_{DD}$			V
Input Current	I_{IN}	V_{DD} = 0 to 5V			1	µA
Input Capacitance	C_I	Note 5			5	pF
Segment Output Impedance	R_{SEG}	I_L = 10µA			10	kΩ
Backplane Output Impedance	R_{BP}	I_L = 10µA			450	Ω
Data Out Current	I_{DOT}	Source Current, V_{OH} = 4.5V			0.6	mA
	I_{DOL}	Sink Current, V_{OL} = 0.5V	–0.6			mA

AC Electrical Characteristics (Note 3) Test circuit. V_{EE} = –25V, V_{SS} = 0V, T_A = 25°C, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Clock Period	t_{CL}	V_{DD} = 5V	1000			ns
		V_{DD} = 10V	500			ns
Clock Pulse Width	t_{CW}	V_{DD} = 5V	450			ns
		V_{DD} = 10V	220			ns
Data-In Setup	t_{DS}	V_{DD} = 5V	300			ns
		V_{DD} = 10V	150			ns
Data-In Hold	t_{DH}	V_{DD} = 5V	10			ns
		V_{DD} = 10V	10			ns
Chip Select Setup to Clock	t_{CSS}	V_{DD} = 5V	200			ns
		V_{DD} = 10V	100			ns
Chip Select Hold to Clock	t_{CSH}	V_{DD} = 5V	450			ns
		V_{DD} = 10V	220			ns
Load Setup to Clock	t_{LS}	V_{DD} = 5V	500			ns
		V_{DD} = 10V	280			ns

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Chip Select Setup to Load	t_{CSL}		0			ns
Load Pulse Width	t_{LW}	V_{DD} = 5V	500			nS
		V_{DD} = 10	300			ns
Chip Select Hold to Load	t_{LCS}		0			ns
Data Out Valid from Clock	t_{CDO}	V_{DD} = 5V			600	ns
		V_{DD} = 10V			300	ns

Note 1 **Absolute Maximum Ratings** indicate limits beyond which damage to the device may occur. Electrical specifications do not apply when operating the device beyond its specified **Operating Ratings**.

Note 2 All voltages are referred to V_{SS} = 0V.

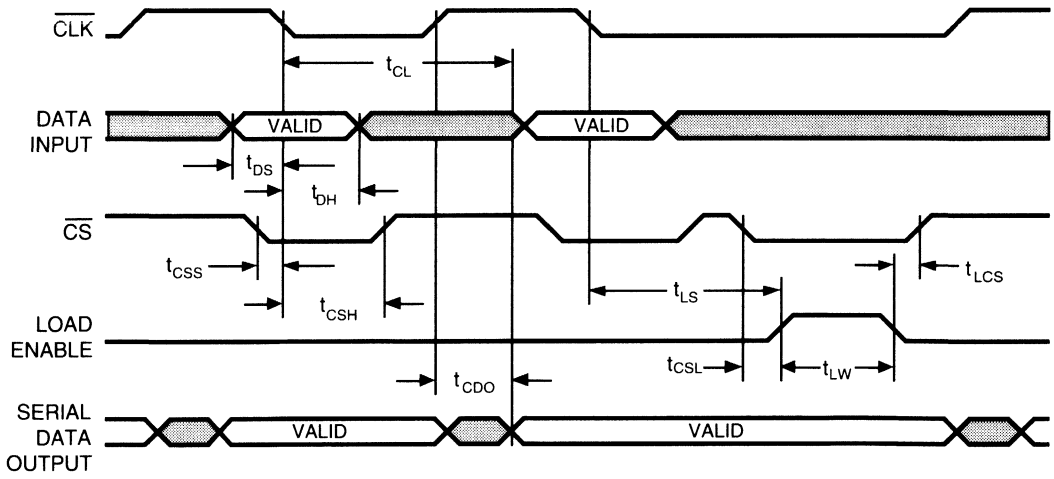
Note 3 **Minimum** and **Maximum** values are 100% tested. **Typical** values represent the most likely parametric norm.

Note 4 $V_{DD} - 32V < V_{EE} - 5V$ is required for proper device operation.

Note 5 Guaranteed by design.

4

Timing Diagram



Applications Information

The MIC8011 utilizes a serial data interface as a means of programming the LCD segment outputs. The interface protocol is compatible with software written for the Holt HI-8010.

An internal shift register is used to load segment data, and a latch is used to transfer this data to the segment drivers. The shift register can be loaded when chip select is held low (V_{SS}). DATA INPUT is shifted in on the falling edges of $\overline{CLOCK}$, and the contents of the shift register exit at SERIAL DATA OUTPUT on the rising edges of $\overline{CLOCK}$. A high level (V_{DD}) at LOAD enables the transfer of data from the shift register to the latch. The latch is transparent while LOAD is held high.

If data is shifted into the internal register but not immediately loaded into the latch, $\overline{CLOCK}$ should remain low. The driver may then be deselected without disturbing the contents of the shift register. If $\overline{CLOCK}$ is held high while $\overline{CHIP\ SELECT}$ is toggled, an extra clock pulse will be generated in the chip, thereby shifting the data.

A data "1" causes the associated segment output to operate 180° out of phase with the backplane output, thus turning the segment on (the segment becomes opaque). If a "0" is loaded, the associated segment will remain off (clear).

Several chips can be cascaded by simply connecting SERIAL DATA OUTPUT from one chip to DATA INPUT of the next. LOAD, $\overline{CLOCK}$, and $\overline{CHIP\ SELECT}$ are each paralleled to allow simultaneous control of all drivers with only 3 lines plus one data line.

Power Supplies

The MIC8011 can operate from a single supply of V_{DD} = 4 to 18V, with V_{EE} and V_{SS} at ground, or from two supplies with V_{DD} for logic voltage and V_{EE} for segment/backplane voltage. V_{EE} is then negative with respect to V_{SS}, and the potential across V_{DD} and V_{EE} must be limited to 35V. If 5V logic levels are used to program the display driver, then V_{DD} should be 5V. The segment and backplane drivers obtain maximum available output swing by switching from V_{EE} to V_{DD}. For higher output voltage swing see the MIC8030 series devices.

Internal Oscillator

The on-chip oscillator (Figure 1) is available in two configurations. Devices with the "-01" suffix feature a 1-pin oscillator (LCDϕ and LCDϕ Option tied together). An external resistor and capacitor set the operating frequency (see Figure 2), and the backplane frequency is $f_{OSC} \div 256$. With R_{OSC} = 150kΩ and C_{OSC} = 470pF, f_{OSC} = 25.6kHz and f_{BP} = 100Hz.

Devices with a "-02" suffix bring out only LCDϕ, leaving LCDϕ Option disconnected. In this case LCDϕ is driven with an external clock; in a typically application several MIC8011-02 drivers would be slaved to a master MIC8011-01 to drive a large display with a common backplane. Figure 2 shows this mode of operation. The input clock signal resets the divider shown in Figure 1 on each cycle so that the backplane operates at the external clock frequency.

Devices with the "-03" suffix have both the LCDϕ and LCDϕ Option available externally, allowing operation in either of the previous two configurations

The oscillator may be disabled entirely, which allows the segment and backplane outputs to operate in a static, dc manner. The feature is used in driving displays other than LCD displays, such as VF or LED. LCDϕ is connected to V_{DD} for this mode.

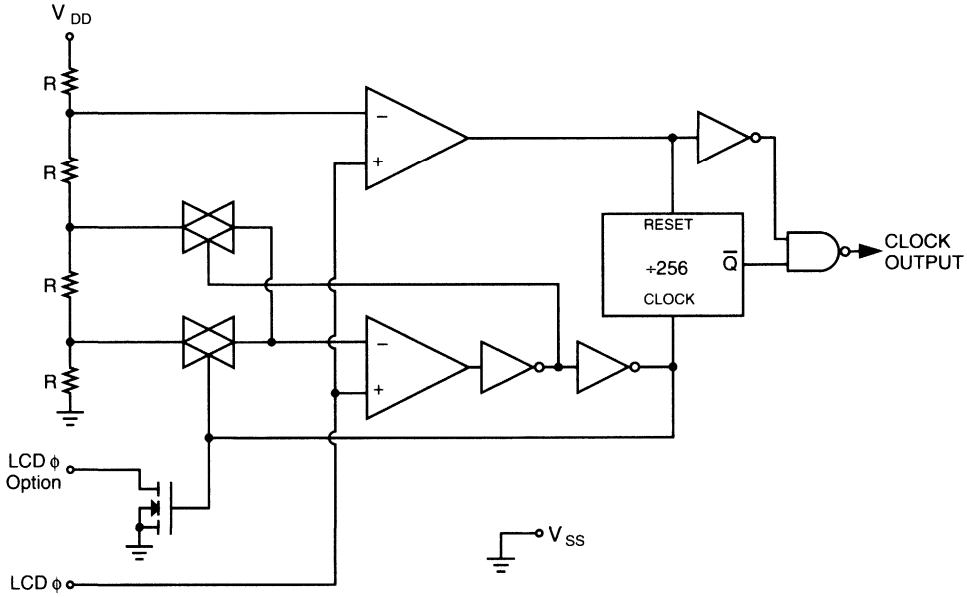


Figure 1. Internal Oscillator Circuit

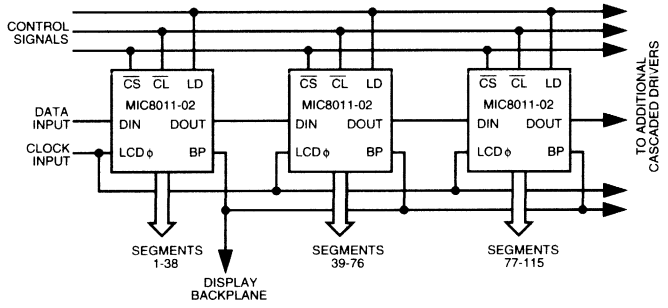


Figure 2. Cascading with External Clocking Source - Option -02

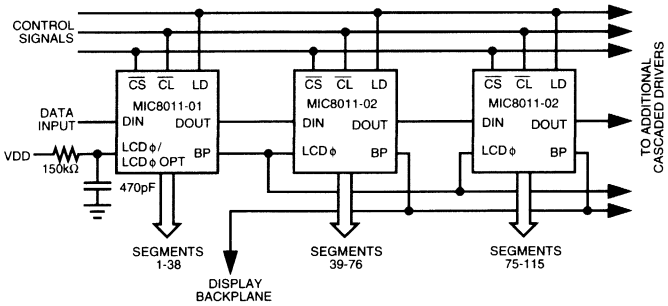


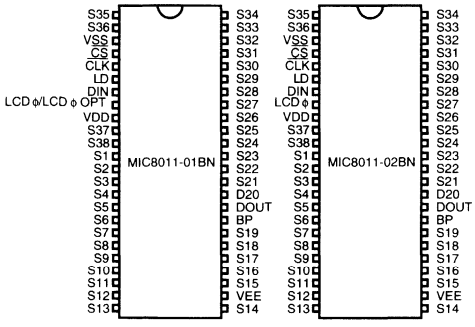
Figure 3. Cascading with Internal Clock Oscillator - Option -01

Pin Assignments

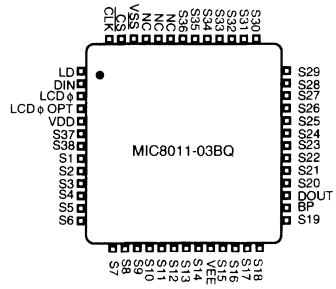
	Device Suffix		
Function	**-01**	**-02**	**-03**
V_{SS}	3	3	50
$\overline{\text{Chip Select}}$	4	4	51
$\overline{\text{Clock}}$	5	5	52
Load	6	6	1
Data Input	7	7	2
LCDϕ	8	8	3
LCDϕ Option	8	NC	4
VDD	9	9	5
Segment 37	10	10	6
Segment 38	11	11	7
Segment 1	12	12	8
Segment 2	13	13	9
Segment 3	14	14	10
Segment 4	15	15	11
Segment 5	16	16	12
Segment 6	17	17	13
Segment 7	18	18	14
Segment 8	19	19	15
Segment 9	20	20	16
Segment 10	21	21	17
Segment 11	22	22	18
Segment 12	23	23	19
Segment 13	24	24	20
Segment 14	25	25	21
V_{EE}	26	26	22

	Device Suffix		
Function	**-01**	**-02**	**-03**
Segment 15	27	27	23
Segment 16	28	28	24
Segment 17	29	29	25
Segment 18	30	30	26
Segment 19	31	31	27
Backplane	32	32	28
Data Output	33	33	29
Segment 20	34	34	30
Segment 21	35	35	31
Segment 22	36	36	32
Segment 23	37	37	33
Segment 24	38	38	34
Segment 25	39	39	35
Segment 26	40	40	36
Segment 27	41	41	37
Segment 28	42	42	38
Segment 29	43	43	39
Segment 30	44	44	40
Segment 31	45	45	41
Segment 32	46	46	42
Segment 33	47	47	43
Segment 34	48	48	44
Segment 35	1	1	45
Segment 36	2	2	46

Connection Diagrams



48-Pin DIPs -01, -02



52-Pin QFP -03

MIC8012

Liquid Crystal Display Driver

General Description

The MIC8012 driver is designed for use with liquid crystal displays. A serial data interface is used to load an internal register, which in turn controls the segment outputs. An on-chip backplane oscillator is included.

A switching regulator is included on-chip to provide a negative supply where only a single, positive supply is available to power the chip.

In addition to the package options shown, the MIC8012 is available in die form; contact factory concerning dice and custom packaging requirements.

Ordering Information

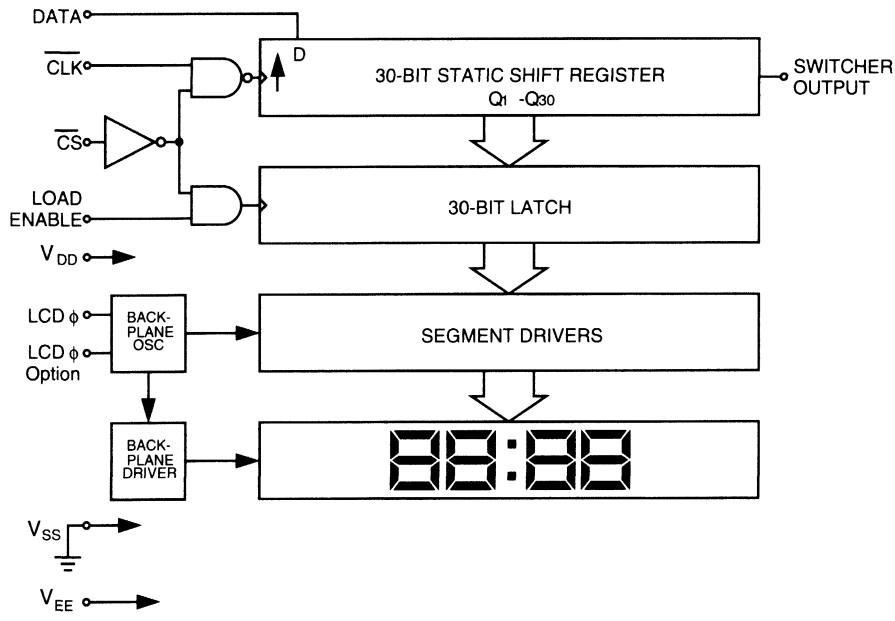
Part Number	Temperature Range	Package
MIC8012-01BN	–40°C to +85°C	40-pin Plastic DIP

Features

- Serial interface
- Drives 30 segments
- Built using Micrel's proprietary rugged high voltage CMOS process for improved reliability
- Compatible with dichroic, midchroic, or TM displays
- Internal backplane oscillator
- 3V to 18V logic supply range
- 5V to 35V output drive swing
- On-chip switching regulator for negative supply voltage
- Mil spec (883C) or extended temperature range part available; contact factory for details
- 60 V extended output swing available; contact factory for details.

4

Block Diagram



Note: The MIC8012 is ESD sensitive.

Absolute Maximum Ratings (Note 1, 2)

Supply Voltage:
- V_{DD} –0.3V to +18V
- V_{EE} V_{DD} – 35V to +0.3V

Input Voltage (except LCDϕ) –0.3V to V_{DD} + 0.3V
LCDϕ Input Voltage V_{DD} – 35V to V_{DD} + 0.3V
DC Current Drain per input pin 10 mA

Operating Temperature Range:
- MIC8012-01BN –40°C to +85°C

Storage Temperature Range –65°C to +150°C
Power Dissipation 250 mW

DC Electrical Characteristics (Notes 3 and 4) V_{DD} = 5V, V_{EE} = –25V, V_{SS} = 0V, T_A = 25°C, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Operating Voltage	V_{DD}		3		18	V
Supply Current	I_{DD}	no load			200	µA
	I_{EE}	no load, f_{BP} = 100Hz			150	µA
Input Low Voltage	V_{IL}		0		1.3	V
(excluding LCDϕ)		–55°C to +125°C, V_{DD} = 4V to 16V			$0.2V_{DD}$	V
Input High Voltage	V_{IH}		2		V_{DD}	V
(excluding LCDϕ)		–55°C to +125°C, V_{DD} = 4V to 16V	$0.5V_{DD}$			V
Input Low Voltage (LCDϕ)	V_{ILX}		V_{EE}		2	V
		–55°C to +125°C, V_{DD} = 4V to 16V			$0.1V_{DD}$	V
Input High Voltage (LCDϕ)	V_{IHX}		2.5		V_{DD}	V
		–55°C to +125°C, V_{DD} = 4V to 16V	$0.9V_{DD}$			V
Input Current	I_{IN}	V_{DD} = 0 to 5V			1	µA
Input Capacitance	C_I	Note 5			5	pF
Segment Output Impedance	R_{SEG}	I_L = 10µA			10	kΩ
Backplane Output Impedance	R_{BP}	I_L = 10µA			450	Ω

AC Electrical Characteristics (Note 3) V_{EE} = –25V, V_{SS} = 0V, T_A = 25°C, no load, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Clock Period	t_{CL}	V_{DD} = 5V	1000			ns
		V_{DD} = 10V	500			ns
Clock Pulse Width	t_{CW}	V_{DD} = 5V	450			ns
		V_{DD} = 10V	220			ns
Data-In Setup	t_{DS}	V_{DD} = 5V	300			ns
		V_{DD} = 10V	150			ns
Data-In Hold	t_{DH}	V_{DD} = 5V	10			ns
		V_{DD} = 10V	10			ns
Chip Select Setup to Clock	t_{CSS}	V_{DD} = 5V	200			ns
		V_{DD} = 10V	100			ns
Chip Select Hold to Clock	t_{CSH}	V_{DD} = 5V	450			ns
		V_{DD} = 10V	220			ns
Load Setup to Clock	t_{LS}	V_{DD} = 5V	500			ns
		V_{DD} = 10V	280			ns

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Chip Select Setup to Load	t_{CSL}		0			ns
Load Pulse Width	t_{LW}	V_{DD} = 5V	500			ns
		V_{DD} = 10	300			ns
Chip Select Hold to Load	t_{LCS}		0			ns
Data Out Valid from Clock	t_{CDO}	V_{DD} = 5V			600	ns
		V_{DD} = 10V			300	ns

Note 1 **Absolute Maximum Ratings** indicate limits beyond which damage to the device may occur. **Electrical Characteristics** do not apply when operating the device beyond its specified **Operating Ratings**.

Note 2 All voltages are referred to V_{SS} = 0V.

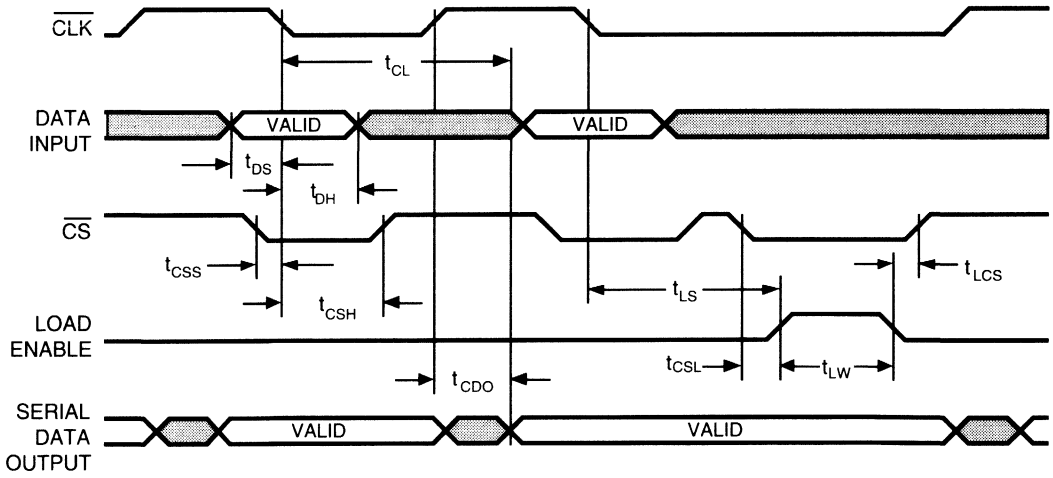
Note 3 **Minimum** and **Maximum** values are 100% tested. **Typical** values represent the most likely parametric norm.

Note 4 $V_{DD} - 32V < V_{EE} - 5V$ is required for proper device operation.

Note 5 Guaranteed by design.

4

Timing Diagram



Applications Information

Power Supplies

The MIC8012 includes a p-channel switch that serves as an inverting buck-boost switching supply to develop V_{EE} (negative supply voltage) where only a positive supply is available (see Figure 1). Although the duty cycle of the p-channel gate drive is approximately 50%, the inductor current is operated in a discontinous mode to obtain an output (V_{EE}) that is greater in magnitude than the input supply (V_{DD}). Regulation is provided by a zener diode. The switching frequency is 1/2 that of the internal backplane oscillator.

Programming

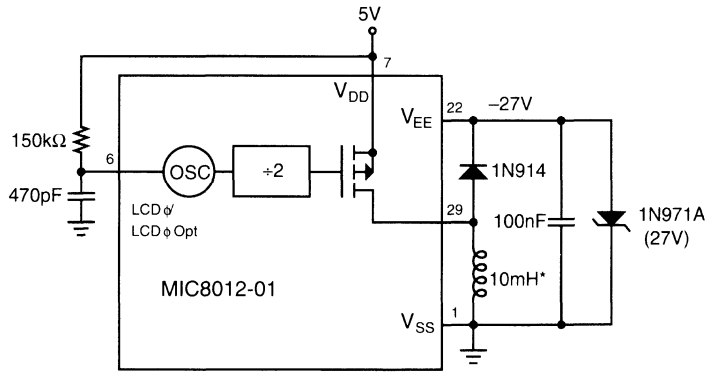
The MIC8012 utilizes an internal shift register as the means of loading segment data, and a latch is used to transfer this data to the segment drivers. The shift register can be loaded when $\overline{\text{CHIP SELECT}}$ is held low (V_{SS}). DATA INPUT is shifted in on the falling edges of $\overline{\text{CLOCK}}$. A high level (V_{DD}) at LOAD enables the transfer of data from the shift register to the latch. The latch is transparent while LOAD is held high.

A data "1" causes the associated segment output to operate 180° out of phase with the backplane output, thus turning the segment on (the segment becomes opaque). If a "0" is loaded, the associated segment will remain off (clear).

Oscillator

The on-chip oscillator (Figure 3) is made available by internally bonding LCDϕ and LCDϕ Option together. An external resistor and capacitor set the operating frequency (see Figure 3), and the backplane frequency is $f_{OSC} \div 256$. With $R_{OSC} = 150k\Omega$ and $C_{OSC} = 470pF$, $f_{OSC} = 25.6kHz$ and $f_{BP} = 100Hz$.

A number of MIC8010-02 and/or MIC8011-02 drivers may be slaved to the MIC8012-01 oscillator by connecting their LCDϕ inputs to the MIC8012-01 backplane output (see Figure 2). In this configuration the "slaved" backplane outputs are tied in parallel and operate at the frequency of LCDϕ. In this application the MIC8012 can generate the negative V_{EE} supply for all of the display drivers.



* 129T, 30 gauge Cu,
wound on Philips (Ferroxcube)
core #2213P-A600-3B7

Figure 1. Switching Supply Connection

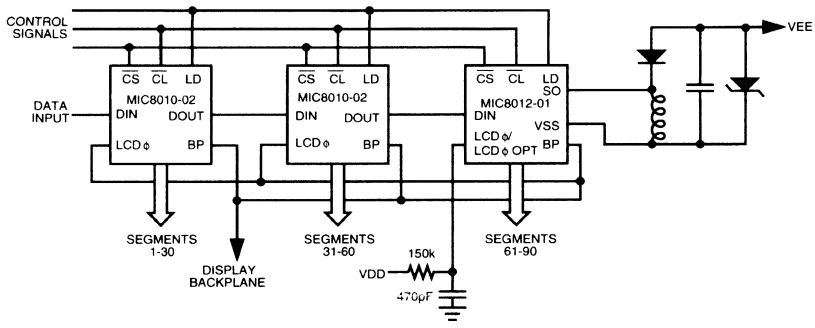


Figure 2. Cascading with MIC8010/12

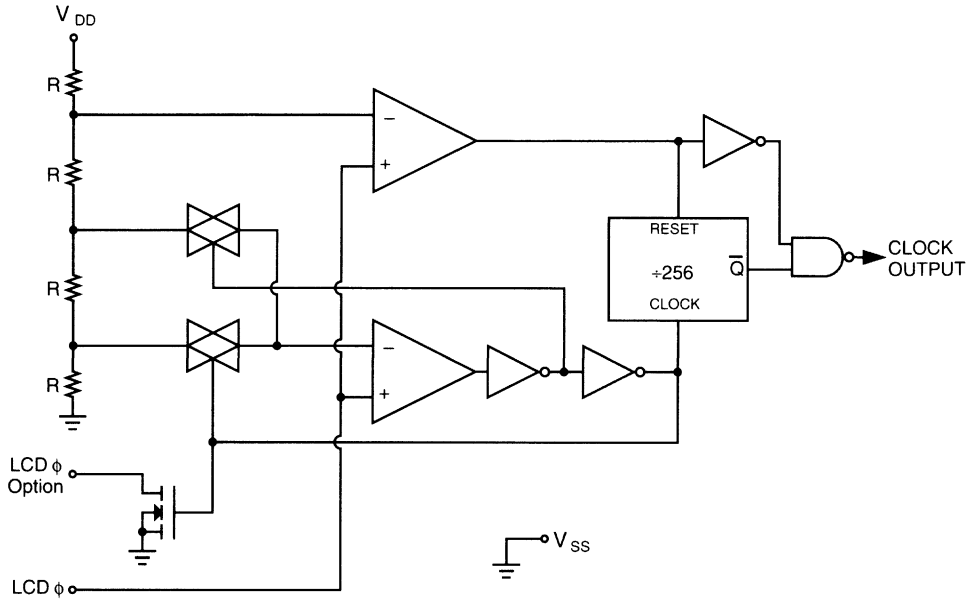


Figure 3. Internal Oscillator Circuit

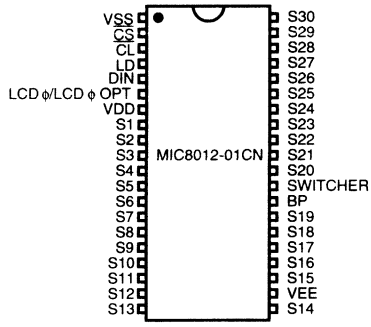
Pin Assignments

Function	Device Suffix -01
V_{SS} (Ground)	1
Chip Select	2
Clock	3
Load	4
Data Input	5
LCDϕ	6
LCDϕ Option	6
V_{DD}	7
Segment 1	8
Segment 2	9
Segment 3	10
Segment 4	11
Segment 5	12
Segment 6	13
Segment 7	14
Segment 8	15
Segment 9	16
Segment 10	17
Segment 11	18
Segment 12	19
Segment 13	20

Function	Device Suffix -01
Segment 14	21
V_{EE}	22
Segment 15	23
Segment 16	24
Segment 17	25
Segment 18	26
Segment 19	27
Backplane	28
Data Output	29
Segment 20	30
Segment 21	31
Segment 22	32
Segment 23	33
Segment 24	34
Segment 25	35
Segment 26	36
Segment 27	37
Segment 28	38
Segment 29	39
Segment 30	40
NC	41,42,43, 44

4

Connection Diagram



40-Pin Plastic DIP

MIC8013

Liquid Crystal Display Driver

General Description

The MIC8013 driver is designed for use with liquid crystal displays. A serial data interface is used to load an internal register, which in turn controls the segment outputs. A FIFO output allows multiple chips to be cascaded and programmed via a single, serial interface. An on-chip backplane oscillator is included.

In addition to the package options shown, the MIC8013 is available in die form; contact the factory concerning dice and custom packaging requirements

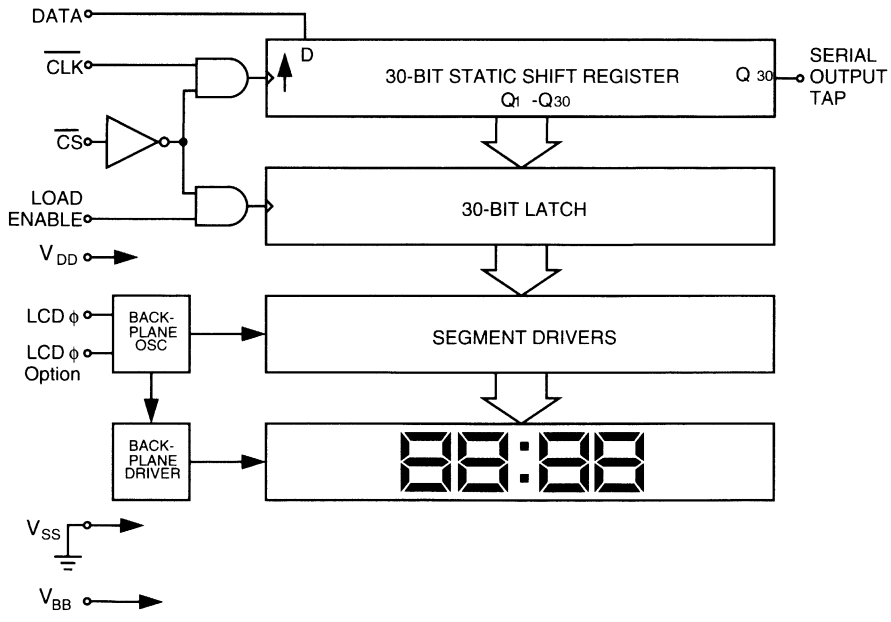
Ordering Information

Part Number	Temperature Range	Package
MIC8013-01BN	–40°C to +85°C	40-pin Plastic DIP
MIC8013-02BN	–40°C to +85°C	40-pin Plastic DIP
MIC8013-01AL	–55°C to +125°C	40-pin Ceramic LCC
MIC8013-02AL	–55°C to +125°C	40-pin Ceramic LCC

Features

- Logic compatible with AMI/Gould S4520
- Drives 30 segments
- Built using Micrel's proprietary rugged high voltage CMOS process for improved reliability
- Compatible with dichroic, midchroic, VF or TM displays
- Internal or external backplane oscillator
- 3V to 18V logic supply range
- 5V to 35V output drive swing
- Single or split power supply operation
- Mil spec or extended temperature range part available; contact factory for details
- Cascadable serial interface
- 60V extended output swing available; contact factory for details

Block Diagram



Note: The MIC8013 is ESD sensitive.

Absolute Maximum Ratings (Note 1, 2)

V_{DD}	−0.3V to +17V	Operating Temperature Range:	
V_{BB}	V_{SS} + 0.3V to V_{DD} − 32V	MIC8013-01BN, -02BN	−40°C to +85°C
Input Voltage (except LCDϕ)	V_{SS} − 0.3V to V_{DD} + 0.3V	MIC8013-01AL, -02AL	−55°C to +125°C
LCDϕ Input Voltage	V_{BB} − 35V to V_{DD} + 0.3V	Storage Temperature Range	−65°C to +150°C
DC Current Drain per input pin	10 mA	Power Dissipation	250 mW

DC Electrical Characteristics (Notes 3 and 4)

$3V \le V_{DD} \le 16V$, $V_{BB} = -25V$, $V_{SS} = 0V$, $-55°C \le T_A \le 125°C$, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Logic Supply Voltage	V_{DD}		3		16	V
Display Supply Voltage	V_{BB}	$V_{BB} \le V_{SS}$	V_{DD}−32		V_{DD}−5	V
Supply Current (external oscillator)	I_{DD}	no load, CMOS input levels			200	µA
Supply Current (internal oscillator)		$V_{DD} \le 5V$			200	µA
		no load, V_{DD} = 16V, CMOS input levels			750	µA
Display Driver Current	I_{BB}	f_{BP} = 100Hz, no load			−200	µA
Input Low Voltage (excluding LCDϕ)	V_{IL}		V_{SS}		0.2V_{DD}	V
Input High Voltage (excluding LCDϕ)	V_{IH}	$V_{DD} \ge 5V$	0.5V_{DD}		V_{DD}	V
Input Low Voltage (LCDϕ)	V_{ILX}	externally driven	V_{BB}		0.1V_{DD}	V
Input High Voltage (LCDϕ)	V_{IHX}	externally driven	0.9V_{DD}		V_{DD}	V
Input Leakage Current	I_L	V_{DD} = 0 to 5V			1	µA
Input Capacitance	C_I				5	pF
DC Bias (Average) Any Segment Output to Backplane	V_{OAVG}	Note 7			±25	mV
Segment Output	C_{LSEG}	Note 8			1000	pF
Backplane Output	C_{LBP}				40,000	pF
Segment Output Impedance	R_{SEG}	I_L = 10µA			10	kΩ
Backplane Output Impedance	R_{BP}	I_L = 10µA			312	Ω
Data Out Output Impedance	R_{DD}				3	kΩ
Data Out Current	I_{DOH}	Source Current, $V_{OH} = V_{DD} - 5V$			0.6	mA
	I_{DOL}	Sink Current, V_{OL} = 0.5V	−0.6			mA

AC Electrical Characteristics (Note 3)

$V_{BB} = -25V$, $V_{SS} = 0V$, $T_A = 25°C$, no load, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Cycle Time	t_{CYC}	V_{DD} = 3V	1000			ns
		V_{DD} = 5V	500			ns
		$V_{DD} \ge 7.5V$	320			ns
Cycle Time (cascaded)	t_{CYC}	V_{DD} = 3V	1300			ns
		V_{DD} = 5V	600			ns
		$V_{DD} \ge 7.5V$	350			ns

AC Electrical Characteristics (Continued)

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Clock Pulse Width Low/High	t_{OL}, t_{OH}	V_{DD} = 3V	450			ns
		V_{DD} = 5V	220			ns
		$V_{DD} \geq 7.5V$	140			ns
Clock Pulse Width Low/High (cascaded)	t_{OH}	V_{DD} = 3V	750			ns
		V_{DD} = 5V	320			ns
		$V_{DD} \geq 7.5V$	180			ns
Clock Rise, Fall Time (Note 4)	t_r, t_f			1		µs
Data-In Setup	t_{DS}	V_{DD} = 3V	300			ns
		V_{DD} = 5V	150			ns
		$V_{DD} \geq 7.5$	120			ns
$\overline{CS}$ Setup to Clock	t_{CSC}	V_{DD} = 3V	200			ns
		V_{DD} = 5V	100			ns
		$V_{DD} \geq 7.5V$	50			ns
Data-In Hold	t_{DH}	V_{DD} = 5V	10			ns
		$V_{DD} \geq 7.5V$	10			ns
$\overline{CS}$ Hold	t_{CCS}	V_{DD} = 3V	450			ns
		V_{DD} = 5V	220			ns
		$V_{DD} \geq 7.5V$	140			ns
Load Pulse Setup (Note 5)	t_{CL}	V_{DD} = 3V	500			ns
		V_{DD} = 5V	280			ns
		$V_{DD} \geq 7.5V$	180			ns
$\overline{CS}$ Hold (rising LOAD to rising $\overline{CS}$)	t_{LCS}	V_{DD} = 3V	300			ns
		V_{DD} = 5V	200			ns
		$V_{DD} \geq 7.5V$	150			ns
Load Pulse Delay	t_{LC}		0			ns
Load Pulse Width (Note 5)	t_{LW}	V_{DD} = 3V	500			ns
		V_{DD} = 5	220			ns
		$V_{DD} \geq 7.5V$	140			ns
$\overline{CS}$ Setup to Load	t_{CSL}		0			ns
Data Out Valid from Clock	t_{CDO}	V_{DD} = 3V			550	ns
		V_{DD} = 5V			220	ns
		$V_{DD} \geq 7.5V$			110	ns

Note 1 **Absolute Maximum Ratings** indicate limits beyond which damage to the device may occur. **Electrical Characteristics** do not apply when operating the device beyond its specified **Operating Ratings**.

Note 2 All voltages are referred to V_{SS} = 0V.

Note 3 **Minimum** and **Maximum** values are 100% tested. **Typical** values represent the most likely parametric norm.

Note 4 Power consumption increases for clock rise or fall times greater than 100ns.

Note 5 LOAD may also be held high while clocking. In this case, the latch is transparent, and the falling edge of LOAD will latch the data.

Note 6 $V_{DD} - 32V < V_{BB} < V_{DD} - 5V$ is required for proper device operation

Note 7 Guaranteed by design.

Note 8 Parameters are not tested using this load. This is given as a maximum only.

Applications Information

The MIC8013 utilizes a serial data interface as a means of programming the LCD segment outputs.

An internal shift register is used to load segment data, and a latch is used to transfer this data to the segment drivers. The shift register can be loaded when chip select is held low (V_{SS}). DATA INPUT is shifted in on the falling edges of $\overline{CLOCK}$, and the contents of the shift register exit at SERIAL DATA OUTPUT on the rising edges of $\overline{CLOCK}$. A high level (V_{DD}) at LOAD enables the transfer of data from the shift register to the latch. The latch is transparent while LOAD is held high.

If data is shifted into the internal register but not immediately loaded into the latch, $\overline{CLOCK}$ should remain high. The driver may then be deselected without disturbing the contents of the shift register. If $\overline{CLOCK}$ is held low while $\overline{CHIP\ SELECT}$ is toggled, an extra clock pulse will be generated in the chip, thereby shifting the data.

A data "1" causes the associated segment output to operate 180° out of phase with the backplane output, thus turning the segment on (the segment becomes opaque). If a "0" is loaded, the associated segment will remain off (clear).

Several chips can be cascaded by simply connecting SERIAL DATA OUTPUT from one chip to DATA INPUT of the next. LOAD, $\overline{CLOCK}$, and $\overline{CHIP\ SELECT}$ are each paralleled to allow simultaneous control of all drivers with only 3 lines plus one data line.

Power Supplies

The MIC8013 can operate from a single supply of V_{DD} = 4 to 18V, with V_{BB} and V_{SS} at ground, or from two supplies with V_{DD} for logic voltage and V_{BB} for segment/backplane voltage. V_{BB} is then negative with respect to V_{SS}, and the potential across V_{DD} and V_{BB} must be limited to 35V. If 5V logic levels are used to program the display driver, then V_{DD} should be 5V. The segment and backplane drivers obtain maximum available output swing by switching from V_{BB} to V_{DD}. For higher output voltage swing see the MIC8030 series devices.

Internal Oscillator

The on-chip oscillator (Figure 1) is available in two configurations. Devices with the "-01" suffix feature a 1-pin oscillator (LCDϕ and LCDϕ Option tied together). An external resistor and capacitor set the operating frequency (see Figure 2), and the backplane frequency is $f_{OSC} \div 256$. With R_{OSC} = 150kΩ and C_{OSC} = 470pF, f_{OSC} = 25.6kHz and f_{BP} = 100Hz.

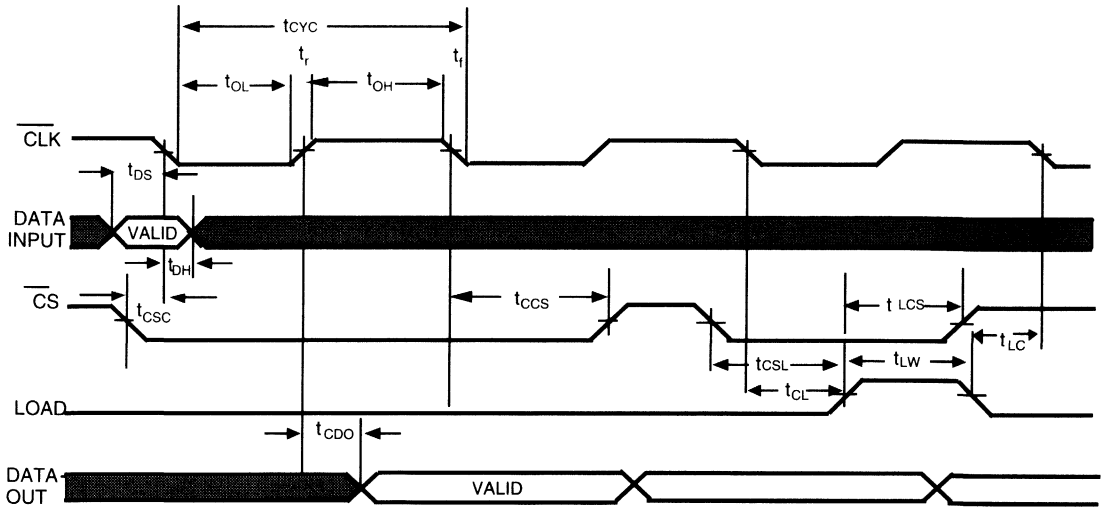
Devices with a "-02" suffix bring out only LCDϕ, leaving LCDϕ Option disconnected. In this case LCDϕ is driven with an external clock; in a typical application several MIC8013-02 drivers would be slaved to a master MIC8013-01 to drive a large display with a common backplane. Figure 2 shows this mode of operation. The input clock signal resets the divider shown in Figure 1 on each cycle so that the backplane operates at the external clock frequency.

An "-03" suffix version of this part is available which offers the option of using either of the two above mentioned configurations. The $\overline{CHIP\ SELECT}$ is always low on this option; contact factory for more details.

The oscillator may be disabled entirely, which allows the segment and backplane outputs to operate in a static, dc manner. LCDϕ is connected to V_{DD} for this mode, used primarily for driving LED and VF type displays.

4

Timing Diagram



Logic Truth Table

Data In	Clock	Chip Select	Load	Q_1(SR)	Q_N(SR)	BP	Q_N(Driver)
X	X	1	0	NC	NC	0	Q_N(L)
X	X	1	1	NC	NC	1	Q_N(L)
0	↑	0	0	NC	NC	1	Q_N(L)
0	↑	0	1	NC	NC	1	Q_N(L)
0	↓	0	0	0	$Q_{(N-1)}$—Q_N	1	Q_N(L)
0	↓	0	1	0	$Q_{(N-1)}$—Q_N	1	Q_N(SR)
1	↑	0	0	NC	NC	1	Q_N(L)
1	↑	0	1	NC	NC	1	Q_N(L)
1	↓	0	0	1	$Q_{(N-1)}$—Q_N	1	Q_N(L)
1	↓	0	1	1	$Q_{(N-1)}$—Q_N	1	Q_N(SR)

↑ = Rising Edge, ↓ = Falling Edge

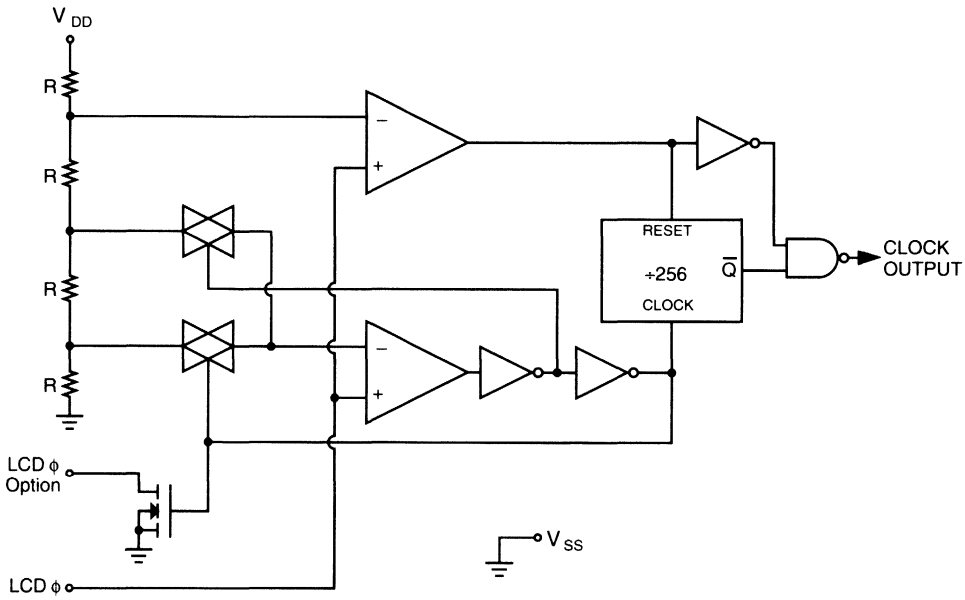


Figure 1. Internal Oscillator Circuit

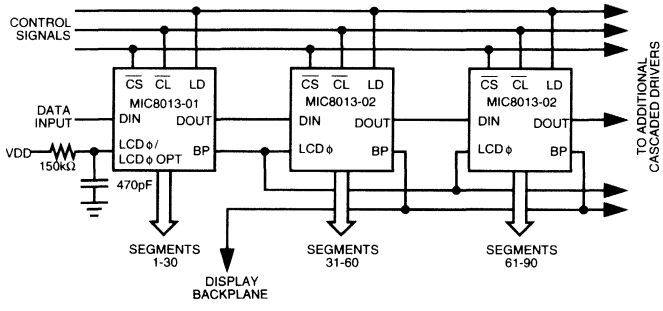


Figure 2. Cascading with Internal Clock Oscillator - 01 Option

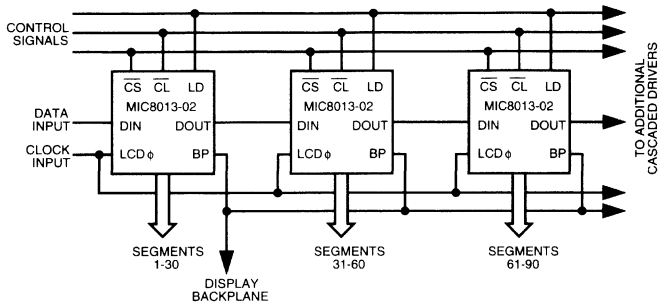


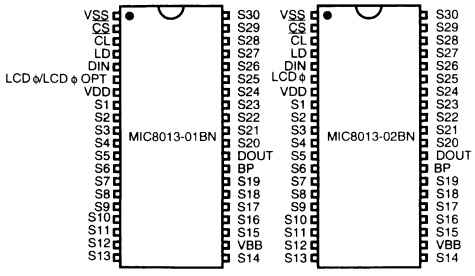
Figure 3. Cascading with External Clocking Source - 02 Option

Pin Assignments

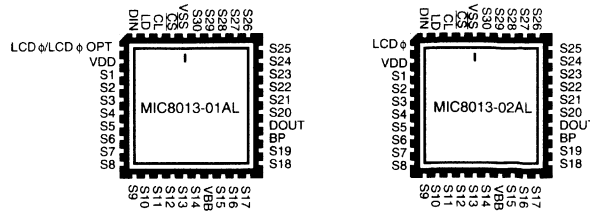
	Device Suffix	
Function	**-01**	**-02**
V_{SS} (Ground)	1	1
Chip Select	2	2
Clock	3	3
Load	4	4
Data Input	5	5
LCDϕ	6	6
LCDϕ Option	6	NC
V_{DD}	7	7
Segment 1	8	8
Segment 2	9	9
Segment 3	10	10
Segment 4	11	11
Segment 5	12	12
Segment 6	13	13
Segment 7	14	14
Segment 8	15	15
Segment 9	16	16
Segment 10	17	17
Segment 11	18	18
Segment 12	19	19
Segment 13	20	20

	Device Suffix	
Function	**-01**	**-02**
Segment 14	21	21
V_{BB}	22	22
Segment 15	23	23
Segment 16	24	24
Segment 17	25	25
Segment 18	26	26
Segment 19	27	27
Backplane	28	28
Data Output	29	29
Segment 20	30	30
Segment 21	31	31
Segment 22	32	32
Segment 23	33	33
Segment 24	34	34
Segment 25	35	35
Segment 26	36	36
Segment 27	37	37
Segment 28	38	38
Segment 29	39	39
Segment 30	40	40

Connection Diagrams



40-Pin Plastic DIP



40-Pin Ceramic Chip Carrier

MIC8014

Liquid Crystal Display Driver

General Description

The MIC8014 driver is designed for use with liquid crystal displays. A serial data interface is used to load an internal register, which in turn controls the segment outputs. A FIFO output allows multiple chips to be cascaded and programmed via a single, serial interface. An on-chip backplane oscillator is included.

In addition to the package options shown, the MIC8014 is available in die form; contact the factory concerning dice and custom packaging requirements

Features

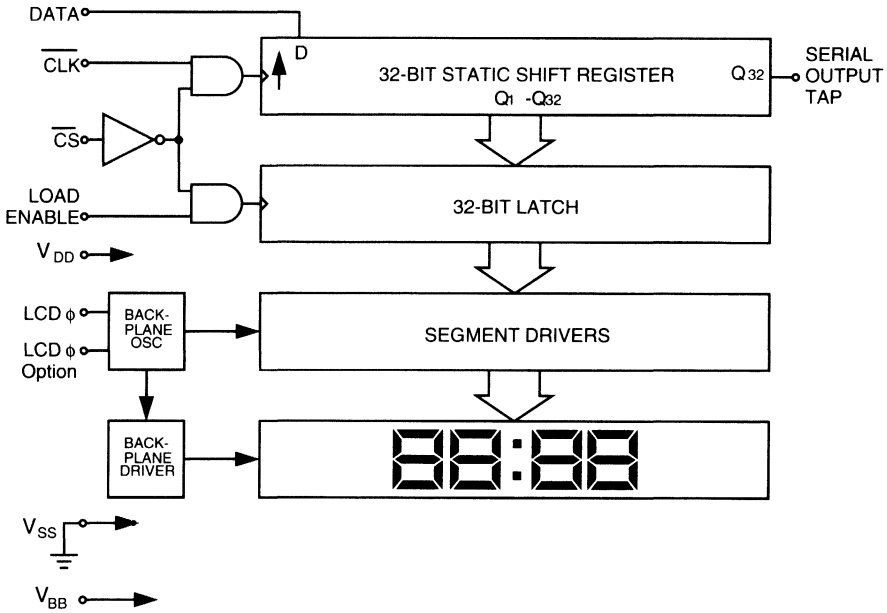
- Pin to pin compatible with AMI/Gould S4520
- Drives 32 segments
- Built using Micrel's proprietary rugged high voltage CMOS process for improved reliability
- Compatible with dichroic, midchroic, VF or TM displays
- Internal or external backplane oscillator
- 3V to 18V logic supply range
- 5V to 35V output drive swing
- Single or split power supply operation
- Mil spec (883C) or extended temperature range part available; contact factory for details
- Cascadable serial interface
- 60V extended output swing available; contact factory for details

Ordering Information

Part Number	Temperature Range	Package
MIC8014-03BV	–40°C to +85°C	44-pin PLCC
MIC8014-03AE	–55°C to +125°C	44-pin CERQUAD

4

Block Diagram



Note: The MIC8014 is ESD sensitive.

Absolute Maximum Ratings (Note 1, 2)

V_{DD}	−0.3V to +17V	Operating Temperature Range:	
V_{BB}	V_{SS} + 0.3V to V_{DD} − 32V	MIC8014-03BV	−40°C to +85°C
Input Voltage (except LCDϕ)	V_{SS} − 0.3V to V_{DD} + 0.3V	MIC8014-03AE	−55°C to +125°C
LCDϕ Input Voltage	V_{BB} − 35V to V_{DD} + 0.3V	Storage Temperature Range	−65°C to +150°C
DC Current Drain per input pin	10 mA	Power Dissipation	250 mW

DC Electrical Characteristics (Notes 3 and 4)

$3V \le V_{DD} \le 16V$, $V_{BB} = -25V$, $V_{SS} = 0V$, $-55°C \le T_A \le +125°C$, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Logic Supply Voltage	V_{DD}		3		16	V
Display Supply Voltage	V_{BB}	$V_{BB} \le V_{SS}$	V_{DD}−32		V_{DD}−5	V
Supply Current (external oscillator)	I_{DD}	no load, CMOS input levels			200	µA
Supply Current		$V_{DD} \le 5V$			200	µA
(internal oscillator)		no load, V_{DD} = 16V, CMOS input levels			750	µA
Display Driver Current	I_{BB}	f_{BP} = 100Hz, no load			−200	µA
Input Low Voltage (excluding LCDϕ)	V_{IL}		V_{SS}		$0.2V_{DD}$	V
Input High Voltage (excluding LCDϕ)	V_{IH}	$V_{DD} \ge 5V$	$0.5V_{DD}$		V_{DD}	V
Input Low Voltage (LCDϕ)	V_{ILX}	externally driven	V_{BB}		$0.1V_{DD}$	V
Input High Voltage (LCDϕ)	V_{IHX}	externally driven	$0.9V_{DD}$		V_{DD}	V
Input Leakage Current	I_L	V_{DD} = 0 to 5V			1	µA
Input Capacitance	C_I				5	pF
DC Bias (Average) Any Segment Output to Backplane	V_{OAVG}	Note 7			±25	mV
Segment Output	C_{LSEG}	Note 8			1000	pF
Backplane Output	C_{LBP}				40,000	pF
Segment Output Impedance	R_{SEG}	I_L = 10µA			10	kΩ
Backplane Output Impedance	R_{BP}	I_L = 10µA			312	Ω
Data Out Output Impedance	R_{DD}				3	kΩ
Data Out Current	I_{DOH}	Source Current, $V_{OH} = V_{DD} - 5V$			0.6	mA
	I_{DOL}	Sink Current, V_{OL} = 0.5V	−0.6			mA

AC Electrical Characteristics (Note 3)

$V_{BB} = -25V$, $V_{SS} = 0V$, $T_A = 25°C$, no load, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Cycle Time	t_{CYC}	V_{DD} = 3V	1000			ns
		V_{DD} = 5V	500			ns
		$V_{DD} \ge 7.5V$	320			ns
Cycle Time (cascaded)	t_{CYC}	V_{DD} = 3V	1300			ns
		V_{DD} = 5V	600			ns
		$V_{DD} \ge 7.5V$	350			ns

AC Electrical Characteristics (Continued)

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Clock Pulse Width Low/High	t_{OL}, t_{OH}	V_{DD} = 3V	450			ns
		V_{DD} = 5V	220			ns
		$V_{DD} \geq$ 7.5V	140			ns
Clock Pulse Width Low/High (cascaded)	t_{OH}	V_{DD} = 3V	750			ns
		V_{DD} = 5V	320			ns
		$V_{DD} \geq$ 7.5V	180			ns
Clock Rise, Fall Time (Note 4)	t_r, t_f			1		µs
Data-In Setup	t_{DS}	V_{DD} = 3V	300			ns
		V_{DD} = 5V	150			ns
		$V_{DD} \geq$ 7.5	120			ns
$\overline{CS}$ Setup to Clock	t_{CSC}	V_{DD} = 3V	200			ns
		V_{DD} = 5V	100			ns
		$V_{DD} \geq$ 7.5V	50			ns
Data-In Hold	t_{DH}	V_{DD} = 5V	10			ns
		$V_{DD} \geq$ 7.5V	10			ns
$\overline{CS}$ Hold	t_{CCS}	V_{DD} = 3V	450			ns
		V_{DD} = 5V	220			ns
		$V_{DD} \geq$ 7.5V	140			ns
Load Pulse Setup (Note 5)	t_{CL}	V_{DD} = 3V	500			ns
		V_{DD} = 5V	280			ns
		$V_{DD} \geq$ 7.5V	180			ns
$\overline{CS}$ Hold (rising LOAD to rising $\overline{CS}$)	t_{LCS}	V_{DD} = 3V	300			ns
		V_{DD} = 5V	200			ns
		$V_{DD} \geq$ 7.5V	150			ns
Load Pulse Delay	t_{LC}		0			ns
Load Pulse Width (Note 5)	t_{LW}	V_{DD} = 3V	500			ns
		V_{DD} = 5	220			ns
		$V_{DD} \geq$ 7.5V	140			ns
$\overline{CS}$ Setup to Load	t_{CSL}		0			ns
Data Out Valid from Clock	t_{CDO}	V_{DD} = 3V			550	ns
		V_{DD} = 5V			220	ns
		$V_{DD} \geq$ 7.5V			110	ns

Note 1 **Absolute Maximum Ratings** indicate limits beyond which damage to the device may occur. **Electrical Characteristics** do not apply when operating the device beyond its specified **Operating Ratings**.

Note 2 All voltages are referred to V_{SS} = 0V.

Note 3 **Minimum** and **Maximum** values are 100% tested. **Typical** values represent the most likely parametric norm.

Note 4 Power consumption increases for clock rise or fall times greater than 100ns.

Note 5 LOAD may also be held high while clocking. In this case, the latch is transparent, and the falling edge of LOAD will latch the data.

Note 6 $V_{DD} - 32V < V_{BB} < V_{DD} - 5V$ is required for proper device operation

Note 7 Guaranteed by design.

Note 8 Parameters are not tested using this load. This is given as a maximum only.

Applications Information

The MIC8014 utilizes a serial data interface as a means of programming the LCD segment outputs.

An internal shift register is used to load segment data, and a latch is used to transfer this data to the segment drivers. The shift register can be loaded when chip select is held low (V_{SS}). DATA INPUT is shifted in on the falling edges of $\overline{CLOCK}$, and the contents of the shift register exit at SERIAL DATA OUTPUT on the rising edges of $\overline{CLOCK}$. A high level (V_{DD}) at LOAD enables the transfer of data from the shift register to the latch. The latch is transparent while LOAD is held high.

If data is shifted into the internal register but not immediately loaded into the latch, $\overline{CLOCK}$ should remain high. The driver may then be deselected without disturbing the contents of the shift register. If $\overline{CLOCK}$ is held low while $\overline{CHIP\ SELECT}$ is toggled, an extra clock pulse will be generated in the chip, thereby shifting the data.

A data "1" causes the associated segment output to operate 180° out of phase with the backplane output, thus turning the segment on (the segment becomes opaque). If a "0" is loaded, the associated segment will remain off (clear).

Several chips can be cascaded by simply connecting SERIAL DATA OUTPUT from one chip to DATA INPUT of the next. LOAD, $\overline{CLOCK}$, and $\overline{CHIP\ SELECT}$ are each paralleled to allow simultaneous control of all drivers with only 3 lines plus one data line.

Power Supplies

The MIC8013 can operate from a single supply of V_{DD} = 4 to 18V, with V_{BB} and V_{SS} at ground, or from two supplies with V_{DD} for logic voltage and V_{BB} for segment/backplane voltage. V_{BB} is then negative with respect to V_{SS}, and the potential across V_{DD} and V_{BB} must be limited to 35V. If 5V logic levels are used to program the display driver, then V_{DD} should be 5V. The segment and backplane drivers obtain maximum available output swing by switching from V_{BB} to V_{DD}. For higher output voltage swing see the MIC8030 series devices.

Internal Oscillator

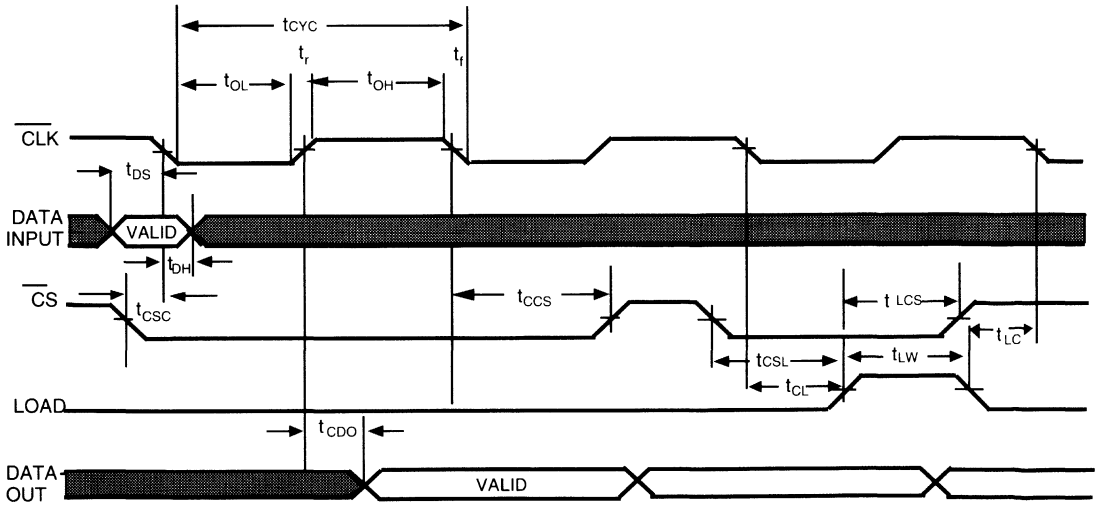
The on-chip oscillator (Figure 1) is available in two configurations. If pins 19 and 20 are tied together, (LCDϕ and LCDϕ Option tied together) a one pin oscillator configuration results. An external resistor and capacitor set the operating frequency (see Figure 2), and the backplane frequency is $f_{OSC} \div 256$. With R_{OSC} = 150kΩ and C_{OSC} = 470pF, f_{OSC} = 25.6kHz and f_{BP} = 100Hz.

To configure this device such that an external oscillator can be used, connect the oscillator to LCDϕ, leaving LCDϕ Option disconnected. In a typical application, several MIC8014 to drive a large display with a common backplane. Figure 2 shows this mode of operation. The input clock signal resets the divider shown in Figure 1 on each cycle so that the backplane operates at the external clock frequency.

An "-03" suffix is used to indicate this device has both LCDϕ and LCDϕ Option pinned out externally, unlike other members of the MIC8010 family.

The oscillator may be disabled entirely, which allows the segment and backplane outputs to operate in a static, DC manner. LCDϕ is connected to V_{DD} for this mode, used primarily for driving VF and LED displays.

Timing Diagram



Logic Truth Table

Data In	Clock	Chip Select	Load	Q_1(SR)	Q_N(SR)	BP	Q_N(Driver)
X	X	1	0	NC	NC	0	Q_N(L)
X	X	1	1	NC	NC	1	Q_N(L)
0	↑	0	0	NC	NC	1	Q_N(L)
0	↑	0	1	NC	NC	1	Q_N(L)
0	↓	0	0	0	$Q_{(N-1)}$—Q_N	1	Q_N(L)
0	↓	0	1	0	$Q_{(N-1)}$—Q_N	1	Q_N(SR)
1	↑	0	0	NC	NC	1	Q_N(L)
1	↑	0	1	NC	NC	1	Q_N(L)
1	↓	0	0	1	$Q_{(N-1)}$—Q_N	1	Q_N(L)
1	↓	0	1	1	$Q_{(N-1)}$—Q_N	1	Q_N(SR)

↑ = Rising Edge, ↓ = Falling Edge

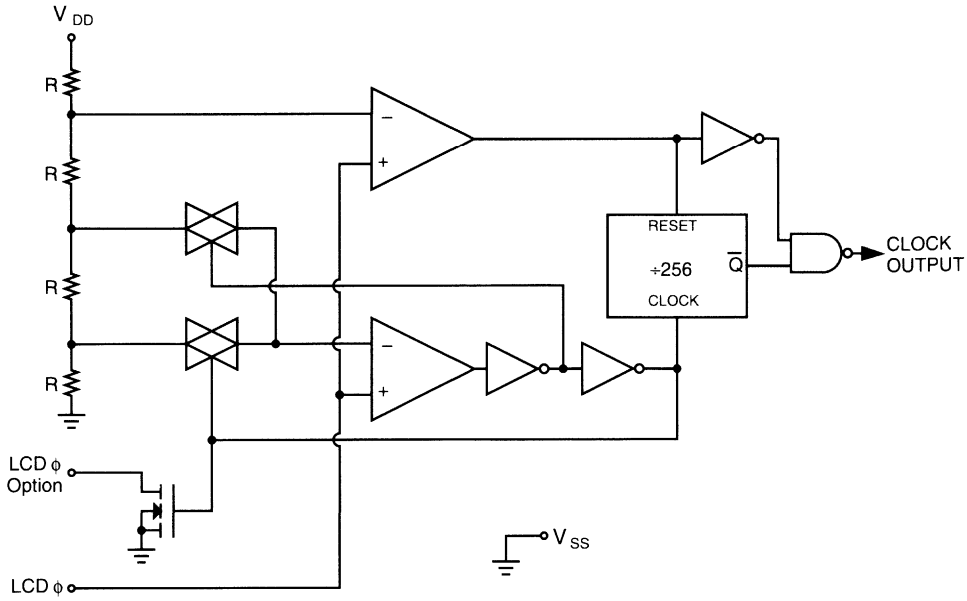


Figure 1. Internal Oscillator Circuit

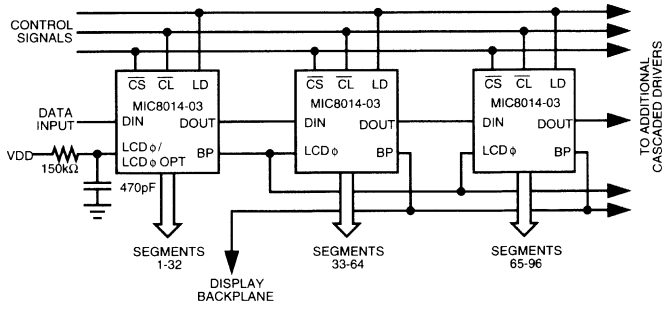


Figure 2. Cascading with Internal Clock Oscillator

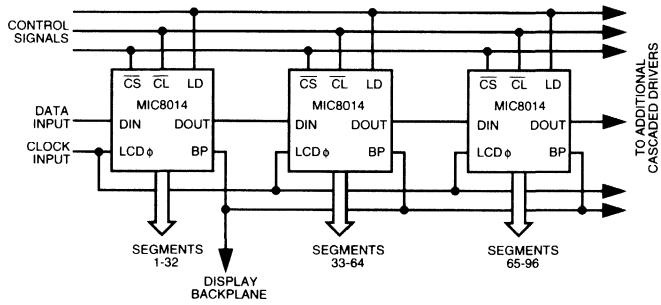


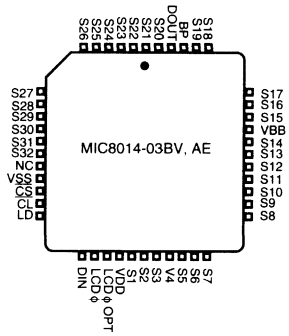
Figure 3. Cascading with External Clocking Source - 02 Option

Pin Assignments

Function	Device Suffix -03
Segment 21	1
Segment 22	2
Segment 23	3
Segment 24	4
Segment 25	5
Segment 26	6
Segment 27	7
Segment 28	8
Segment 29	9
Segment 30	10
Segment 31	11
Segment 32	12
NC	13
V_{SS} (Ground)	14
$\overline{\text{Chip Select}}$	15
$\overline{\text{Clock}}$	16
Load	17
Data In	18
LCDφ	19
LCDφ Option	20
V_{DD}	21
Segment 1	22

Function	Device Suffix -03
Segment 2	23
Segment 3	24
Segment 4	25
Segment 5	26
Segment 6	27
Segment 7	28
Segment 8	29
Segment 9	30
Segment 10	31
Segment 11	32
Segment 12	33
Segment 13	34
Segment 14	35
V_{BB}	36
Segment 15	37
Segment 16	38
Segment 17	39
Segment 18	40
Segment 19	41
BP	42
Data Out	43
Segment 20	44

Connection Diagram



MIC8030/8031

High Voltage Display Driver

General Description

The MIC8030/MIC8031 is a CMOS high voltage liquid crystal display driver. Up to 38 segments can be driven from four CMOS level inputs (CLOCK, DATA IN, LOAD and $\overline{\text{CHIP SELECT}}$). The MIC8031 is rated at 100V and the MIC8030 is rated at 50V. Data is loaded serially into a shift register, and transferred to latches which hold the data until new data is received.

The backplane can be driven from external source, or the internal oscillator can be used. If the internal oscillator is used, the frequency of the backplane will be determined by an external resistor and capacitor. The oscillator need not be used if a DC output is desired.

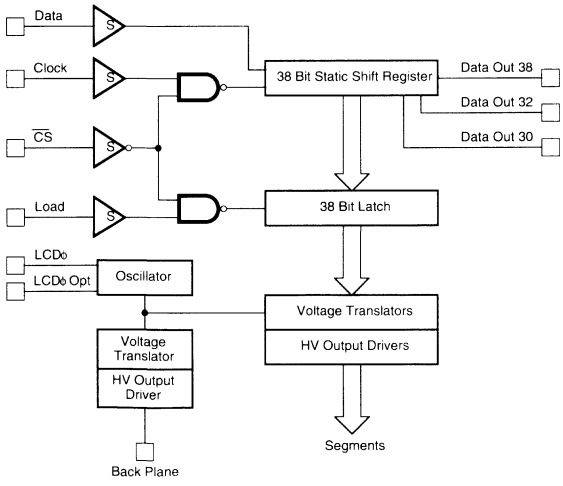
Features

- High Voltage Outputs capable of a driving up to 100 volt outputs from 5 to 15 volt logic
- Drives 30, 32, or 38 segments
- Cascadable
- On chip Oscillator or External Backplane Input
- CMOS construction for wide supply range and low power consumption
- Schmitt Triggers on all inputs
- CMOS, PMOS, and NMOS compatible

Applications

- Dichroic and Standard Liquid Crystal Displays
- Flat Panel Displays
- Print Head Drives
- Vacuum Fluorescent Displays

Functional Diagram

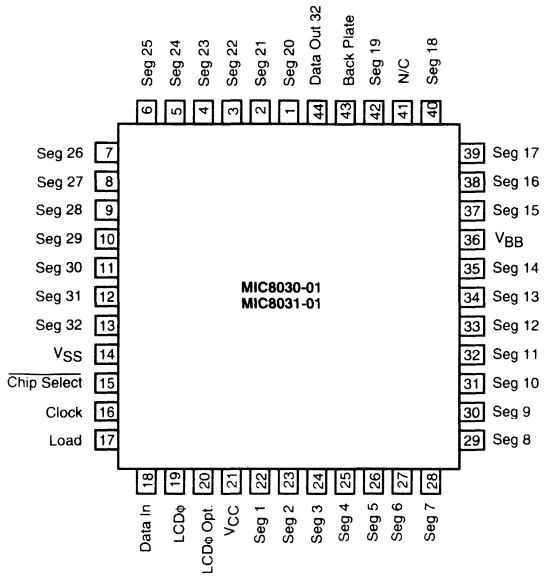


Ordering Information

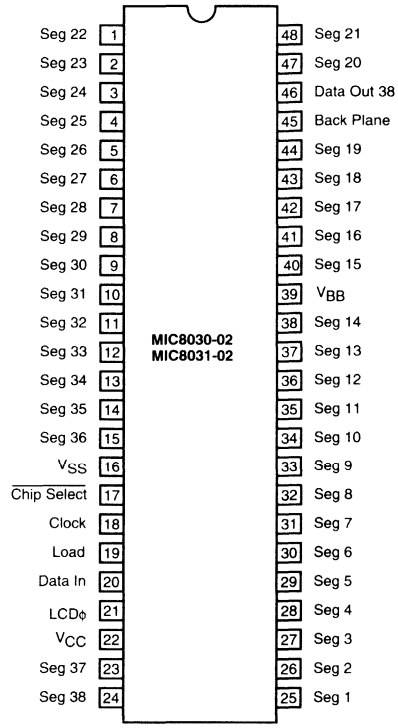
Part Number	Temperature Range	Package
MIC8030-01AEB MIC8031-01AEB	–55°C to +125°C	44-lead CER QUAD, Class B screened
MIC8030-01CV MIC8031-01CV	0°C to +70°C	44-pin PLCC
MIC8030-02CN MIC8031-02CN	0°C to +70°C	48-pin Plastic DIP

* Contact factory for other package options.

Pin Configuration 44-Pin CER QUAD - E 44-Pin LCC -L 44-Pin PLCC -V



Pin Configuration 48-Pin Plastic DIP - N



Functional Description

With CHIP SELECT tied low, serial data is clocked into the shift register at each falling edge of the CLOCK input. Pulling LOAD high will cause a parallel loading of the shift register contents into the latches. If load is left high, the latches are transparent.

A logic "1" clocked into the shift register corresponds to that segment being on, and that segment is out of phase with the backplane.

The backplane may be externally driven or the internal oscillator can be used. If LCDϕ is externally driven, the backplane will be in phase with the input; LCDϕ OPT is not connected. The internal oscillator is used by shorting LCDϕ OPT to LCDϕ, connecting a capacitor to ground, and a resistor to V_{CC}. The frequency of the backplane will be 1/256 of the input frequency, and is given as: $f = 10/[R(C + .0002)]$ at V_{DD} = 5V, R in kΩ, C in μF.

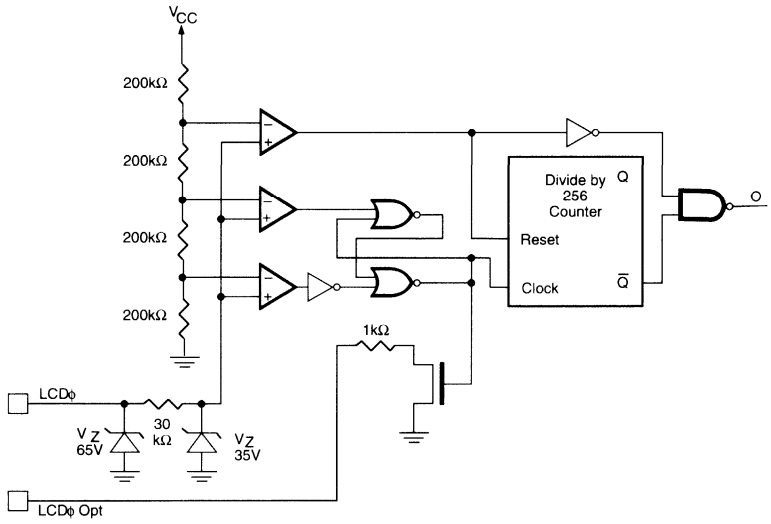
Example: R = 150 kΩ, C = 420 pF: f = 108 Hz

For displays with more than 38 segments, two or more MIC8030/MIC8031 may be cascaded by connecting DATA OUT of the previous stage with DATA IN of the next stage; CLOCK, LOAD and CHIP SELECT of all following stages should be tied to the control lines of the first MIC8030/MIC8031. The backplane output of the first stage should be tied to LCDϕ of all following stages, the LCDϕ OPT must be left unconnected on those stages. If the internal oscillator is used, and V_{BB} > 50V then an external 330 kΩ resistor must be used between the BACKPLANE of the first stage and LCDϕ of all following stages.

Packaging options available include DATA OUT 30, 32 or 38 with the corresponding number of segments, and the availability of LCDϕ OPT. Types of packages include plastic and ceramic DIPs, surface mount packages, plastic and ceramic Leadless Chip Carriers and custom packaging.

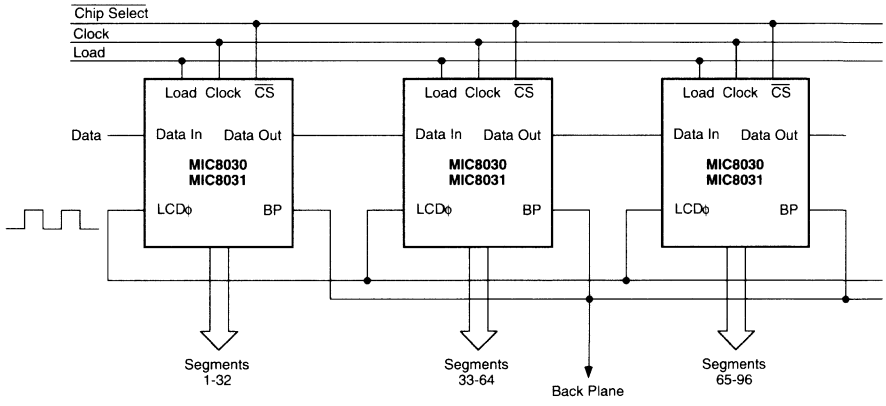
4

Internal Oscillator Circuit

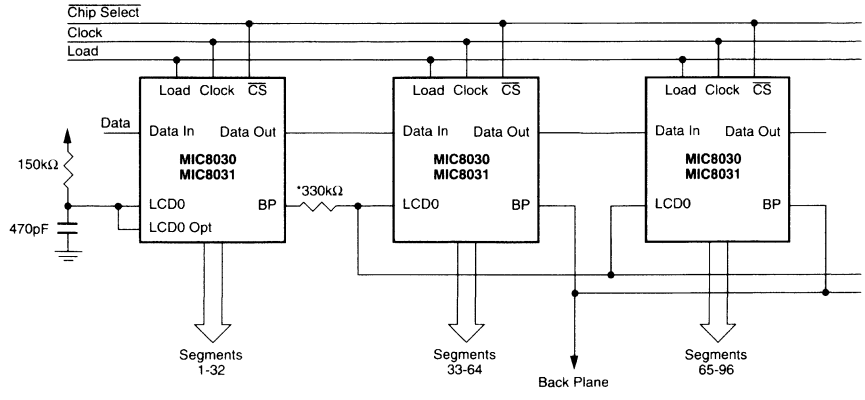


Typical Application

External Oscillator



Internal Oscillator



*Required if using MIC8031 with V_{BB} > 50V.

Absolute Maximum Ratings

V_{CC}	18V
V_{BB} (MIC8030)	75V
V_{BB} (MIC8031)	110V
Inputs (CLK, DATA IN, LOAD, $\overline{CS}$)	–0.5V to 18V
Inputs (LCD0)	–0.5V to 50V
Storage Temperature	–65°C to +150°C
Operating Temperature	–55°C to +125°C
Maximum Current into and out of any segment	20 mA
Maximum Power Dissipation, any segment	50 mW
Maximum Total power dissipation	600 mW

DC Electrical Characteristics: V_{CC} = 5V, V_{SS} = 0V, V_{BB} = 50V (MIC3830), V_{BB} = 100V (MIC3831), –55°C ≤ T_A ≤ +125°C, unless otherwise noted.

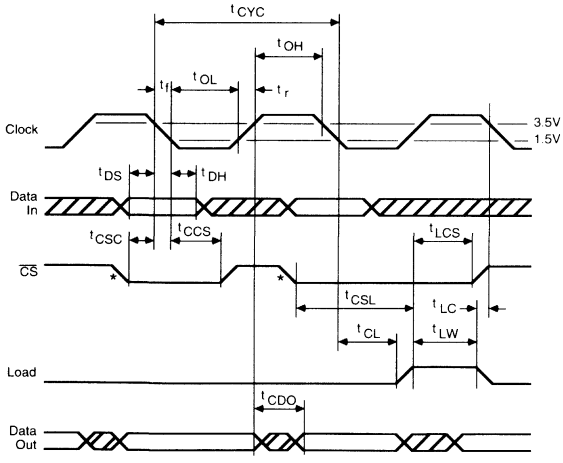
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
POWER SUPPLY						
V_{CC}	Logic Supply Voltage	MIC8030	4.5	5	5.5	V
V_{CC}	Logic Supply Voltage	MIC8031	4.5	5	16.5	V
V_{BB}	Display Supply Voltage	MIC8030	20	35	50	V
V_{BB}	Display Supply Voltage	MIC8031	20	35	100	V
I_{CC}	Supply Current (external oscillator)	Note 1		35	250	µA
	Supply Current (internal oscillator)	Note 1		35	250	
I_{BB}	Display Driver Current	F_{BP} = 100Hz No Loads		7	100	µA
I_{BB}	Display Driver Current	MIC8031, V_{BB} = 100V		20	200	µA
INPUTS (CLK, DATA IN, LOAD, $\overline{CS}$)						
V_{IH}	Input High Level		V_{CC} - 1.5	V_{CC} - 1.8	V_{CC}	V
V_{IL}	Input Low Level		0	2.5	2.0	V
I_L	Input Leakage Current			<1	5	µA
C_I	Input Capacitance	Note 2		5	10	pF
INPUT LCD0						
V_{IH}	LCD0 Input High Level	Externally driven	0.9V_{CC}	V_{CC}	50	V
V_{IL}	LCD0 Input Low Level	Externally driven	–0.5V	0	0.1V_{CC}	V
I_{LCD0}	LCD0 Leakage Current	V_{LCD0} = 15V		2	10	µA
I_{LCD0}	LCD0 Leakage Current	V_{LCD0} = 35V		6	100	µA
I_{LCD0}	LCD0 Leakage Current	V_{LCD0} = 50V			1	mA
CAPACITANCE LOADS (TYPICAL)						
C_{LSEG}	Segment Output	FBP < 100Hz			100	pF
C_{LBP}	Backplane Output	FBP < 100Hz			4000	pF
V_{OAVG}	DC Bias (Average) Any Segment	FBP < 100Hz, Note 2			+25	mV
OUTPUT TO BACKPLANE						
R_{SEG}	Segment Output Impedance	I_L = 100µA		1.4	10	kΩ
R_{BP}	Backplane Output Impedance	I_L = 100µA		170	312	Ω
$R_{DATA\ OUT}$	Data Out Output Impedance	I_L = 100µA		1.8	3	kΩ

Note 1: CMOS input levels. No loads.
Note 2: Guaranteed by design but not tested on a production basis.

AC Electrical Characteristics: V_{CC} = 5V, V_{SS} = 0V, V_{BB} = 50V (MIC3830), V_{BB} = 50V (MIC3831), $-55°C \le T_A \le +125°C$

Symbol	Parameter	Min	Typ	Max	Units
t_{CYC}	Cycle Time	500			ns
t_{OL}, tOH	Clock Pulse Width low/high	250			ns
t_r, t_f	Clock rise/fall			1	µs
t_{DS}	Data In Setup	100			ns
t_{CSC}	$\overline{CS}$ Setup to Clock	100			ns
t_{DH}	Data Hold	10			ns
t_{CCS}	$\overline{CS}$ Hold	220			ns
t_{CL}	Load Pulse Setup	250			ns
t_{LCS}	$\overline{CS}$ Hold (rising load to rising $\overline{CS}$)	200			ns
t_{LW}	Load Pulse Width	300			ns
t_{LC}	Load Pulse Delay (falling load to falling clock)	0			ns
t_{CDO}	Data Out Valid from Clock			220	ns
t_{CSL}	$\overline{CS}$ Setup to LOAD	0			ns
F_{BP}	Backplane Frequency	50	100	2000	Hz

Timing Diagram



* The $\overline{CS}$ high-to-low transition will generate a clock pulse.

Logic Truth Table

Data In	Clock	Chip Select	Load	$Q_{1(SR)}$	$Q_{N(SR)}$	$Q_{N(DRIVER)}$
X	X	1	X	NC	NC	$Q_{N(L)}$
0	↑	0	0	NC	NC	$Q_{N(L)}$
0	↑	0	1	NC	NC	$Q_{N(L)}$
0	↓	0	0	0	$Q_N - 1 \rightarrow Q_N$	$Q_{N(L)}$
0	↓	0	1	0	$Q_N - 1 \rightarrow Q_N$	$Q_{N(SR)}$
1	↑	0	0	NC	NC	$Q_{N(L)}$
1	↑	0	1	NC	NC	$Q_{N(L)}$
1	↓	0	0	1	$Q_N - 1 \rightarrow Q_N$	$Q_{N(L)}$
1	↓	0	1	1	$Q_N - 1 \rightarrow Q_N$	$Q_{N(SR)}$

↑ = Rising Edge, ↓ = Falling Edge

MIC10937/10957

V. F. Alphanumeric Display Controller

Summary Information*

General Description

The MIC10937 and MIC10957 Alphanumeric Display Controllers are MOS/LSI general purpose display controllers designed to interface to segmented displays (vacuum fluorescent or LED).

The MIC10937 and MIC10957 will drive displays with up to 16 characters with 14 or 16 segments plus a decimal point and comma tail. Segment decoding within each device provides for the ASCII character set (upper case only). No external driver circuitry is required for displays that operate on 20mA of drive current up to 50V. A 16 × 64-bit segment decoder provides internal ASCII character set decoding for the display.

The MIC10937 and MIC10957 are identical with the exception that the MIC10957 has two additional decodings for the decimal point and comma tail.

Micrel has received the rights from Rockwell International to manufacture and market this product and reproduce the specifications, including references to Rockwell.

Features

- 16-character display with decimal point and comma tail
- 14 or 16-segment drivers
- Up to 66kHz data rate
- Direct digit drive and 20mA at 50V
- Supports vacuum fluorescent or LED displays
- 64 × 16-bit PLA provides segment decoding for ASCII character set (all caps only)
- Serial data input for 8-bit display and control data words
- 40-pin DIP or 44-pin PLCC

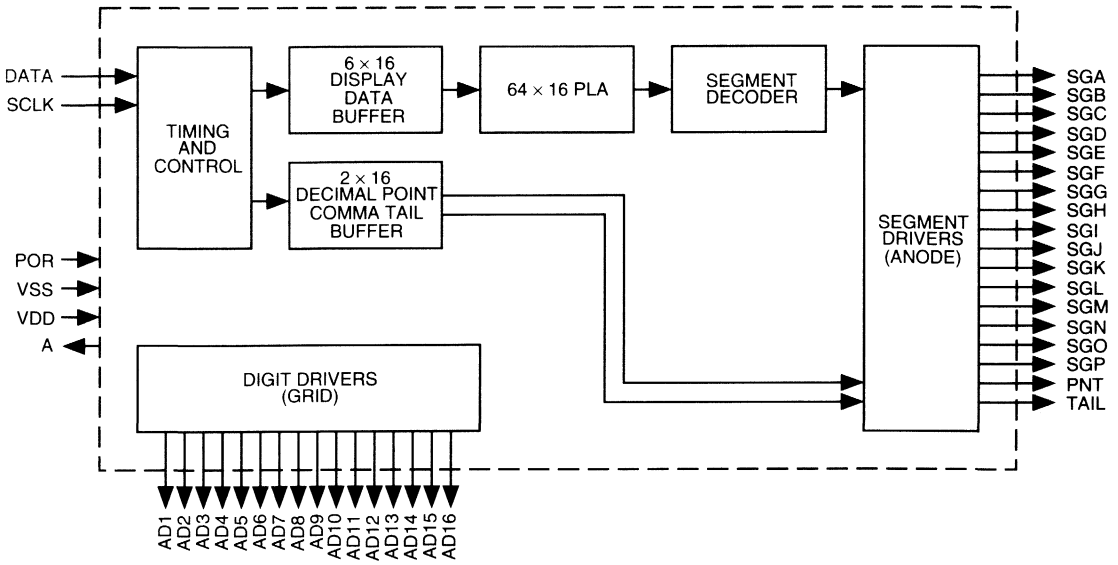
Ordering Information

Part Number†	Drive	Temp. Range	Package
MIC109x7P-40	40V	0°C to +70°C	Plastic
MIC109x7P-50	50V	0°C to +70°C	Plastic
MIC109x7PE-40	40V	–40°C to +85°C	Plastic
MIC109x7PE-50	50V	–40°C to +85°C	Plastic

† x = 3 or 5

4

Block Diagram



* Contact Micrel for more information.

MIC10938/10939

V. F. Dot Matrix Display Controller

Summary Information*

General Description

The MIC10938 and MIC10939 Dot Matrix Display Controller is a two-chip MOS/LSI general purpose display controller system designed to interface to dot matrix displays (vacuum fluorescent or LED).

The two-chip set will drive displays with up to 35 anodes (dots) and up to 20 grids (characters) plus a cursor. The chips can be cascaded to drive larger displays of as many as 80 characters.

An internal PLA-type decoder provides character decoding and dot pattern generation for the full 96-character ASCII set and an additional 32 special characters.

Micrel has received the rights from Rockwell International to manufacture and market this product and reproduce the specifications, including references to Rockwell.

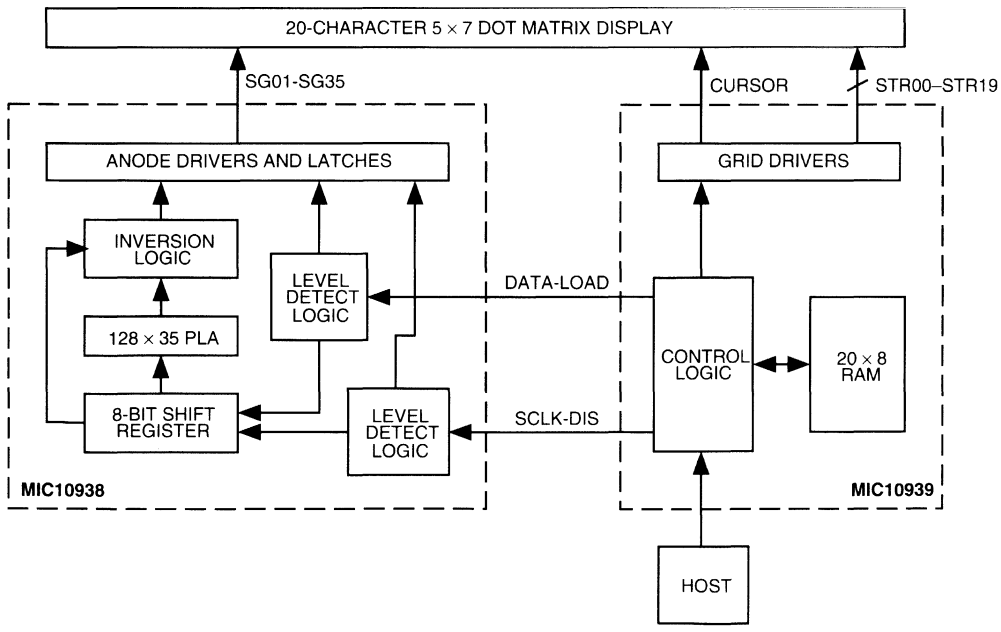
Features

- 20-character display driver cascadable to 80 characters
- Standard 5 × 7 character font
- Separate cursor driver output
- Direct drive capability for vacuum-fluorescent displays
- 128 × 35 PLA provides segment decoding for full 96-character ASCII set, plus 32 special characters
- Serial or parallel data input for 8-bit display and control characters
- 40-pin DIP or 44-pin PLCC

Ordering Information

Part Number	Temperature Range	Package
MIC10938P	0°C to +70°C	Plastic
MIC10938PE	–40°C to +85°C	Plastic
MIC10939P	0°C to +70°C	Plastic
MIC10939PE	–40°C to +85°C	Plastic

Block Diagram



* Contact Micrel for more information.

MIC10939/10942/10943

V. F. Dot Matrix Display Controller

Summary Information*

General Description

The MIC10939, MIC10942, and MIC10943 Dot Matrix Display Controller is a three-chip MOS/LSI general purpose display controller system designed to interface to dot matrix displays (vacuum fluorescent or LED).

The three-chip set will drive displays with up to 46 anodes (dots) and up to 20 grids (characters) plus a cursor. The chips can be cascaded to drive larger displays of up to 80 characters.

An internal PLA-type decoder provides character decoding and dot pattern generation for the full 96-character ASCII set and an additional 32 special characters.

Micrel has received the rights from Rockwell International to manufacture and market this product and reproduce the specifications, including references to Rockwell.

Features

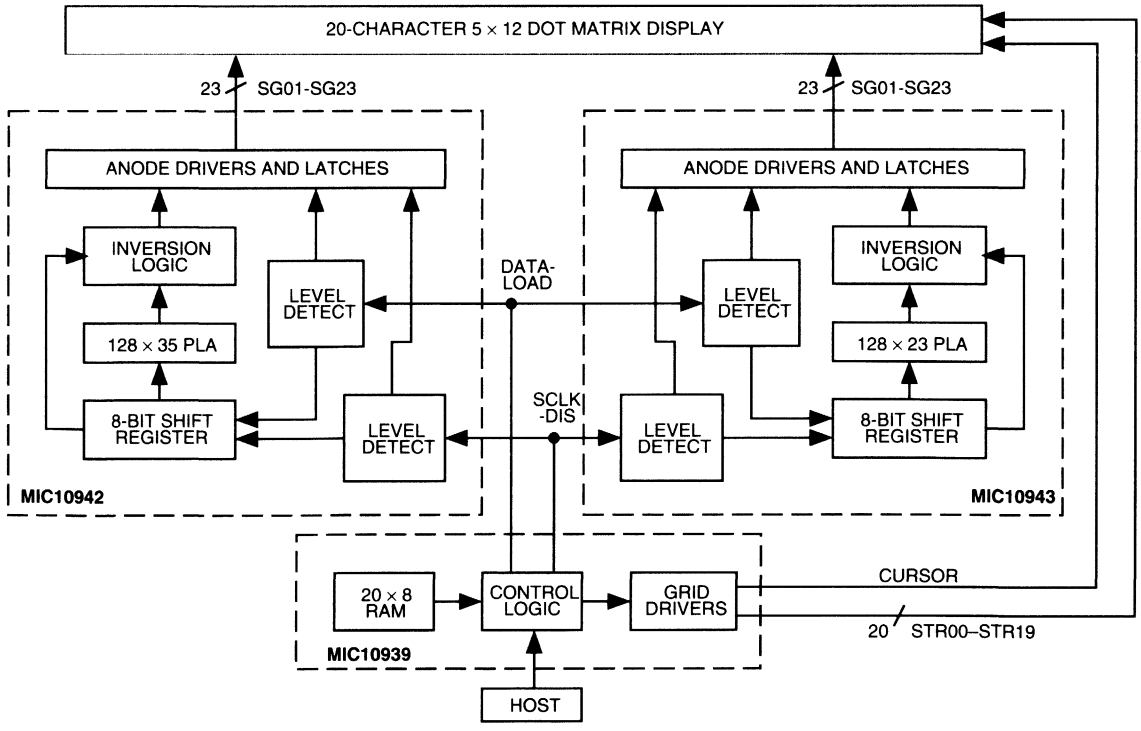
- 20-character display driver cascadable to 80 characters
- Standard 5 × 12 character font
- Separate cursor driver output
- Two 128 × 23 PLAs provides segment decoding for full 96-character ASCII set, plus 32 special characters
- Serial or parallel data input for 8-bit display mode controls
- Brightness, refresh rate, and display mode controls
- 40-pin DIP or 44-pin PLCC (MIC10939)
- 28-pin DIP (MIC10942 and MIC10943)

Ordering Information

Part Number	Temperature Range	Package
MIC10939P	0°C to +70°C	Plastic
MIC10939PE	–40°C to +85°C	Plastic
MIC10942P	0°C to +70°C	Plastic
MIC10942PE	–40°C to +85°C	Plastic
MIC10943P	0°C to +70°C	Plastic
MIC10943PE	–40°C to +85°C	Plastic

4

Block Diagram



* Contact Micrel for more information.

MIC10941/10939

V. F. Alphanumeric and Bargraph Display Controller

Summary Information*

General Description

The MIC10941 and MIC10939 Alphanumeric and Bargraph Display Controller is a two-chip MOS/LSI general purpose display controller system designed to interface with bargraph and segmented displays (vacuum fluorescent or LED).

The two-chip set will drive displays with up to 16 segments (plus decimal point and comma tail) and up to 20 grids (characters) plus a cursor. The chips can be cascaded to drive larger displays of 80 characters. Segment decoding for ASCII characters and bargraph patterns is accomplished through an internal PLA.

Micrel has received the rights from Rockwell International to manufacture and market this product and reproduce the specifications, including references to Rockwell.

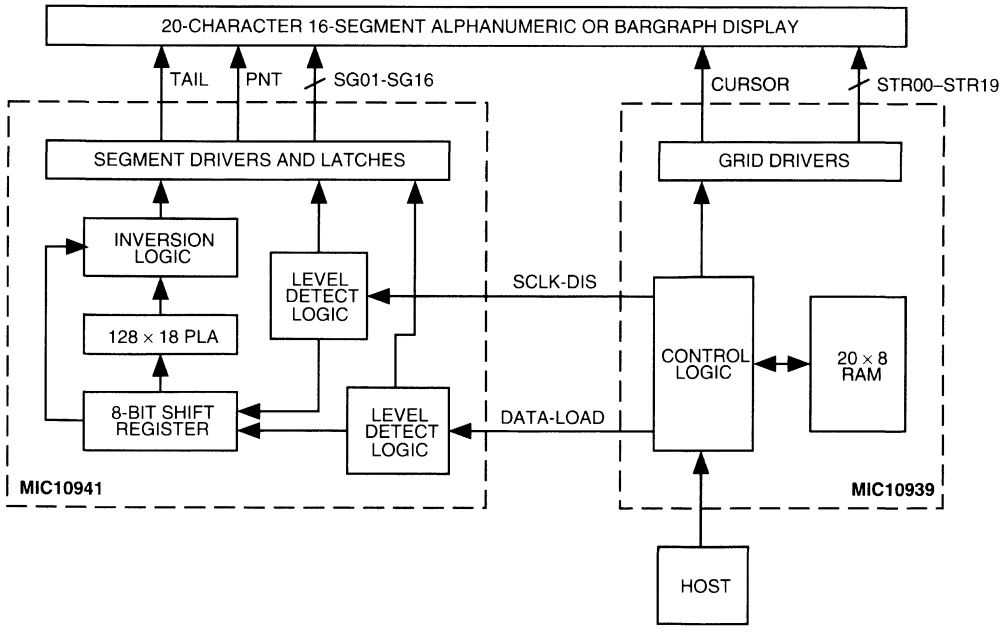
Features

- 20-character display driver cascadable to 80 characters
- Direct drive capability for vacuum-fluorescent displays
- 128 × 18 PLA provides segment decoding for ASCII characters (all caps only) and bargraph patterns
- Serial or parallel data input for 8-bit display and control characters
- Brightness, refresh rate, and display mode controls
- Separate cursor driver output
- 40-pin DIP or 44-pin PLCC (MIC10939)
- 24-pin DIP package (MIC10941)

Ordering Information

Part Number	Temperature Range	Package
MIC10941P	0°C to +70°C	Plastic
MIC10941PE	–40°C to +85°C	Plastic
MIC10939P	0°C to +70°C	Plastic
MIC10939PE	–40°C to +85°C	Plastic

Block Diagram



* Contact Micrel for more information.

MIC10951

V. F. Bargraph and Numeric Display Controller

Summary Information*

General Description

The MIC10951 Bargraph and Numeric Display Controller is an LSI general purpose display controller designed to interface to bargraph and numeric displays (vacuum fluorescent or LED).

The MIC10951 will drive 16-segment bargraph or 7-segment plus comma and decimal numeric displays with up to 16 display positions. The controller accepts command and data input words on a clocked serial input line. Commands control the on/off duty cycle, starting character position, and number of characters to display. Encoded data words display bargraph position (single segment or increasing bar length), numbers, comma, decimal, and selected upper and lower case letters. No external drive circuitry is required for displays that operate on 20mA of drive current up to 50V. A 64 × 16-bit segment decoder provides character set decoding for the display.

Micrel has received the rights from Rockwell International to manufacture and market this product and reproduce the specifications, including references to Rockwell.

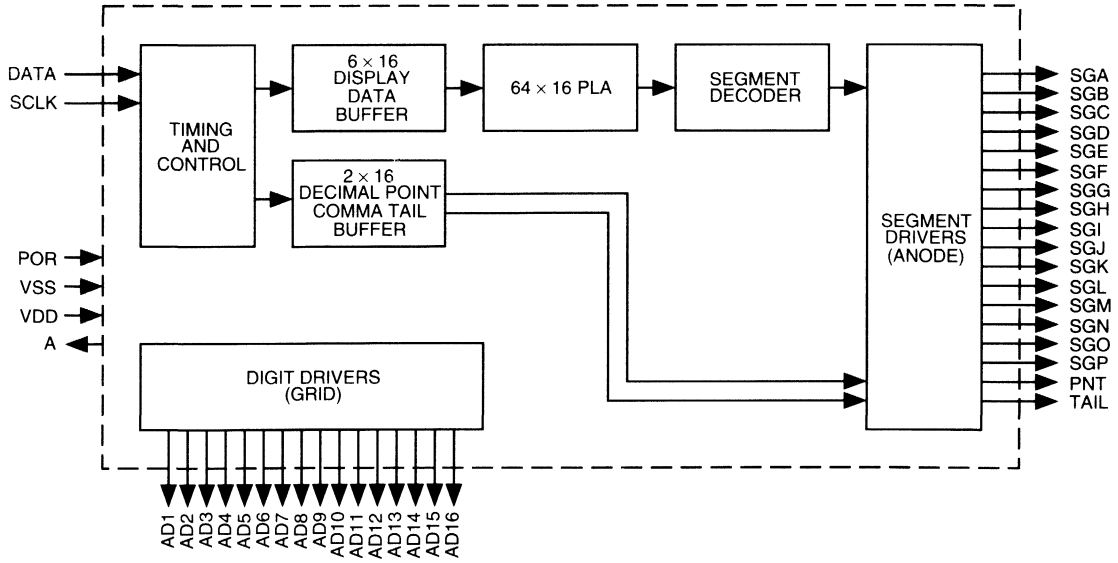
Features

- 16 segment drivers plus decimal point and comma tail drivers
- 16 digit drivers
- Up to 66kHz data rate
- Direct digit drive of 20mA for up to 50V displays
- Supports vacuum fluorescent or LED displays
- Serial data input for 8-bit display and control data words
- 64 × 16-bit PLA provides segment decoding driving
  - Any 1 of 16 bargraphs segments
  - 1 to 16 bargraph segments
  - Ten 7-segment numeric characters (0 through 9)
  - Comma and decimal
  - 8 upper and lower case 7-segment characters
- Command functions
  - Duty cycle adjust
  - Character position select
  - Number of characters
- 40-pin DIP package

Ordering Information

Part Number	Drive	Temp. Range	Package
MIC10951P-40	40V	0°C to +70°C	Plastic
MIC10951P-50	50V	0°C to +70°C	Plastic
MIC10951PE-40	40V	–40°C to +85°C	Plastic
MIC10951PE-50	50V	–40°C to +85°C	Plastic

Block Diagram



* Contact Micrel for more information.

MIC10955

V. F. Segmented Display Controller/Driver

Summary Information*

General Description

The MIC10955 Segmented Display/Driver is a MOS/LSI device capable of directly driving both the grids and anodes of multiplexed vacuum-fluorescent segmented displays. All timing circuits (including a clock generator) required to control the display drivers are contained within the device. The MIC10955 can drive segmented displays with 8 or 16 grids (characters) and 8, 16, or 24 anodes (segments). A serial interface allows for a host microprocessor to transmit commands and display data to the MIC10955 directly.

A 128 × 16-bit PLA provides coding for both 16-segment and 14-segment alphanumeric ASCII code character sets (all caps only). The PLA is divided into lower 64 and upper 64 code sets. Only one set can be selected at a time. In lower set mode the 16-segment display characters are selected. In upper set mode the 14-segment display characters are selected. The PLA can also be bypassed so that data words from the host microprocessor are loaded directly into segment drivers without decoding by the PLA. This mode is especially useful for creating special display patterns such as bar graph displays. Bypass mode is limited to eight drivers per data word.

Micrel has received the rights from Rockwell International to manufacture and market this product and reproduce the specifications, including references to Rockwell.

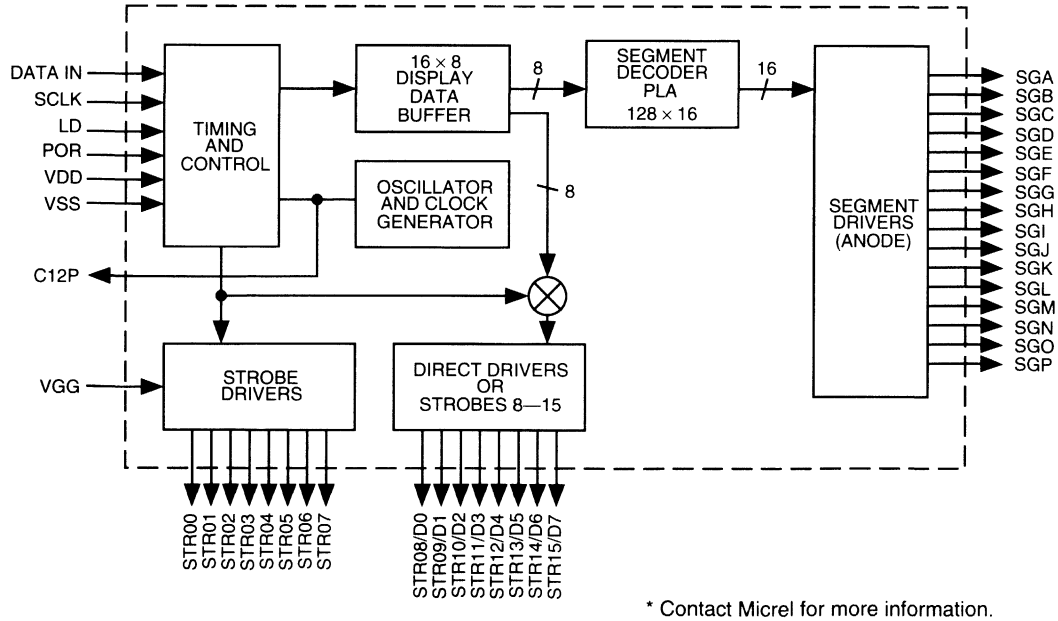
Features

- 8 or 16-character display driver
- 8, 16, or 24-segment drivers
- Average data rate 66kHz
- Single character burst rate 500kHz
- Direct digit drive of 20mA for up to 40V or 50V vacuum fluorescent serial displays
- 128 × 16-bit PLA provides 16 or 14-segment alphanumeric characters set
- Internal clock generator circuit
- Serial host interface
- PLA bypass mode
- 40-pin DIP

Ordering Information

Part Number	Drive	Temp. Range	Package
MIC10955P-40	40V	0°C to +70°C	Plastic
MIC10955P-50	50V	0°C to +70°C	Plastic
MIC10955PE-40	40V	–40°C to +85°C	Plastic
MIC10955PE-50	50V	–40°C to +85°C	Plastic

Block Diagram



* Contact Micrel for more information.

MM5450/5451

LED Display Driver

General Description

The MM5450 and MM5451 LED display drivers are monolithic MOS IC's fabricated in an N-Channel, metal-gate process. The technology produces low threshold, enhancement mode, and ion-implanted depletion mode devices. These devices are available in packaged or die form, suitable for conventional packaging, hybrid assembly or chip on board technology.

A single pin controls the LED display brightness by setting a reference current through a variable resistor connected to V_{DD}.

Applications

- Industrial control indicator
- Relay driver
- Digital clock, thermometer, counter, voltmeter
- Instrumentation readouts

Features

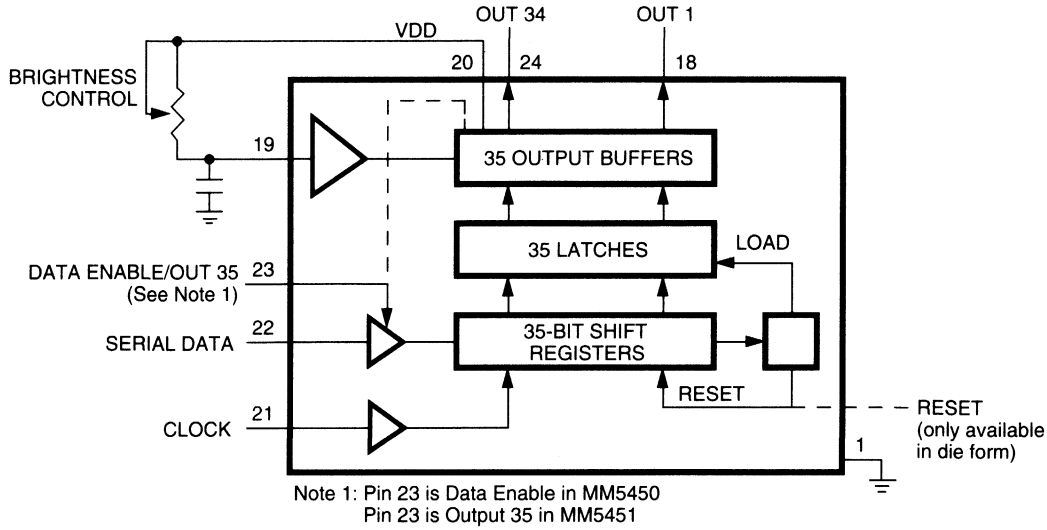
- Continuous brightness control
- Serial data input
- No load signal requirement
- Enable (on MM5450)
- Wide power supply operation
- TTL compatibility
- 34 or 35 outputs, 15 mA capability
- Alphanumeric capability
- Available in die or packaged form

Ordering Information

Part Number	Temp. Range	Package
MM5450BN	–25 to +85°C	40-pin Plastic DIP
MM5451BN	–25 to +85°C	40-pin Plastic DIP
MM5450BV	–25 to +85°C	44-pin PLCC
MM5451BV	–25 to +85°C	44-pin PLCC
MM5450/51CY	0 to +70°C	(die form)

4

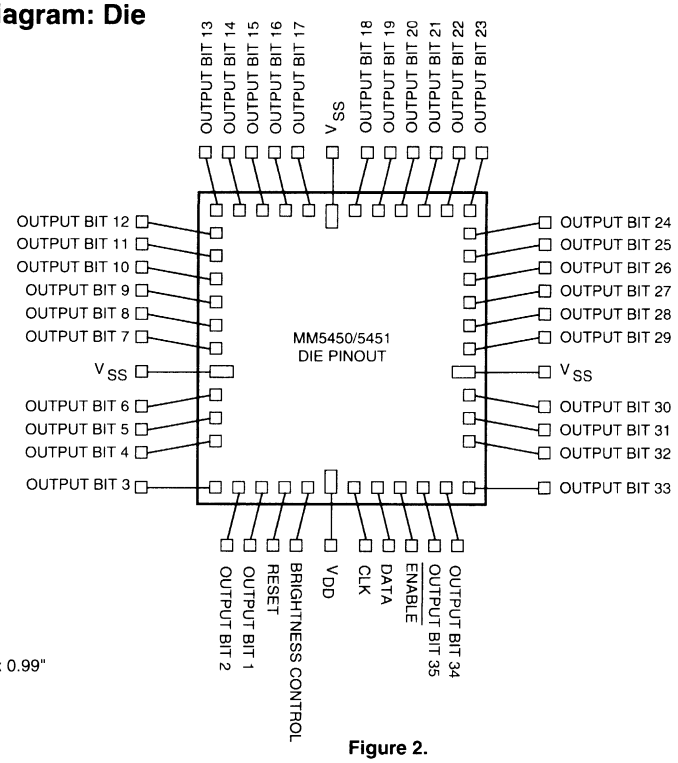
Block Diagram



Note 1: Pin 23 is Data Enable in MM5450
Pin 23 is Output 35 in MM5451

Figure 1.

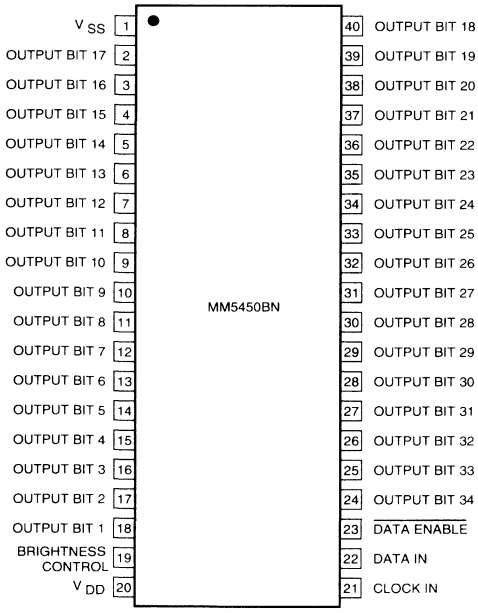
Connection Diagram: Die



Note: Die size is 0.106" x 0.99"

Figure 2.

Connection Diagram: Dual-in-line Package



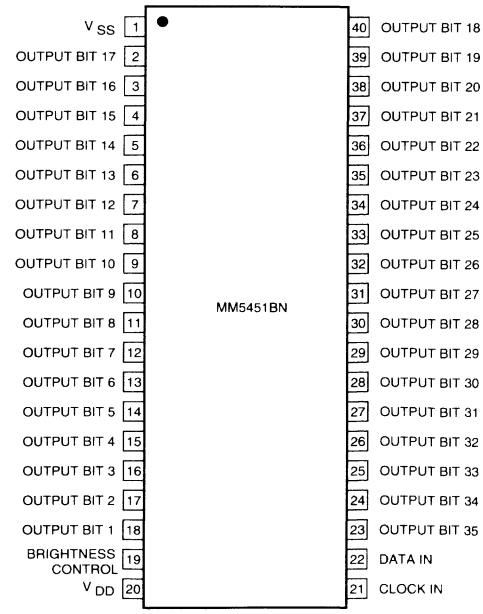


Figure 3a, 3b.

Connection Diagram: Plastic Leaded Chip Carrier

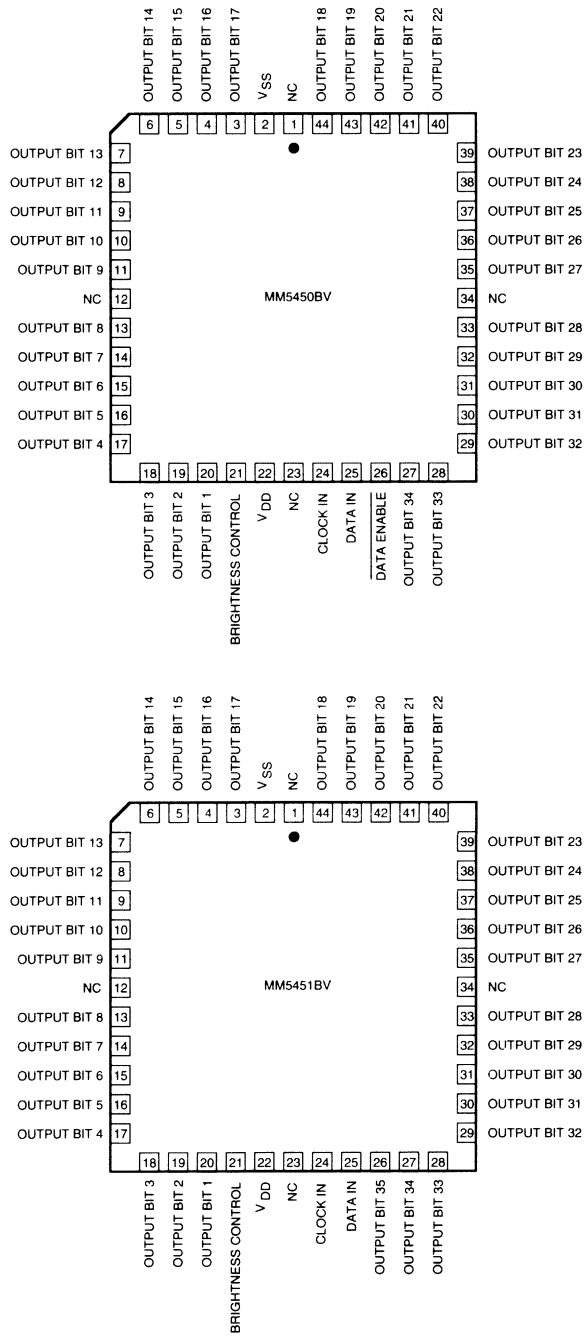


Figure 4a, 4b.

Absolute Maximum Ratings

Voltage at Any Pin	V_{SS} to V_{SS}+12V	Junction Temperature	+150°C
Operating Temperature	–25°C to +85°C	Lead Temperature (max. soldering time is 10 seconds)	300°C
Storage Temperature	–65°C to +150°C		
Power Dissipation	560 mW at +85°C 1 W at +25°C		

Electrical Characteristics

T_A within operating range, V_{DD} = 4.5 V to 11.0 V, V_{SS} = 0 V unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Power Supply		4.75		11	V
Power Supply Current	Excluding Output Loads			8.5	mA
Input Voltages					
Logical "0" Level (V_L)	±10 µA Input Bias	–0.3		0.8	V
Logical "1" Level (V_H)	4.75 ≤ V_{DD} ≤5.25	2.2		V_{DD}	V
	V_{DD} > 5.25	V_{DD} – 2		V_{DD}	V
Brightness Input (Note 2)		0		0.75	mA
Output Sink Current					
Segment OFF	V_{OUT} = 3.0 V			10	µA
Segment ON	V_{OUT} = 1.0 V (Note 3)	0		15	mA
	Brightness Input = 0 µA	0		10	µA
	Brightness Input = 100 µA	2.0	2.7	4	mA
	Brightness Input = 750 µA	15		25	mA
Brightness Input Voltage (Pin 19)	Input Current = 750 µA	3.0		4.3	V
Output Matching (Note 1)				±20	%
Clock input	(Notes 5 and 6)				
Frequency, f_C				500	kHz
High Time, t_H		950			ns
Low Time, t_L		950			ns
Data Input					
Set-Up Time, t_{DS}		300			ns
Hold Time, t_{DH}		300			ns
Data Enable Input Set-up Time, t_{DES}		100			ns
Reset Pad Current (Die Version)		8			µA

Note 1: Output matching is calculated as the percent variation (I_{MAX} + I_{MIN}) / 2.

Note 2: With a fixed resistor on the brightness input pin, some variation in brightness will occur from one device to another. Maximum brightness input current can be 2 mA as long as Note 3 and junction temperature equation are complied with.

Note 3: See Figures 7, 8 and 9 for Recommended Operating Conditions and limits. Absolute maximum for each output should be limited to 40 mA.

Note 4: The V_{OUT} voltage should be regulated by the user. See Figures 8 and 9 for allowable V_{OUT} vs. I_{OUT} operation.

Note 5: AC input waveform specification for test purpose: t_r ≤ 20 ns, t_f ≤ 20 ns, f = 500 kHz, 50% ±10% duty cycle.

Note 6: Clock input rise and fall times must not exceed 300 ns.

Functional Description

The MM5450 and MM5451 were designed to drive either 4 or 5 digit alphanumeric LED displays with the added benefit of requiring minimal interface with the display or data source.

Data is transferred serially via 2 signals; clock and serial data. Data transfer without the added inconvenience of an external load signal is accomplished by using a format of a leading "1" followed by the allowed 35 data bits. These 35 data bits are latched after the 36th has been transferred. This scheme provides non multiplexed, direct drive to the LED display. Characters currently displayed (thus, data output) changes only if the serial data bits differ from those previously transferred.

Control of the output current for LED displays provides for the display brightness. To prevent oscillations, a 1nF capacitor should be connected to pin 19, brightness control.

The block diagram is shown in Figure 1. For the MIC5450, the DATA ENABLE is a metal option and is used instead of the 35th output. The output current is typically 20 times greater that the current into pin 19, which is set by an external variable resistor. There is an external reset connection shown which is available on unpackaged (die) units only.

Figure 2 illustrates the die "pinout", or pad location for bonding in "chip on board" applications.

Figure 5 shows the input data format. A leading "1" is followed by 35 bits of data. After the 36th had been transferred, a LOAD signal is generated synchronously with the clock high state. This loads the 35 bits of data into the latches. The low side of the clock is used to generate a RESET signal which clears all shift registers for the next set of data. All shift registers are static master-slave, with no clear for the master portion of the first register, allowing continuous operation.

There must be a complete set of 36 clocks or the shift registers will not clear.

When the chip first powers ON an internal power ON reset signal is generated which resets all registers and all latches. The START bit and the first clock return the chip to its normal operation.

Figure 3 and 4 show the pin-out of the MIC5450 and MIC5451. Bit 1 is the first bit following the start bit and it will appear on pin 18. A logical "1" at the input will turn on the appropriate LED.

Figure 5 shows the timing relationships between data, clock and DATA ENABLE. A max clock frequency of 0.5 MHz is assumed.

For applications where a lesser number of outputs are used, it is possible to either increase the current per output, or operate the part at higher than 1V V_{OUT}. The following equation can be used for calculations.

$$T_j = (V_{OUT})\,(I_{LED})\,(\text{No. of segments})\,(124°C/W) + T_A$$

where:

T_j = junction temperature + 150°C max

V_{OUT} = the voltage at the LED driver outputs

I_{LED} = the LED current

124°C/W = thermal resistance of the package

T_A = ambient temperature

The above equation was used to plot Figures 7–9.

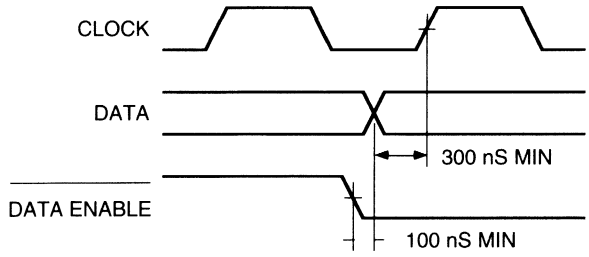


Figure 5.

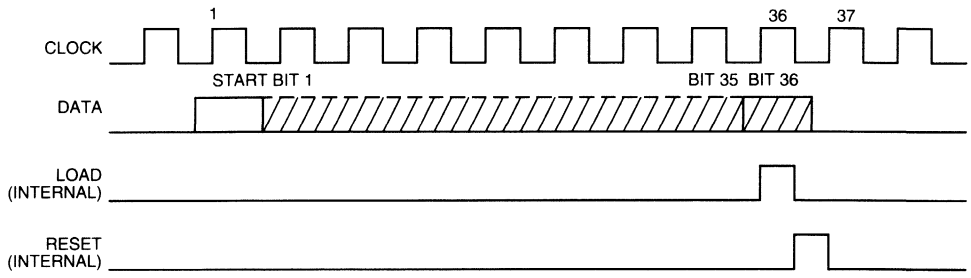


Figure 6. Input Data Format

Typical Performance Characteristics

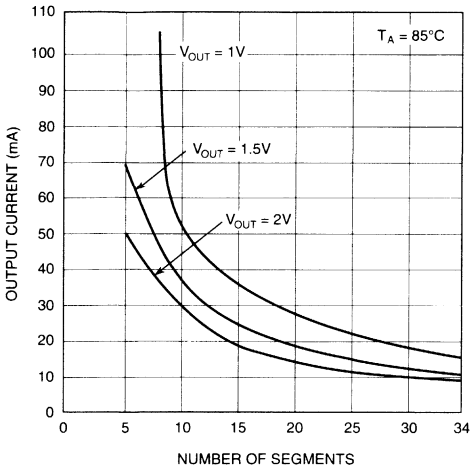


Figure 7.

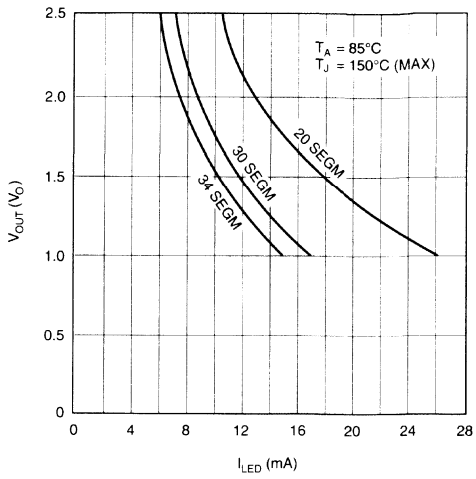


Figure 8.

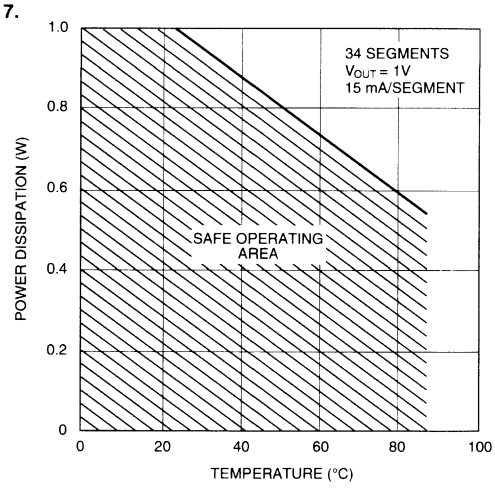


Figure 9.

Typical Applications

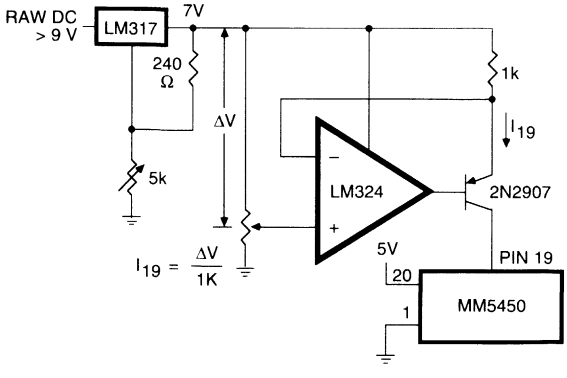


Figure 10. Typical Application of Constant Current Brightness Control

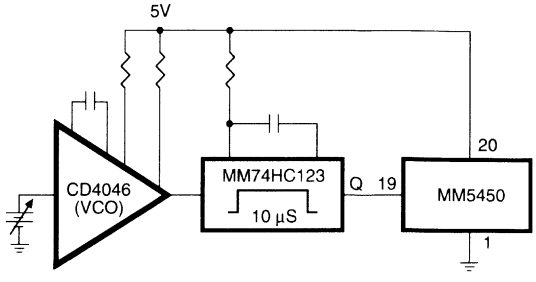


Figure 11. Brightness Control Varying the Duty Cycle

Typical Applications

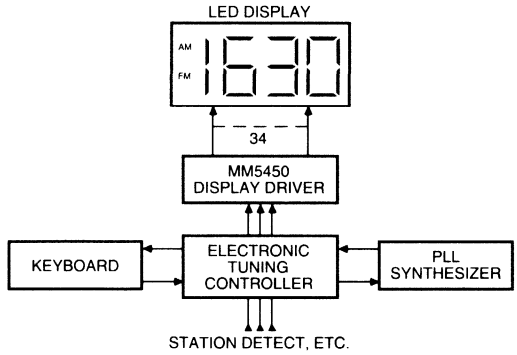


Figure 12. Basic Electronically Tuned Radio System

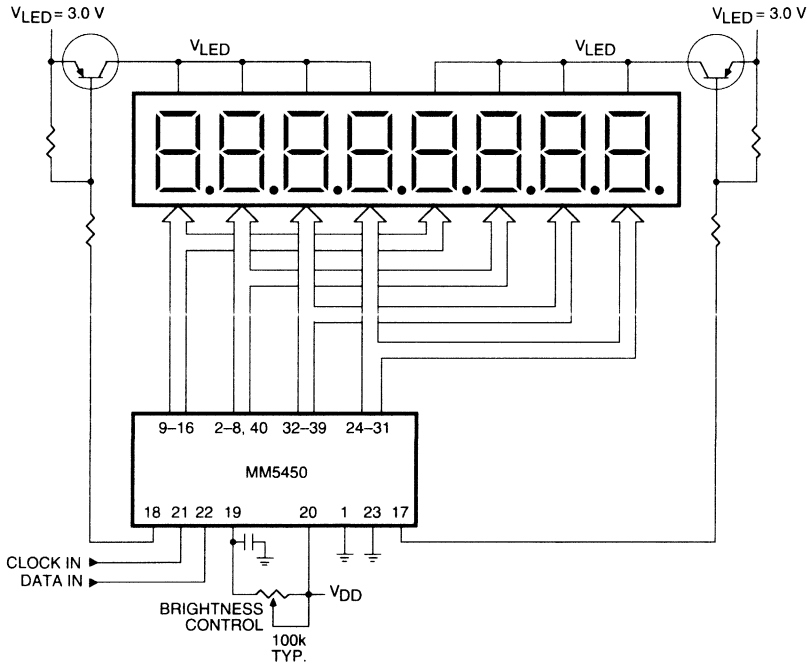


Figure 13. Duplexing 8 Digits with One MM5450.

Application Note 7

Six Decade Counter/Display Totalizer

Introduction

The Micrel MIC50395 was developed to provide counting system for most needs. This device consists of six, synchronous, up down decade counters with a data store and an auxiliary storage register that may be compared with the counter value. The circuit is relatively insensitive to power supply variation, and can interface with CMOS logic using power supplies in the 10 to 15 volt range. Counting speeds up to 1.0MHz are permissable and the circuits are readily cascaded.

The MIC50395 uses positive logic, i.e., logic 1 is the more positive level in the following description:

DESCRIPTION OF OPERATION

COUNTER

The positive going edges of a pulse train at the COUNT input (pin 36) are standardized by an internal monostable to a fixed pulse width thereby giving only a minimum value to the time for which the input pulse must stay high. This pulse is applied synchronously to the six decades and if the UP/DOWN input is a logic 1 the counters will be incremented, if at logic 0 then the counters will be decremented. At any time the value in the counter will be set back to zero if the CLEAR COUNTER input goes to a logic 1 for 2μs or longer. This resetting action occurs whether or not there is a counting input pulse train by forcing the counters directly to 0.

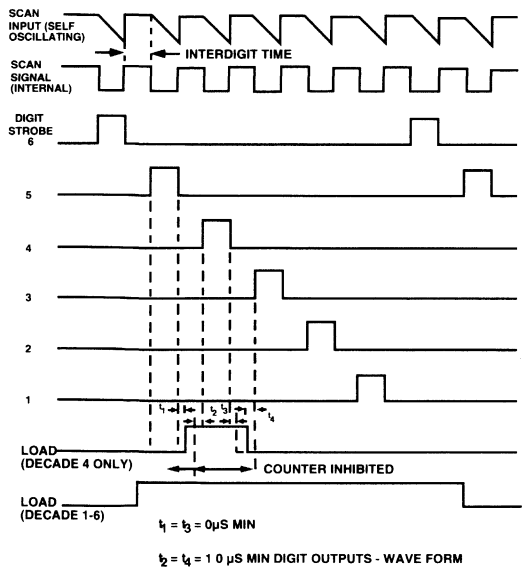


Figure 1: Load Counter, Register Timing

In addition to resetting it is also possible to preset any desired value into the counter. This is done sequentially decade by decade, under control of the LOAD COUNTER command in the following manner. If LOAD COUNTER is taken to logic one a minimum of 2μs prior to the positive transition of the digit output of the digit being loaded, the chip will latch this command and the BCD data presented to the counter will be loaded upon the negative transition of the digit strobe. It is thus possible to load each of the 6 counters individually if required. While the counter is being loaded the counting input is inhibited. Internally the load counter command is synchronized to the scan oscillator. Thus if LOAD COUNTER is brought to a logic zero in the middle of a digit strobe, the counter will remain inhibited until the next interdigit blanking time. A separate COUNT INHIBIT control is provided to stop the applied count inputs from being accepted while this signal is a logic 1.

The counter section has two control outputs, a CARRY from the most significant decade and a ZERO SIGNAL that indicates when the counter contents are zero. These signals are suppressed during LOAD COUNTER operations to avoid a spurious output being given during a counter presetting operation.

COMPARISON AND REGISTER

The six digit storage register may be preset to any value by bringing the LOAD REGISTER signal to logic 1. The presetting sequence is exactly the same as for the counter. The value on the REGISTER BCD INPUTS being loaded decade by decade by the six digit signals in the order "most significant" (digit 6) to "least significant" (digit 1). The outputs of this register are compared continuously with the value currently in the counter; this comparison is made in parallel and not decade by decade. When the two values are the same an EQUAL signal is given, however, during presetting of either the counter or the register, the CARRY, ZERO and EQUAL signals are inhibited so that no false intermediate comparison result is given. Since the counter and the register have separate BCD inputs, both may be preset simultaneously if desired. The value held in the register can only be altered by the BCD inputs. The Count Input is not inhibited during load register operations.

DIGIT SCANNING AND OUTPUT FUNCTIONS

The digit scan counter is timed from an internal oscillator which may be driven externally from the SCAN input. A capacitor attached from V_{SS} to this pin will determine the scan frequency when an external logic drive to this pin is not used. Internal circuitry gives a fixed delay to the DIGIT OUTPUT

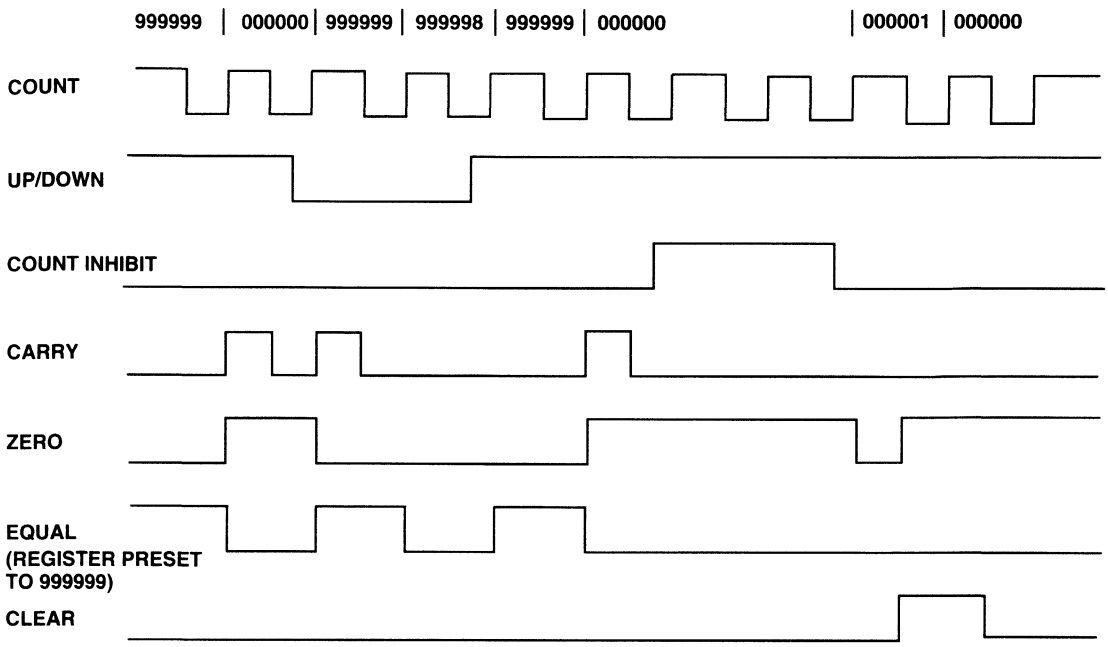


Figure 2: Up/Down Count Timing

signal to ensure that there is a gap between each digit strobe, thus a "ghosting" effect in a displayed output due to the storage time of external display driver transistors is eliminated. This is the interdigit blanking time. Typically this time can range from 3 to 10μs. SET input is used to force the digit strobe counter to the digit 6 position for purposes of synchronizing the counter output. The digit counter outputs are gated by the interdigit blanking period and appear as DIGIT STROBE OUTPUTS. The counter outputs are not directly multiplexed but are buffered by a 6 digit latch controlled by the STORE command. The outputs of the latch go directly to the output multiplexer, thus when the STORE signal is at logic 0 the counter contents are directly available, but as soon as STORE goes to logic 1 the value present as the signal changed is retained and subsequent changes in counter value are ignored. The contents of the store are read out, digit by digit — the scan counter again performs this function in the order most significant to least significant — and appear on BCD OUT pins. The four bits in each BCD digit are encoded simultaneously to seven segment code and appear as SEGMENTS OUT and can be used to drive a suitable 7 segment display. The $\overline{SET}$ operation will also turn off these seven outputs, blanking the display, as well as setting the digit counter to digit 6. This is to prevent possible destruction of an LED type display when $\overline{SET}$ is a prolonged signal. Frequently it is required to display only significant numbers, in which case taking the LZB control to a logic 0 will blank the leading zeros in the seven segment output.

INTERFACING WITH THE MIC50395

The wide range of power supply, 10.0 to 15.0V, makes the counting system particularly suitable for interfacing with CMOS logic.

A. Segment output — these transistors can source 10mA from the V_{SS} supply, there is no internal pull down to V_{DD} when the transistor is turned off. These transistors are capable of driving small LED displays directly via series resistors.

B. Digit outputs — a push pull configuration is used here as the most suitable arrangement for driving both external logic and display drivers. These outputs supply 3.0mA max from V_{SS} and sink 30μA to V_{DD}.

When higher power displays are used the segment outputs should be buffered by an emitter follower in order to provide the extra current.

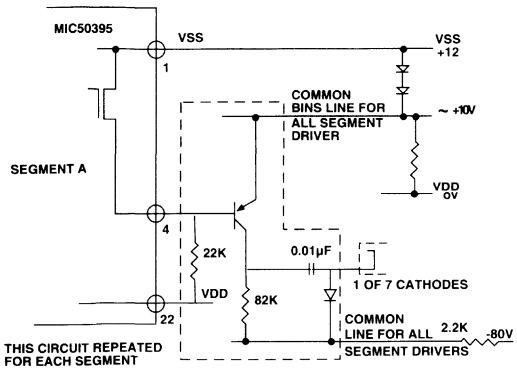


Figure 3: Segment Driver

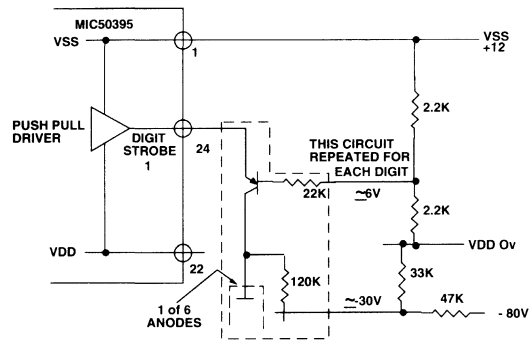


Figure 4: Digit Driver

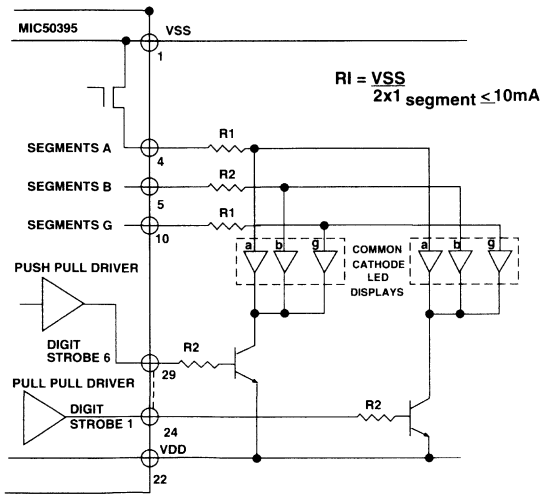
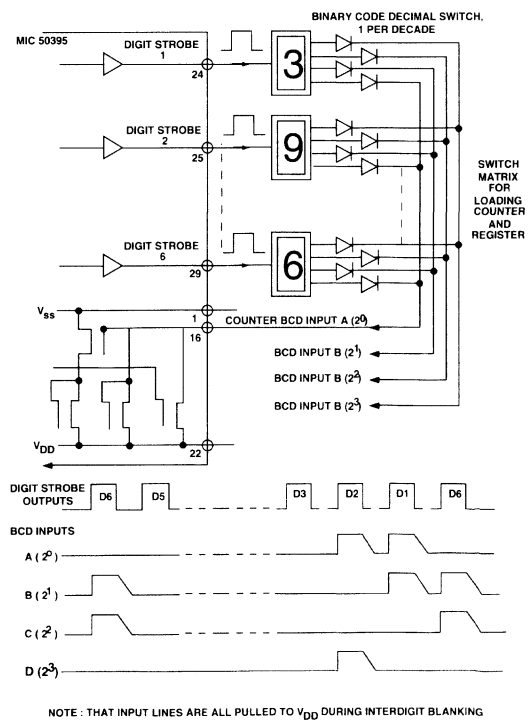


Figure 5: Driving LED Displays Directly

The BCD OUTPUTS, EQUAL, ZERO and CARRY are also push-pull. Output drive capabilities are listed in the following table:

	V_{OL}	V_{OH}
Segment Output (Pins 4-10)		V_{SS} – 3V at 10 mA (average over one digit cycle)
Digit Outputs (Pins 24 - 29)	V_{DD} at no load 0.2 V_{SS} at 30 µA	V_{SS} – 2V at 3.0 mA
Equal/Zero/Carry (Pins 23, 39,38)	V_{DD} at no load 0.2 V_{SS} at 30 µA	V_{SS} – 2V at 1.5 mA

The following inputs, COUNT, STORE, UP/DOWN, COUNT INHIBIT, CLEAR, LZB, and LOAD REGISTER have no internal current sources and must therefore be driven from sources that give correct logic 1 and 0 levels—open collector circuits, or switches without pull down resistors for example, may not be used. If any of the above functions are not required then those pins should be tied to the appropriate supply, that is to V_{SS} for logic 1 and V_{DD} for logic 0. SET has an internal transistor that pulls the pin to V_{SS}, if unconnected, thus the driving circuit should be able to sink this current, approximately 60µA, when pulling the input to logic 0. The COUNTER BCD and REGISTER BCD inputs have two internal transistors, one static and one switched as a precharge, that pull to



NOTE : THAT INPUT LINES ARE ALL PULLED TO V_{DD} DURING INTERDIGIT BLANKING

Figure 6: BCD Switch Matrix

V_{DD}. The static current is < 350µA to V_{DD} when the input is taken to Vss: the dynamic current from V_{SS} is 1mA while the transistor is on. The dynamic precharge ensures that even with the large capacitive loading and leakage current of a switch matrix at these pins, the correct data will be entered at the maximum digit scan frequency.

An example of a switch matrix input illustrates this operation. Six binary coded decimal switches are used, one for each decade, the switches being enabled by the corresponding DIGIT STROBE output, with the paralleled switch outputs connected to the COUNTER (or REGISTER) BCD inputs. The DIGIT STROBE outputs are separated by the interdigit blanking time and it is only during this time that the precharge transistors at the BCD inputs are all pulled to logic 0 (V_{DD}). After this blanking time the next DIGIT STROBE output will in its turn switch to logic 1 (only one out of six is ever on) and pull those BCD inputs selected by the switch and diode matrix to

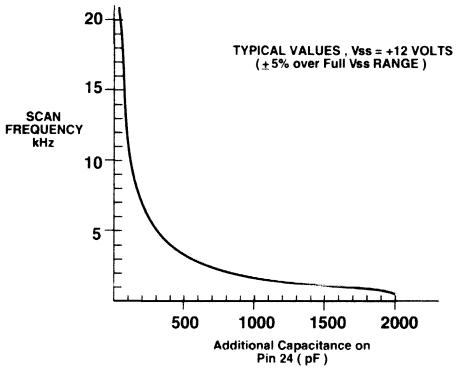


Figure 7: Scan Frequency vs. External

logic 1. This value is loaded into the corresponding register or counter stage, i.e. the switch matrix driven by DIGIT STROBE 6 will be loaded into MSB of the register or counter. As the DIGIT STROBE switches back to logic 0 the next interdigit blanking time begins and the inputs are all pulled back to logic 0 again by the internal precharge. It is possible for the DIGIT STROBE outputs to drive both the switch matrix and a display. If the COUNTER & REGISTER BCD inputs are connected in parallel they may still be driven directly from the DIGIT STROBE outputs.

When the scan oscillator is free running the SCAN input may use an external capacitor to set the scanning frequency to a particular value. The signal seen at the pin is a ramp determined by the capacitance, followed by a period clamped at V_{SS}. This period clamped at V_{SS} is determined by the internal oscillator and is the interd igit blanking period. During this time the DIGIT STROBE outputs are all turned off.

When the SCAN input is driven externally this fixed interdigit period remains plus the time at which the synchronizing signal is at logic 0. Making the interdigit blanking time independent of the external synchronizing signal requires only the addition of a resistor and capacitor.

Time A is the interdigit blanking time, time B should be greater than 2µs—a range of 2 to 5µs is suitable and time C may be from infinity to 30µs. If time C is made too short then the interdigit blanking circuit never resets itself and will stay at logic 0 and no DIGIT STROBE outputs will appear.

TYPICAL MIC50395 APPLICATIONS

BATCH CONTROL

In many situations involving the metering of material, whether as a liquid, individual items or revolutions of a spindle, a two step operation is required for better efficiency. The flow is started at the maximum speed and at a preset point before the end of the operation a signal is required to slow down and eventually stop the equipment. Such applications could be as diverse as filling sacks with cement or controlling the turns on a transformer bobbin. A block diagram of such a system is presented. Pressing the start switch allows the input to the D flip flop to go to logic 1. This is clocked by the DIGIT STROBE 6 so that a synchronous signal at least one complete scan counter cycle long is obtained. This signal is used as LOAD COUNTER and LOAD REGISTER, the two controls being tied in parallel for simultaneous loading. It does not matter how long the load signal is as long as it is at least one scan cycle long and changes synchronously with the scan signal. The two values representing total quantity and "slow down"

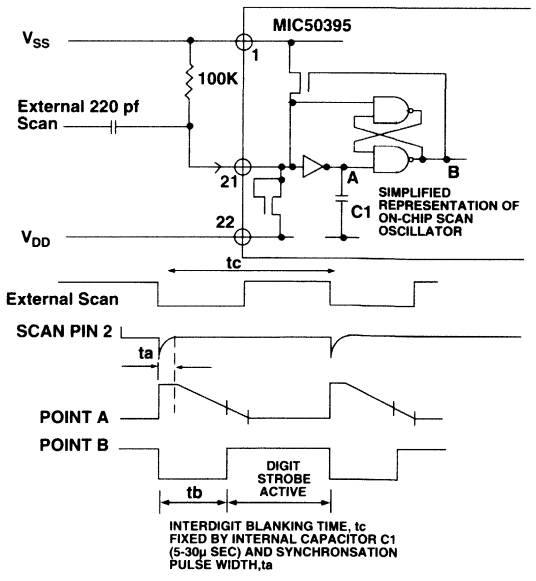


Figure 8: External Drive To Scan Input

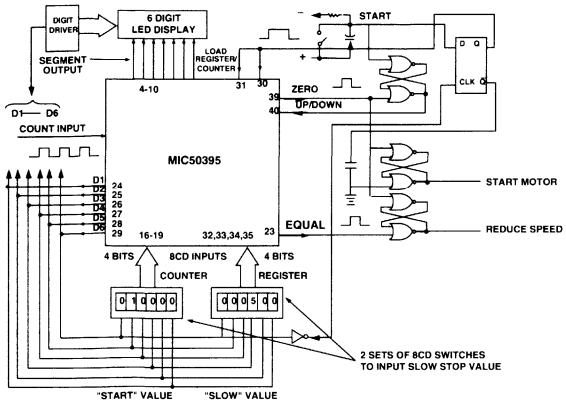


Figure 9: Batch Control

quantity are set on the digit switches and these values are loaded at the beginning of each cycle. Once the counter register loading is complete, a start signal is generated to set the equipment in operation. The train of pulses representing the measured quantity is counted, the UP/ DOWN control is in the down mode. Thus with two quantities at, for example, 10,000 and 500, the counter starts off with 10,000 loaded and counts toward zero. When the counter reaches 500 an EQUAL signal is generated and this sets the signal controlling the brake. A further 500 pulses and the counter reaches zero, an output on the ZERO pin resets the start flip flop and the equipment is brought to reset awaiting a new start signal. In such an operation the display outputs would probably not be used.

This application can be extended by using the ZERO output to control the UP/DOWN input. The operation is identical but the start signal also sets a latch into the count down state. As ZERO is detected this latch is reset so that the counter mode is now up. Even with a braking facility there may be an "overrun" and the value now held in the counter and displayed is the extra quantity. The operator may now decide if this extra quantity is within the tolerance allowed for the job and to take whatever action is necessary.

POSITIONAL MEASUREMENT

Positional measurement can readily be made using this circuit, the six decades gives considerable accuracy in one package. The two quadrature signals from a graticule type displacement measurement system must be converted to

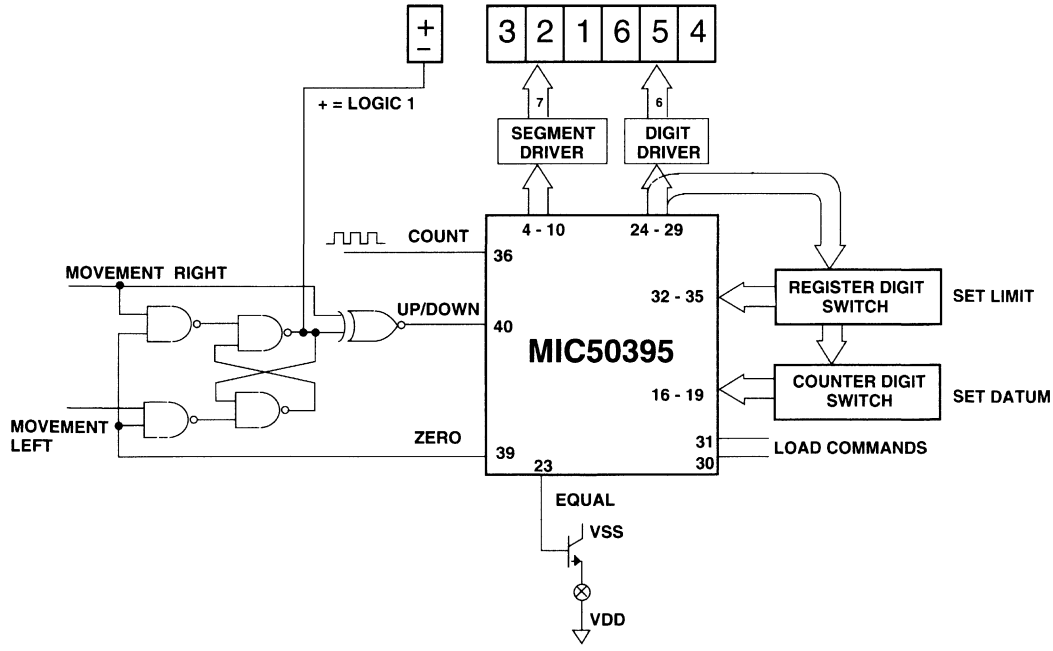


Figure 10: Positional Measurement

count impulses and an UP/DOWN signal. If the measurement zero datum is in the middle of the measurement area then the following counting conditions arise:

Direction of Movement	Displayed sign + or – Of Datum	Count Direction	
RIGHT	–	DOWN	ZERO DATUM CROSSED
RIGHT	+	UP	
LEFT	+	DOWN	ZERO DATUM CROSSED
LEFT	–	UP	

COUNT edge (Fig. 2) that ZERO has as much longer propagation delay than the EQUAL output. In the event that the register is not used it may be loaded with zeros—by giving a LOAD REGISTER command with the BCD inputs as zero — and the EQUAL output then used as zero detect. This has the advantage of increasing the system speed for although the counter can accept inputs up to 1.0MHz; the propagation delay of the outputs is too long to allow a control signal to be changed between clock pulses at this counting rate. In this example UP/DOWN has to be controlled and using the faster output enables a higher counting speed to be used; if necessary in this case, approximately 600kHz instead of 300kHz.

GREATER THAN—LESS THAN DETECTION

The availability of an EQUAL output facilitates the generation of greater than and less than signals. The only requirement is the circuit is set into the correct initial state. When the counter has the same value as the register, the generation of the "greater/less than" signal depends on the direction of count, i.e. from this EQUAL condition count up gives "greater than" and count down gives "less than". EQUAL is gated with UP and with DOWN and these are connected to the D inputs of two D flip flops that are both clocked by the counting pulse. As EQUAL is reached, the two flip flops are reset, but the next count pulse after the EQUAL condition will set one or the other flip flop, and thereby provide the appropriate signal.

AUTOMATIC STOP

The COUNT INHIBIT input may be used to stop the counter automatically when the EQUAL or ZERO outputs are connected directly to this input. As EQUAL, for example, goes to a logic 1, then further counting is inhibited when this signal is connected directly to COUNT INHIBIT. Since no more count inputs are accepted, the EQUAL value remains and blocks the counting action. The operation of CLEAR, LOAD REGISTER or LOAD COUNTER can be used to start the system counting again.

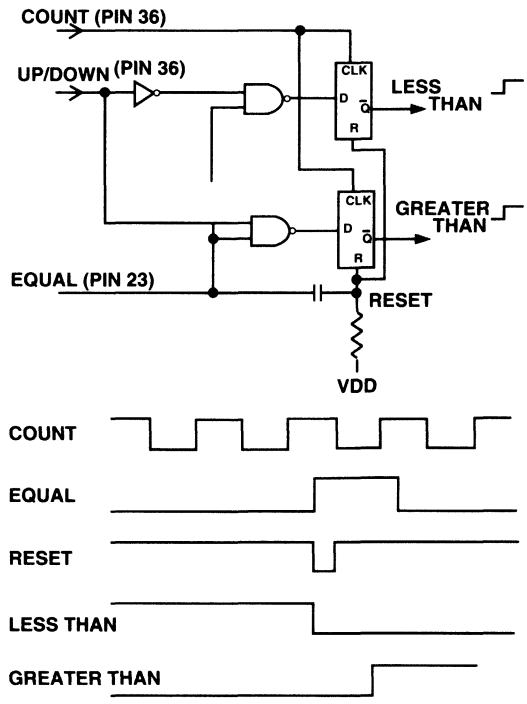


Figure 11: Less Than Greater Than

4

MIC8030/MIC8031 Application Hints on Compatibility with Display Drivers Produced by AMI and HOLT

The MIC8030/MIC8031 can be made compatible with all bonding options of the Gould-AMI S4520 as well as all bonding options of the HOLT HI-8010. However, the high voltage supply must be positive with respect to ground for the MIC8030/MIC8031. Both AMI and HOLT use a negative High Voltage. See MIC8010/11/12/13 family for drop in replacements in existing sockets.

High Voltage Supply

Device	Vmin	Vmax	Absolute Max
MIC8031	20V	100V	110V
MIC8030	20V	50V	75V
HI-8010	Vlogic-35V	+0.3V	Vlogic-35V
S4520	Vlogic-32V	+0.3V	Vlogic-32V

Logic Power Supply

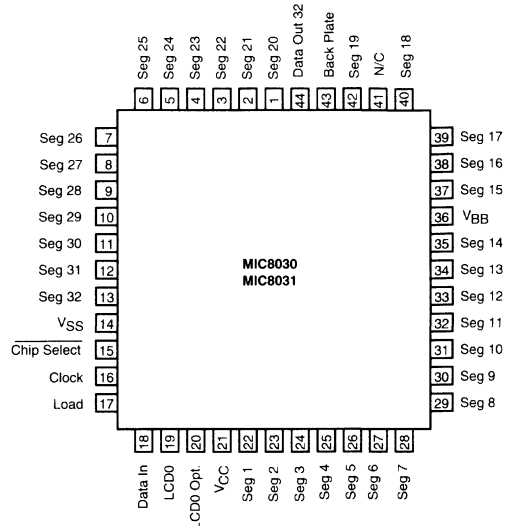
Device	Vmin	Vmax	Absolute Max
MIC8031	4.5V	16.5V	18V
MIC8030	4.5V	5.5V	18V
HI-8010	3.0V	18.0V	18V
S4520	3.0V	16.0V	17V

As can been seen above, the MIC8030/MIC8031 are superior to both AMI and HOLT in the voltage that can be applied to a Dichroic LCD display. Using the MIC8030/MIC8031 allows for a derating of 50%/70% if operated at 35V; the HI-8010 allows for no derating at 35V and the S4520 allows for no derating at 32V.

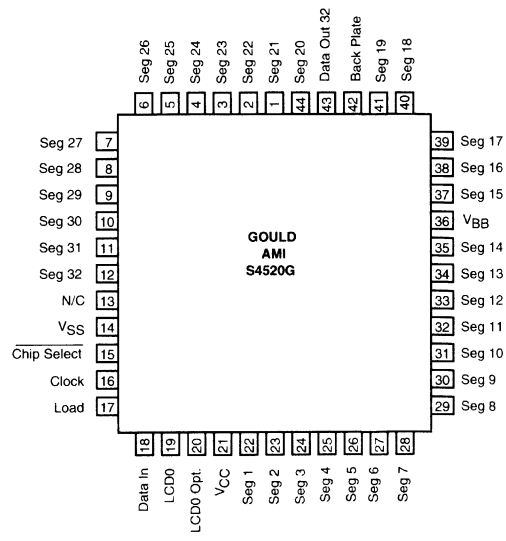
When placing the MIC8030/MIC8031 in a pin compatible configuration on a board which previously used a HOLT or AMI device, care must be taken before changing the polarity of the High Voltage Supply, to reverse the direction of any polarized filter capacitor on the High Voltage line, as well check any other circuit (like a zener diode, etc) which contacts the High Voltage line.

The pin out drawings match the MIC8030/MIC8031 to the S4520. By moving the No-Connect, from pin 41 to pin 13 and shifting the displaced signals clockwise, the pin out can be matched.

Other pin outs that can be matched are the S4520A, S4520B, S4520C, S4520S, S4520F, S4520G, HI-8010L5, HI-8010L6, HI-8010L7, HI-8010C5, HI-8010C6, and the HI-8010C7. Other packaging options are available, all options must use a positive V_{BB}.



MIC8030/MIC8031
Standard 44 Pin Quad Package



S4520G
AMI 44 Pin Quad Package

High Voltage Semicustom Power Array

SECTION 5: HIGH VOLTAGE SEMICUSTOM POWER ARRAY

MPD8020

CMOS/DMOS SEMICUSTOM

HIGH VOLTAGE ARRAY

CONCEPT

The MPD8020 is a monolithic I.C. semiconductor array of low voltage CMOS analog and digital circuits on the same chip with high voltage DMOS power transistors. For quick turnaround time, wafers are held at the last step (metalization) where the customer's specific metal interconnect pattern makes each wafer run into thousands of custom I.C.'s. These smart power ASIC's (Application Specific I.C.'s) cast in silicon the proprietary advantages of the customer's design even for moderate volume applications, and give the customer a size, reliability and performance advantage over the competition!

GENERAL DESCRIPTION

The MPD8020 CMOS/DMOS Semicustom High Voltage Array uses **Micrel's** proprietary process to combine TTL/CMOS compatible high speed CMOS logic, CMOS analog, and high voltage DMOS power drive circuits on the same monolithic I.C. A single +5 Volt to +15 Volt supply powers the logic and analog circuitry while the high voltage portion functions at voltages of from +20 Volts to +100 Volts. An optional internal voltage pump with the help of two external components generates an extra voltage such that the high side gates of the power N-channel DMOS FET's are driven approximately 15 Volts above the +100 Volt supply allowing rail-to-rail high voltage switching.

The MPD8020 in combination with **Micrel's** CAD systems, CAE simulations (SPICE, HILO, TIMVER, etc.) and an experienced fab and test group give a design engineer a highly versatile means of taking a circuit idea from concept to packaged silicon.

AVAILABLE IN:

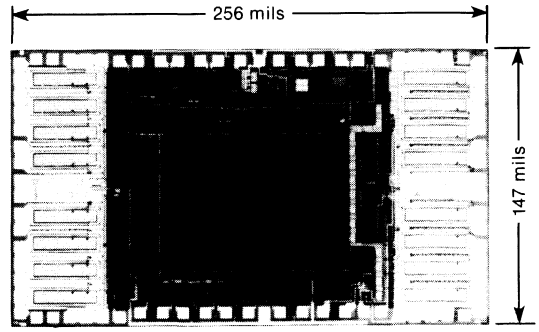
- Chip Form
- 16 to 48 pin plastic DIP's
- 16 to 48 pin ceramic DIP's
- Ceramic LCC's
- Surface mount packages
- PLCC
- Fused lead PLCC and DIP's
- Custom packages

FEATURES

- 16 N-Channel DMOS power FET's (fully floating sources, gates and drains), each 100 V, 200 mA, and 10 ohms.
- DMOS can be paralleled for 100 V, 3.2 Amp, 0.625 ohm single, half bridge, full bridge or bilateral switches.
- 200 CMOS gates in an uncommitted gate array.
- 12 TTL/CMOS I/O buffers.
- 3 op amp / comparator / Schmitt Triggers.
- 1 unity gain analog buffer.
- Bandgap reference (1.25 V / 2.5 V).
- Overtemperature sensor.
- Voltage pump (drives high side gates above V_{dd}).
- 16 medium current sink pre-drivers.
- 16 high voltage level-shifting high side pre-drivers.
- Separate analog and digital ground (V_{ss}) pads.
- Numerous logic I/O, high voltage I/O, V_{cc} and V_{dd} pads.
- Miscellaneous resistors, capacitors, and a zener.
- Available to military temperature range specifications.
- Selection of military, commercial, and power packages.

APPLICATIONS

- Switching regulators
- Motor control
- Bilateral analog switching
- High voltage switching
- Relay and solenoid driver
- Smart switch with bus decode
- Half or full bridge driver
- 3 phase driver
- Lamp driver
- Differential line driver
- Automotive switching
- Printer solenoid driver
- High voltage display driver



MPD8020 CMOS/DMOS/Bipolar Semicustom Array

Protected under Patent Numbers: #4,951,101; #4,979,001

MPD8020 MACRO CELL MENU

- 16 fully floating 100 V, 200 mA, 10 ohm Vertical-DMOS FET's
- 16 high voltage 100 V P and N channel level shifters (made up of 32 cross coupled 20 to 50 mA P & N channel pairs)
- 200 CMOS gates in an uncommitted gate array
  - — over 30 pre-designed logic "templates" of shift registers, decoders, flip-flops, NAND gates, NOR gates, etc.
  - — general purpose op amps, comparators and Schmitt Triggers, implemented in the gate array
- 12 TTL/CMOS I/O buffers
- 16 logic predrivers (with logic enable) for bottom side DMOS drive
- 3 configurable op amp / comparator / Schmitt Trigger cells which can be hooked-up as:
  - — ground sensing or V_{CC} sensing amplifiers or comparators
  - — folded cascode high performance amplifiers
  - — NPN input amplifiers
  - — programmable bandwidth / power consumption amplifiers
- A unity gain buffer with adaptive bias (to drive large loads with minimum quiescent current)
- A bandgap reference with a 1.25 V output plus multiple programmable outputs up to V_{CC}
- An over-temperature protection circuit with programmable temperature trip points and hysteresis
- A master bias programming circuit for all the linears
- A high voltage V++ "doubler" for N-channel gate drive above the +100 V V_{dd} rail
- A low voltage (V_{CC}) pass regulator to drive a local low voltage analog and digital power supply from the high voltage supply
- Multiple current mirrors both at high (100 V) and low (15 V) levels
- Floating zener clamps, avalanche zeners, references and Schottky diodes
- Diffusion, diffusion P-well, pinched and poly resistors
- 40 picofarads of on-chip capacitance
- Isolated PNP and NPN transistors

What MICREL Supplies with the MPD8020

- MPD8020 CMOS/DMOS Semicustom High Voltage Array Data Sheet
- MPD8020 Kit Part #1, Analog SSI and MSI Circuits
  - — Kit parts in a 40 pin DIP with eleven commonly used analog circuits
  - — Kit Part #1 data sheet with specifications and application hints
- MPD8020 Kit Part #2, Digital SSI and MSI Circuits
  - — Kit parts in a 40 pin DIP with eight revealing digital circuits for checking speed and digital timing characteristics (also some analog circuits implemented in the gate array)
  - — Kit Part #2 data sheet with specifications and application hints
- Highly experienced design and applications engineers on call to discuss how to optimize putting a complex analog, digital, and power circuit on one I.C.

What MICREL Needs from You — the Designer

- System block diagram with basic I/O specifications, or
- Schematic of circuit implemented with analog, digital and discrete power transistors plus the I/O specifications, or
- Breadboard using our kit parts plus "glue" logic and I/O specifications, or
- Spice and Hi-Low netlists or any other compatible computer generated description and I/O specifications.

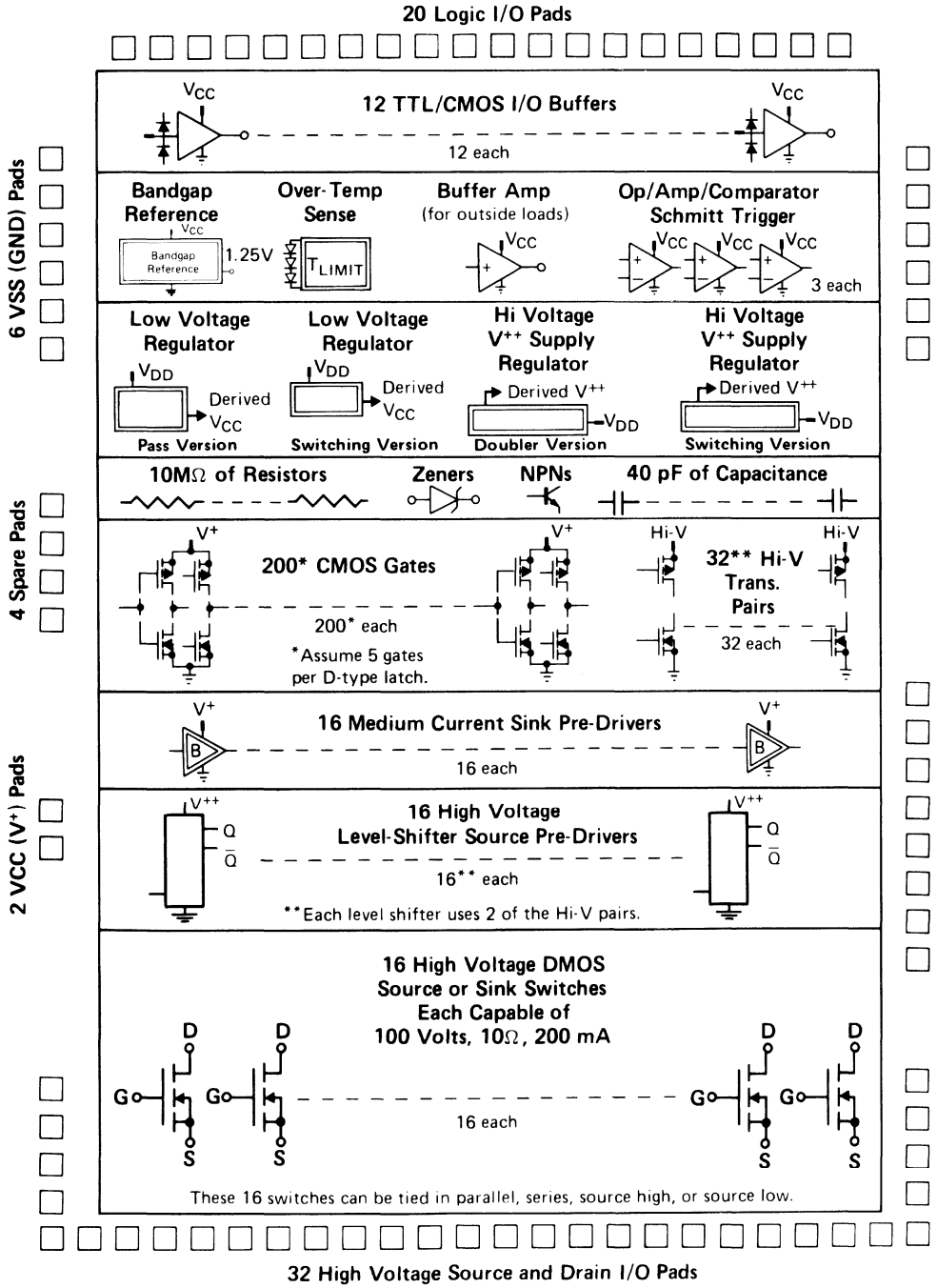
5

Typical Semicustom Design Cycle Following Exploratory Discussions and Contract Initiation

Week	Action
1	Design & Customer Interface
2	Design & Customer Interface
3	Electrical & Layout Computerized Checks
4	Mask Generation
5	Mask Generation
6	Apply ASIC Masks to Preprocessed Wafers
7	Wafer Test
8	Package Test Units
9	Final Test, QA & Ship 25 Units

DETAILED COMPONENT AND PAD LISTING:

This diagram lists the components available to the designer for laying out an MPD8020 semicustom circuit. The I/O pads shown around the periphery represent the total number available; all pads are not normally used in a given circuit/package combination.



MPD8020 ELECTRICAL SPECIFICATIONS

MPD8020 SPECIFICATIONS AND MASK PROGRAMMABILITY

The MPD8020 is a highly versatile mask programmable semicustom chip and the electrical specifications of the predesigned macros cannot be fully specified for all possible bias currents and all possible transistor combinations. For example, the linear block op amp will exhibit different gain bandwidth, slewrate, and input voltage capabilities, depending on the transistors used and the bias current into the current mirrors. The hysteresis and trip points of the overtemperature protection macro and the Schmitt trigger similarily are a function of what the designer specifies in the I/O parameters.

The following specifications are examples of how the MPD8020 can function, but should not be considered the final word on performance specifications.

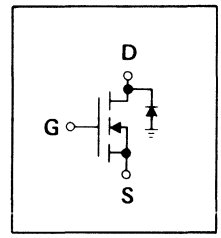
Greater speed, lower offsets, different operating ranges are all available by making engineering tradeoffs and by exercising design options.

Absolute Maximum Ratings

Storage Temperature	Ts	−65 to +150°C
Operating Temp	Ta MIC8020	0 to +70°C
	MIC8020M	−55 to +125°C
DC Input Voltage		−0.5 to Vdd
(any input pin to Vss)		+0.5 Volts
Vcc Supply Voltage		18 Volts
Drain-Source Voltage	Bvdss	110 Volts
Drain-Gate Voltage	Bvdgr, Rgs=20K-ohm	110 Volts
Continuous Drain Current per output	Id	200mA
Pulsed Drain Current per outlet	Ip	500mA
Gate-Source Voltage	Vgs	+/-20 Volts

N-CHANNEL DMOS POWER FET'S

The 16 DMOS power FET's are fully floating between ground and Vdd. Normally a 35V gate-to-source protection diode is inserted to protect the gate from excessive transients. Each DMOS FET may be tied to Vdd, ground, or in between. Paralleling 2 or more DMOS FET's reduces the "ON" resistance and increases the current handling capability in a ratio directly proportional to the number of FET's used.



Electrical characteristics @ Vss=OV T =25°C unless otherwise specified.

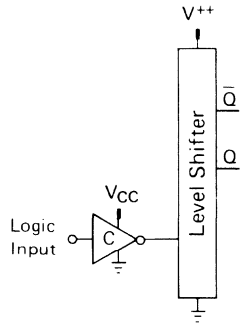
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1 $BV_{DSS, DRAIN}$	V_{in} = OV; I_D = 100μA	100			V
2 I_D (continuous)	V_{in} = 15V; V_{out} ≤ 2V	200			mA
3 I_D (pulse)	V_{in} = 15V; V_{out} ≤ 8V (note 1)	500			mA
4 R_{DS} (15V)	V_{in} = 15V; I_D = 100mA (note 1)		8	14	ohm
5 R_{DS} (10V)	V_{in} = 10V; I_D = 100mA (note 1)		9	24	ohm
6 I_{DSS}	V_{in} = OV; T_j = 125°C, V_{DS} = 100V		100	1000	μA
7 V_{th}	I_D = 1mA; V_{DS} = V_{GS}		3	5	V
8 V_{DS} (on)	I_D = 100mA; V_{in} = 15V (note 1)			1.4	V
9 C_{iss}	(note 2)		35	60	pF
10 t_d (on)	(notes 1 & 3); V_{in} = OV, 15V; R_s = 50 ohm		33	40	ns
11 t_f (off)	(notes 1 & 3); V_{in} = OV, 15V; R_s = 50 ohm		50	70	ns
12 I_{in}	V_{in} = OV or V_{in} = 15V		1	10	μA

Note 1—Pulse test; pulsewidth ≤ 300μS, duty cycle ≤2%
Note 2—Guaranteed by design, but not tested on a production basis.
Note 3—R_L = 1000 ohm non-inductive 10W resistor to 100V supply; measured form 50% of input to 50% of output.

HIGH VOLTAGE LEVEL SHIFTERS

The 16 possible level shifters are each made up of 2 N-channel and 2 P-channel high voltage, thick gate oxide (capable of withstanding the full V++ supply in either direction), transistors connected in 2 cross coupled pairs. Multiple level shifters or augmented outputs may be metalized-in for greater drive capability.

The 64 high voltage CMOS transistors (used in the level shifters) are also available in uncommitted form for high voltage logic and use as switching and pass devices for voltage regulators.



Electrical characteristics @ Vss=OV, Vcc=15V, Vdd=100V, 1 open source DMOS connected to the $\overline{Q}$ output, Ta=25°C unless otherwise specified.

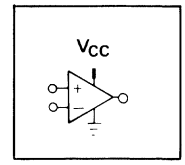
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1 $BV_{DSS, DRAIN}$	V_{in} = OV; I_D = 100μA	100			V
2 V_{in} low	$\|I_{in}\| \leq$ 1mA @ V_{out} = 100V		7.8	2.5	V
3 V_{in} high	I_D = 100mA; (note 1)	12.5	7.6		V
4 t_d (on)	(notes 1 & 2); R_s = 50 ohms		37	65	ns
5 t_f (off)	(notes 1 & 2); R_s = 50 ohms		35	60	ns

Note 1—Pulse test; pulsewidth ≤ 300μS, duty cycle ≤ 2%
Note 2—R_L = 700 ohm non-inductive 10W resistor to a 70V supply; measured from 50% of input to 50% of output.

GROUND SENSING OP AMP FROM A LINEAR MACRO

A configurable linear gain macro metalized as an op amp with P-channel MOS transistors in the input is capable of sensing linear signals down to (and approximately 300 millivolts below) ground. The gain, bandwidth, slewrate, etc. are functions of the master bias current fed to the op amp. The following specifications are one snapshot of the op amp at the bias and voltage shown below.

Other op amp options include NPN bipolar inputs, N-channel MOSFET inputs, and lighter frequency compensation.



All of the linear macro implementations, with the exception of the linear buffer, are intended to drive light loads (i.e. another op amp, a comparator, a gate, etc.) and so they are tested with high impedance loads on the order of a megaohm. Gain degradation should be expected at loads of 100K ohms or less.

Electrical characteristics @ Vss=OV, Vcc=15V, Rbias=390K Ohms, Ta=25°C unless otherwise specified.

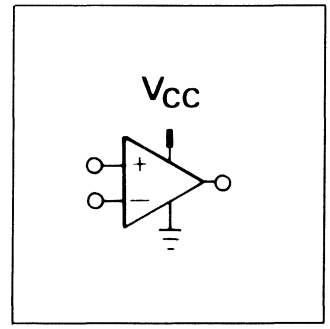
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1 V_{in} Range		−0.3		13.5	V
2 $\|V_{OS}\|$	$V_{in\ common\ mode}$ = 7.5V		2.7	30	mV
3 V_{out} Swing	R_L = 1M ohm	0.2		13.0	V
4 AV_{OL}	$V_{in\ common\ mode}$ = 7.5V	1.5	25		V/mV
5 CMRR	V_{in} = 5V, 10V	40	88		dB
6 PSRR	V_{cc} = 14V, 15V	50	88		dB
7 Slew Rate	V_{REF} = 7.5V, V_{in} = 7V, 8V		3		V/μs
8 Bandwidth	−3dB small signal unity gain		4		MHz
9 $\|I_{in}\|$	$V_{in\ common\ mode}$ = 7.5V			1.0	μA

GROUND SENSING COMPARATOR FROM A LINEAR MACRO

A linear macro, configured as a comparator with ground sensing inputs, has P-channel MOS inputs and like the ground sensing op amp can accept signals down to approximately 300 millivolts below ground. The gain and response speed are a function of the bias and supply voltage. The following specifications are one snapshot of the comparator at the bias and voltage shown below.

Other comparator options include NPN bipolar inputs, N-channel MOSFET inputs, and higher bias for increased accuracy, higher input voltage range, and speed respectively.

All of the linear macros, with the exception of the linear buffer, are intended to drive light loads (i.e. op amps, gates, etc.) and so are tested with high impedance loads on the order of a megaohm. Gain degradation should be expected at loads of 100K ohms or less.



Electrical characteristics @ Vss=OV, Vcc=15V, Rbias=390K Ohms, Ta=25°C unless otherwise specified.

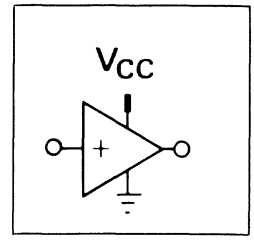
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1 V_{in} Range		−0.3		13.5	V
2 $\|V_{OS}\|$	$V_{in\ common\ mode}$ = 7.5V		2.5	30	mV
3 CMRR	$V_{in\ common\ mode}$ = 5V, 10V	60	65		dB
4 PSRR	V_{cc} = 14V, 15V; $V_{in\ common\ mode}$ = 7.5V	50	53		dB
5 AV_{OL}	$V_{in\ common\ mode}$ = 7.5V	1.5	10		V/mV
6 V_{OH}	R_L = 1M ohms to ground	13.4	14.8		V
7 V_{OL}	R_L = 1M ohms to ground		0.01	0.5	V
8 Response, TTL	V_{REF} = 1.4V; V_{in} = 0.8, 2.0V; note 1, note 2		290	300	ns
9 Response, 110mV	V_{REF} = 1.4V; V_{in} = 1.345V, 1.455V; note 1, note 2		750	900	ns
10 $\|I_{in}\|$	$V_{in\ common\ mode}$ = 7.5V			1.0	μA

Note 1—Measured from 50% of input to 50% of output.
Note 2—R_{BIAS} = 56K ohms; decreasing R_{BIAS} increases the speed. Chip designs allow changing current mirror ratios to improve speed while leaving R_{BIAS} unchanged.

UNITY GAIN BUFFER

The unity gain buffer provides a relatively high current linear element for driving analog signals off of the chip.

For increased accuracy the buffer is normally included in the loop with another linear macro or one of the gate array implementations of an op amp.

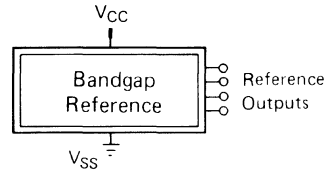


Electrical characteristics @ Vss=OV, Vcc=15V, Rbias=390K Ohms, Ta=25°C unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1 Voltage Gain	V_{in} = 7.5V	0.9		1.2	V/V
2 V_{out} Range	R_L = 2M ohms to ground	1.5		13.5	V
3 V_{out} Swing	R_L = 2K ohms to ground	2.5		12.5	V
4 Slew Rate	V_{in} = 1.5V to 13.5V		280		V/μs
5 $\|I_{in}\|$	V_{in} = 7.5V			1.0	μA

BANDGAP REFERENCE

The bandgap reference supplies a low drift reference voltage for the overtemperature, overvoltage, overcurrent, and linear comparison functions of the chip. The basic output is approximately 1.25V with ratioed voltage taps available from a resistor chain extending up to close to Vcc. Popular taps include 2.5V, 5V, 10V, etc., but the additional output need not be restricted to integer multiples of 1.25V.



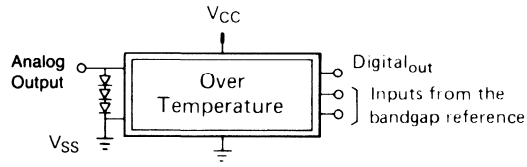
Electrical characteristics @ Vss=OV, Vcc=15V, Ibias=3.5μA, Ta=25°C unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1 V_{out}			1.21	1.35	V
2 V_{out} average T.C.	$-55°C \leq T_j \leq 125°C$		300		ppm/°C

OVERTEMPERATURE DETECTION CIRCUIT

The overtemperature detector senses the temperature of the chip and reacts with a digital "1" output when the chip exceeds a predetermined temperature (+125°C in the example below). Built-in hysteresis prevents the circuit from resetting until the chip passes a preset lower trip point (+85°C in this example) thereby inhibiting thermal oscillations.

Both trip points are mask programmable from the output of the bandgap reference.



Electrical characteristics @ Vss=OV, Vcc=15V, Rbias= 390K Ohms, Ta=25°C unless otherwise specified.

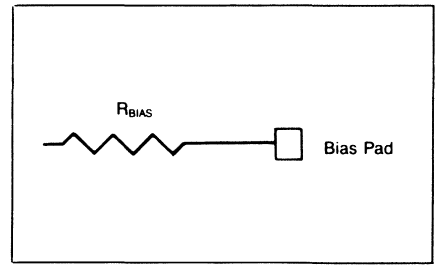
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1 V_{out} Digital	T_j = 125°C	14.5	14.94		V
2 V_{out} Analog	T_j = 25°C, I_{out} = 1μA		1.8	2.2	V
3 V_{out} Analog T.C.	−55°C ≤ T_j ≤ +155°C, I_{out} = 10μA		6.7		mV/°C
4 V_{out} Digital	Low temperature T_j < +85C		0.006	0.5	V
5 V_{out} Digital	Temp decreasing +85°C < T_j < +125°C	14.5	14.94		V
6 V_{out} Digital	Temp increasing +85°C < T_j < +125°C		0.006	0.5	V

5

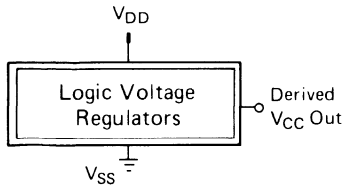
BIAS

A single bias resistor (or current source) is used to program all of the current mirrors used in the linear portions of the chip. The same current is also used to determine the operating point of linear op amps, and comparators, imprinted on the gate array. Typical bias configurations call for a resistor tied from Vcc to the bias pin (which would be one N-channel MOS threshold above ground) or alternatively the resistor is tied from ground to the bias pin (which in that case would be one P-channel MOS threshold below Vcc).

The master bias input allows programming of the speed, bandwidth, output driver, and power dissipation of most of the analog functions on the chip.

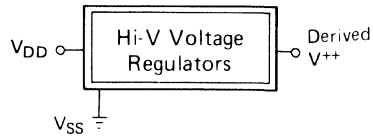


INTERNAL VOLTAGE REGULATORS



Internal regulators can generate local low level digital/analog voltages (Vcc) from a single Vdd high voltage supply of 20 Volts to 100 Volts or extra high (V^{++}) voltages above Vdd.

Low Voltage digital/analog Vcc voltage is normally derived using a pass regulator for low current requirements. A switching regulator using an inductor is used when current requirements are high and input/output voltage differentials are large.

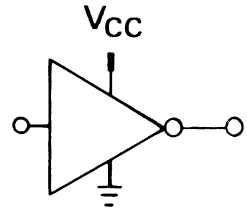


Extra high voltage (V^{++}) is normally derived using a voltage "doubler." V^{++} is needed to power the level shifters used to pull the N-channel DMOS gates above Vdd. An external clamping zener diode holds V^{++} at 15V to 20V above Vdd (for Vdd ≥ 20V). This zener diode gives over voltage protection to the level shifters, while holding V^{++} at 18V to 20V above Vdd.

This is sufficient to insure "rail-to-rail" switching of DMOS power FET's. For cases requiring higher efficency, V^{++} can be derived using an inductor in a switching regulator.

TTL/CMOS INPUT/OUTPUT BUFFERS

The 12 TTL/CMOS I/O buffers accept TTL and CMOS logic level input signals and are capable of driving offchip TTL or CMOS gates and buses.



Electrical characteristics @ Vss=OV, Ta=25°C unless otherwise specified.

		Vcc = 15V			Vcc = 5V			
PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
1 V_{IH}		12.5	7.6		2.0	1.5		V
2 V_{IL}			7.4	2.5		1.3	0.8	V
3 V_{OH}	I_O = 10 μA	13.5	14.9		4.5	4.99		V
4 V_{OL}	I_O = 10 μA		.01	1.5		.005	0.5	V
5 $\|I_{in}\|$				1			1	μA
6 $\|I_{OH}\|$	V_{out} = V_{IH} min	2	24		0.4	15		mA
7 I_{OL}	V_{out} = V_{IL} max	13	40		6	7.7		mA
8 C_{in}			7.5			7.5		pF
9 t_{PLH}	C_L = 15pF to gnd		55	100		55	150	nS
10 t_{PHL}	C_L = 15pF to gnd		55	100		55	150	nS

DIGITAL GATE ARRAY

The 200 gates which make up the digital gate array are two input logic elements. Each gate's 2 P-channel and 2 N-channel transistors are floating and can be used to make up transmission gates, op amps, comparators, Schmitt triggers and so forth.

Predesigned digital macros for the gate array include NAND gates, NOR gates, flip-flops, decoders, latches, shift registers, counter, etc. Essentially any 74XX, 74CXX, or 4000 series digital function of reasonable size can be imprinted on the array. Extensive underpasses and logic highways are present to optimize utlization of the array.

The following table shows some of the gate delays low-to-high and high-to-low for various implementations of NAND and NOR gates. NOR gates with their use of stacked slow P-channel FET's are slower than NAND gates which use paralleled P-channel's to accomplish this logic function.

Electrical characteristics @ Vss=OV, Ta=25°C unless otherwise specified.

		Vcc = 15V			Vcc = 5V			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
1 V_{OH}	$V_{in} = V_{IH}$	13.5	7.6		4.5	1.5		V
2 V_{OL}	$V_{in} = V_{IL}$		7.4	1.5		1.3	0.5	V
3 $\|I_{in}\|$	$V_{in} = V_{CC}$			1			1	μA
4 t_{PLH} Inverter	(note 1)		1.4			3.5		ns
5 t_{PLH} 2input NAND	(note 1)		1.4			4.1		ns
6 t_{PLH} 4input NAND	(note 1)		2.2			6.0		ns
7 t_{PLH} 2input NOR	(note 1)		2.0			6.3		ns
8 t_{PLH} 4input NOR	(note 1)		6.3			19.0		ns
9 t_{PHL} — inverter	(note 1)		0.5			1.0		ns
10 t_{PHL} 2input NAND	(note 1)		0.6			1.8		ns
11 t_{PHL} 4input NAND	(note 1)		2.5			8.4		ns
12 t_{PHL} 2input NOR	(note 1)		0.5			1.0		ns
13 t_{PHL} 4input NOR	(note 1)		0.6			2.8		ns
14 f_{osc}	Nine gate. Free running ring oscillator		50			20		MHz

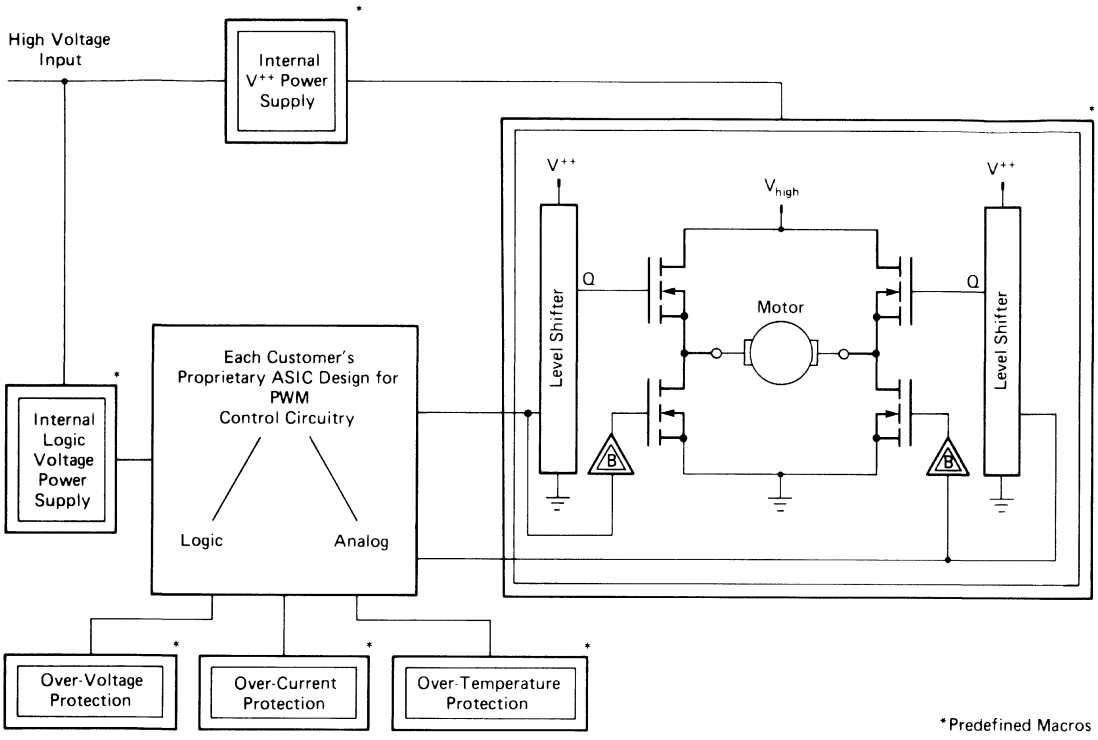
Note 1—Delay time is measured from 50% point of input to 50% point of output.

ZENERS, RESISTORS, AND CAPACITORS

The array contains a large number of zener diodes with 35V, 10V, and 6V breakdowns. In addition there are polysilicon resistors for the 0.1 ohm to 1K ohm range, p-plus resistors for the 1K ohm to 10K ohm range, and p-well resistors for the 10K ohm to 1M ohm range. Each of the linear gain blocks plus the buffer amplifier and the bandgap reference contain capacitors (which are available if a particular circuit is not used) and in addition the innate capacitance of diodes and zener diode can be used for implementing delay and AC coupling functions.

MPD8020 APPLICATION EXAMPLES

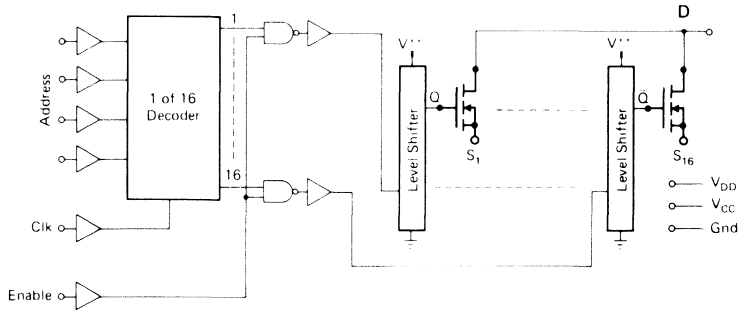
MOTOR CONTROL APPLICATION



The above motor control application shows how a mixture of predefined macros and customer proprietary ASIC control circuits are used to make a circuit optimally fit an application. Each transistor in the bridge can be a single DMOS FET, or 2 to 4 FET's in parallel for added current capability. Three phase motor control simply requires an addition level shifter and buffer driver. Since there are 16 DMOS FET's, 16 level shifters and sixteen drivers, a large number of drive combinations are possible.

DECODER DRIVER APPLICATIONS

1 of 16 HIGH SIDE DECODER-DRIVER APPLICATION

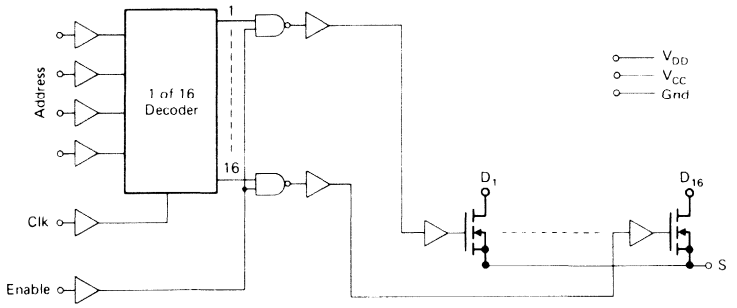


COMMON DRAIN VERSION

- 4 bit address input
- 16 outputs of 200 mA (500mA pulse) each at up to 100 Volts
- Enable input for multichip systems
- Optional over-temperature, over-current and over-voltage sensing

5

1 of 16 CURRENT SINKING DECODER-DRIVER APPLICATION



COMMON SOURCE VERSION

- 4 bit address input
- 16 outputs of 200 mA (500mA pulse) each at up to 100 Volts
- Enable input for multichip systems
- Optional over-temperature, over-current and over-voltage sensing

Common drain and common source decoder drivers can be run as 1 of 16 as shown above or the DMOS outputs can be paralleled for greater output current capability.

MPD8020 KIT PARTS

Micrel offers two kit parts for use in developing ASIC designs on the MPD8020 CMOS/DMOS/Bipolar semicustom array.

MPD8020-KIT PART # 1 ANALOG SSI AND MSI CIRCUITS APPLIED TO THE MPD8020

PURPOSE

Kit Part #1 demonstrates the operation of several of the analog SSI and MSI circuits which can be implemented on the MPD8020 CMOS/DMOS Semicustom High Voltage Array. This kit part offers the designer the opportunity to see one set of characteristics of the array. Since all of the op amps, comparators, power DMOS FET's, bandgap, Schmitt Trigger, and digital circuits are configurable, parameters such as gain, offset, drive current, temperature settings, etc. can be changed and in fact optimized for each designer's application. This kit part shows the performance of several of the analog circuits plus some of the digital circuits in one of their many configurations.

DESCRIPTION

The metal and contact masks which define Kit Part #1 were applied to the MPD8020 CMOS/DMOS Semicustom High Voltage Array such that eleven analog circuits are available. These circuits are:

1. Comparator, with ground sensing inputs
2. Op Amp, with ground sensing inputs
3. Unity gain buffer
4. Over Temperature detector circuit
5. Pass version of a local Vcc voltage regulator (dropped from Vdd)
6. Voltage "doubler" for V^{++} (above Vdd)
7. Open drain DMOS FET (10 Ohm) with direct gate access
8. Open drain DMOS FET (10 Ohm) with logic input
9. Open source DMOS FET (10 Ohm) with high voltage level shifter
10. Bandgap reference
11. Pulse width modulator "H" Bridge (3.3 Ohm) with steering and enable

MPD8020-KIT PART # 2 ANALOG SSI AND MSI CIRCUITS APPLIED TO THE MPD8020 (PLUS GATE ARRAY LINEAR CIRCUITS)

PURPOSE

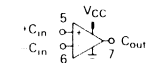
Kit Part #2 demonstrates the operation of several of the digital SSI and MSI circuits which can be implemented on the MPD8020 CMOS/DMOS Semicustom High Voltage Array. This kit part offers the designer the opportunity to see actual gate delays, shift register speeds, ring counter operation, etc. versus supply voltage and temperature. Analog circuits imposed on the digital array are explored using a transmission gate/analog switch, comparator, Schmitt Trigger, and op amps. This kit part shows a few of the myriad of digital (and analog) macros which can be implemented in the digital array. Any 74C or 4000 series logic function or set of functions taking up fewer than 200 gates can be put on the gate array.

DESCRIPTION

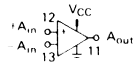
The metal and contact masks which define Kit Part #2 were applied to the MPD8020 CMOS/DMOS Semicustom High Voltage Array such that eight digital circuits are available. These circuits are:

1. 4-bit parallel output shift register plus a shift by sixteen output
2. Ring oscillator and gate timing check circuits
3. TTL compatible flip-flop
4. Comparator (built from gate array transistors)
5. Schmitt Trigger (built from gate array transistors)
6. Op Amp (built from gate array transistors) and the unity gain buffer
7. Op Amp (1 of the 3 configurable macros) with NPN bipolar input transistors
8. Transmission-gate/analog-switch

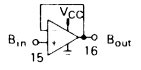
MPD8020 KIT PART #1
ANALOG SSI AND MSI CIRCUIT OVERVIEWS



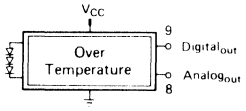
1. Comparator



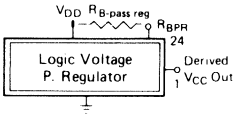
2. Op Amp



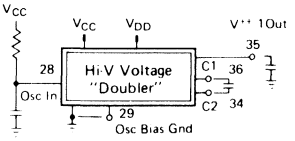
3. Buffer Amp



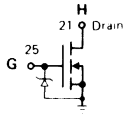
4. Over Temperature Detection Circuit



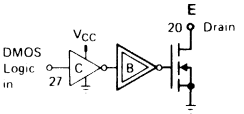
5. Pass Version of Local V_{CC} Voltage Regulator



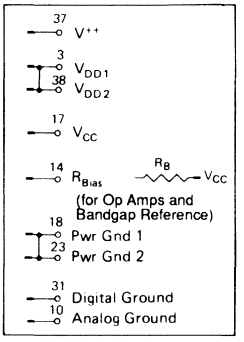
6. $V^{++}1$ High Voltage "Doubler"

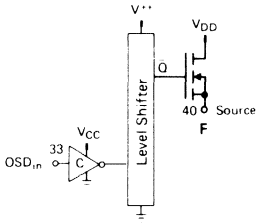


7. Open Drain DMOS with Direct Access

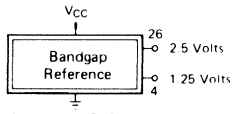


8. Open Drain DMOS with Logic Driver

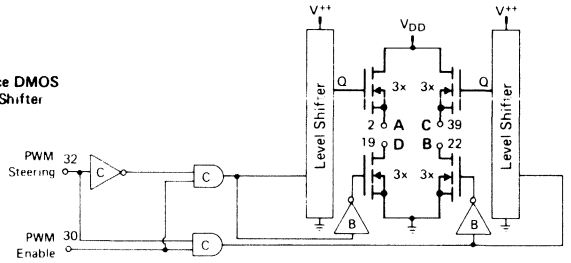




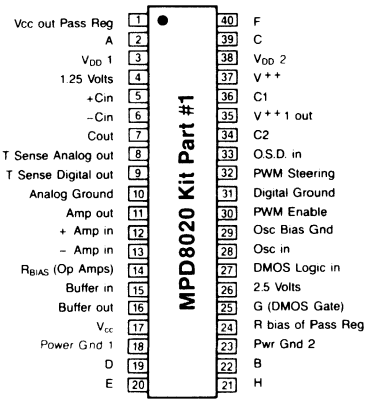
9. Open Source DMOS with Level Shifter



10. Voltage Reference



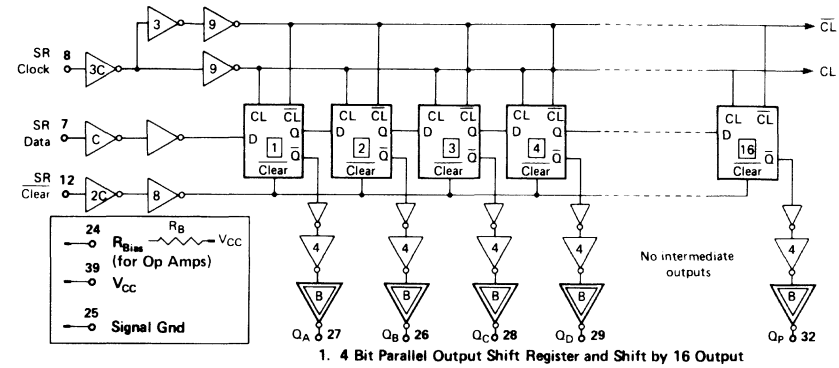
11. PWM "H" Bridge



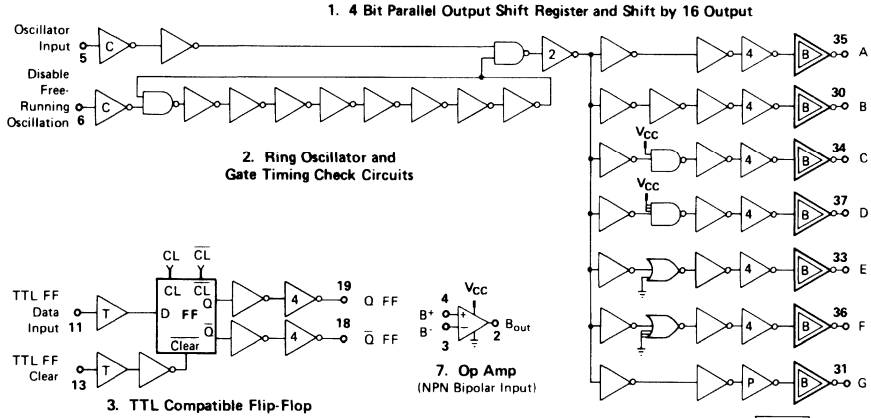
Kit Part #1 Pin-out
TOP VIEW

5

MPD8020 KIT PART #2
DIGITAL SSI AND MSI CIRCUITS OVERVIEWS



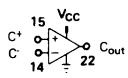
1. 4 Bit Parallel Output Shift Register and Shift by 16 Output



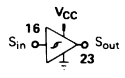
2. Ring Oscillator and Gate Timing Check Circuits

3. TTL Compatible Flip-Flop

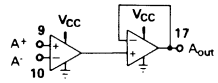
7. Op Amp
(NPN Bipolar Input)



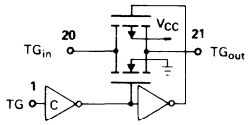
4. Comparator
(from gate array)



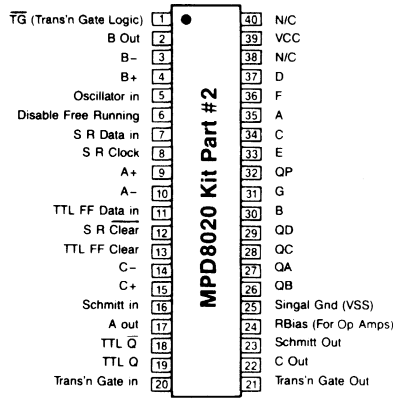
5. Schmitt Trigger
(from gate array)



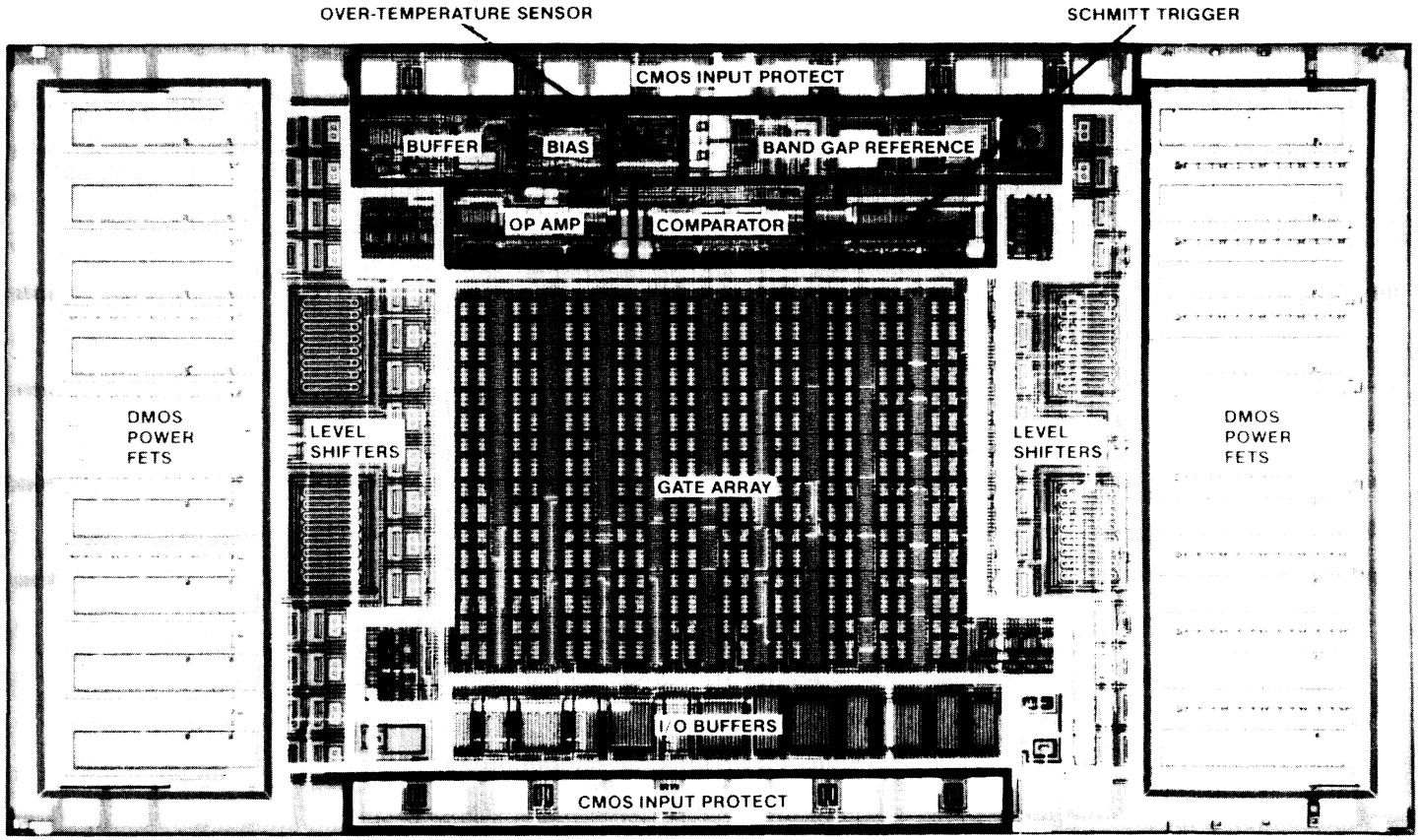
6. Op Amp/Buffer Amp
(from gate array)



8. Transmission Gate



Kit Part #2 Pin-out
TOP VIEW



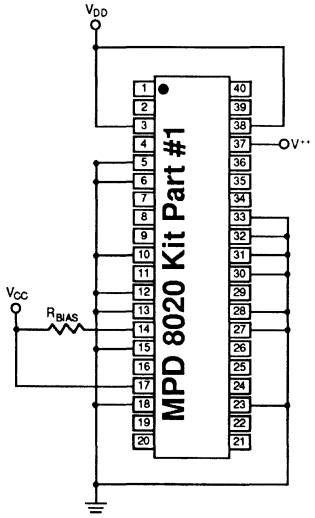
MICREL *MPD8020 CMOS/DMOS SEMICUSTOM HIGH VOLTAGE ARRAY

*(PATENT PENDING)

Application Hints KP1

Unused Inputs

Unused inputs should be tied together to V_{CC} or ground, specifically pins 5, 6, 12, 13, 15, 27, 28, 30, 32, and 33; not doing so can cause excessive and/or variable I_{CC} current. R_{BIAS} (pin 14) and oscillator bias ground (pin 29) should be left floating when not in use.



Unused Input Pins KP1

Analog Circuits

The analog circuits i.e. (the comparator, op amp, buffer amp, and the over temperature detection circuit) all require that pin 10 (analog ground) is grounded, and pin 14 (R_{BIAS}) is connected through a bias resistor (usually 390 kΩ) to V_{CC}.

The buffer amp is designed to be used in the loop with either the op amp or the comparator to drive analog signals off the chip; any offset associated with the buffer amp will be divided by the gain of the previous stage. Suitable frequency compensation for loop stability should be employed. The gain, slewrate, output drive capability, and bandwidth of the linears may be adjusted by changing R_{BIAS} (and therefore I_{BIAS}).

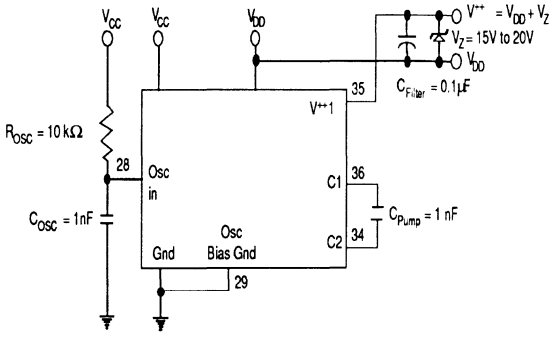
The true rise and fall times on the comparator are about 50nS when driving an on chip load such as a gate (0.5 pF), when V_{CC} = 15V and R_{BIAS} = 390 kΩ. If this comparator is used to drive an off chip load, the rise and fall times will be much larger due to capacitive loading and the other effects. With a scope probe on the output, the capacitive loading from the probe, pad, and the bond wire, is about 20 pF, or about 40 times larger than the intended load.

High Voltage Circuits

The high voltage doubler is used to generate the V^{++}supply. V^{++} is used for the level shifters, and should be greater than 15 volts above V_{DD}. for simplification, V^{++} may be connected to V_{DD} ,however the DMOS outputs will be one threshold below V_{DD} when the DMOS is on.

The level shifters come in two varieties, those in Kit Part-1A and those in Kit Part-1B. Kit Part-A1 is marked with a dot: MPD8020 "●". The level shifters are faster in Kit Part-1B than those in Kit Part-1A, however the current for the level shifters is larger in Kit Part-1B than Kit Part-1A.

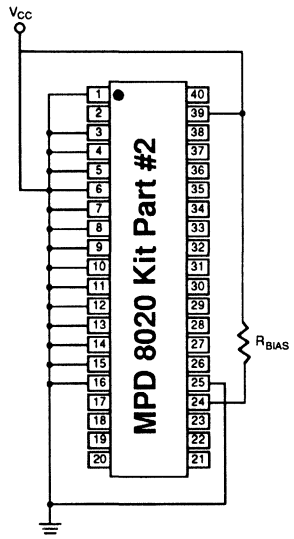
The voltage doubler may be driven either by a square wave generator or an external RC circuit connected to pin 28 (osc. in).The frequency of oscillation is approximately f=1/[0.7 C_{OSC} (R_{OSC}+ 4300)]. Connecting a 10 kΩ resistor to V_{cc} and a 1nF capacitors to ground resistor to V_{CC} and a 1nF capacitor to ground will generate a frequency of about 100kHz. For both cases pin 29 (oscillator bias ground) must be connected to ground. The recommended value C_{PUMP} is 1nF (between pin 34 and pin 36) and C_{FILTER} = 1.0μF (pin 35 to V_{DD}); an external 15V to 20 zener diode should be connected from V^{++} 1 out to



Application Hints KP2

Unused Inputs

Unused inputs should be tied together to V_{CC} or ground, specifically pins 1, 3, 4, 5, 7, 8, 9, 10, 11, 12, 13, 14, 15 and 16; not doing so can cause excessive and/or variable I_{CC} current. Disable free running oscillator (pin 6) must be tied to V_{CC} when not in use.



Unused Input Pins KP2

Digital Circuits

The free running oscillator will toggle at approximately 20MHz (for V_{CC} = 5V). Since CMOS draws current only during switching, a high I_{CC} will be observed when the oscillator is enabled (pin 6 to ground). At higher voltages, the oscillator will toggle faster, and draw a significant I_{CC}; it is therefore recommended that the free running oscillator be disabled during testing of other functions.

Analog Circuits

The analog circuits (i.e. the comparator, NPN op amp, and the op amp/buffer amp) all require that pin 24 (R_{BIAS}) is connected through a bias resistor (usually 390 kΩ) to V_{CC}.

The comparator and NPN op amp are designed to drive internal loads (i.e. small capacitive loads such as a buffer, logic, etc.,) and cannot drive resistive or moderate capacitive loads. The op amp/buffer amp combination however, is designed to drive off chip capacitive loads.

Any offset associated with the buffer amp will be divided by the gain of the previous stage. Suitable frequency compensation for loop stability should be employed. The gain, slew rate, output drive capability and bandwidth of the linears may be adjusted by changing R_{BIAS} (and therefore I_{BIAS}).

5

Micrel Semiconductor MPD8020 ASIS™ Design Package Overview

CMOS/DMOS Semicustom Array

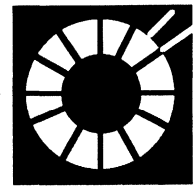
- Start with your circuit design needs
- Solve a problem in:
  - –Size
  - –Reliability
  - –Performance
  - –Keeping out competition
  - –Assembly and inventory costs
- Use the CMOS/DMOS technology to put any or all of the following on one IC:
  - –Analog CMOS
  - –Digital CMOS
  - –High voltage CMOS
  - –DMOS power FETs
  - –Predesigned macros
  - –CMOS gate array
  - –Bipolar

MPD8020 ASIS™ Applications

- Switching regulators
- Motion control
- Bilateral analog switches
- High voltage switching
- Relay and solenoid drivers
- Smart switch with bus decode
- Half or full bridge driver
- 3-ϕ motor driver
- Lamp driver
- Differential line drivers
- Automotive switching
- Printer solenoid drivers
- High-voltage display drivers

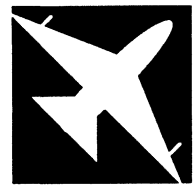
MPD8020 ASIS™ Advantages

Switch Mode Power Supplies



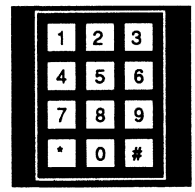
25 to 100V operation. Small size, up to 1MHz switching. Full and half H-bridge configurations. DMOS FET source/sink. "Bulletproof circuits" provide overcurrent, overvoltage, and overtemperature protection.

Military Avionics



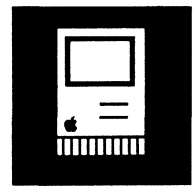
80V peak, 28V operating (more than 50% derated), capable of meeting Mil Std. 704C. Use for mil spec displays, pin diode drivers, lamp drivers, compact actuator controls, relay drivers, fly-by-wire controls. Wide environmental tolerance. High MTBF. Lightweight, and small size.

Telecommunications



48V for the central office. VLSI to reduce circuit board real estate. A prefect choice for card cages and subscriber sets. Shrink the size, increase the features and reliability.

Computer Peripherals, Office Equipment, and Industrial Controls



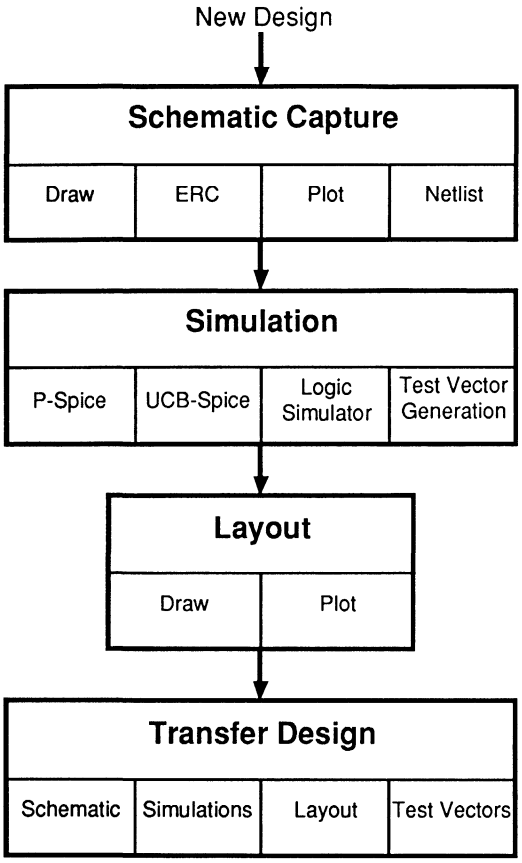
24V operating, 100V peak allows >50% derating for ruggedness. From FAX to friction. 16 solenoid drivers on a single chip. High efficiency and low development cost. 5V to 15V controls high current and/or high voltage. Customize your I/O. High side driver improves safety. Half, full, or 3-ϕ H-bridge configurations are great for HVAC controls, machine driver control, and robotics.

Medical Equipment

80 to 100V. High voltage for feedback and physiological needs. Semicustom array cuts costs, lowers size, reduces parts count, increases features, and improves reliability.

5

MPD8020 Design Flow



MPD8020 Design Package

Contents: Design books, software, and manuals

Training: 1 man week on-site at Micrel in Sunnyvale, California

Delivery: From Stock

MPD8020 ASIS™ IC Design Package Books

- Design Manual
- User's Guide
- Components Book
- Macro Book

MPD8020 Design Package Software

- **Automenu** Supports menus and runs batch jobs
- **Orcad Std III** Schematic capture
- **P-Spice** Analog and digital Spice simulation
- **UC Berkeley Spice** Analog Spice simulation
- **Orcad VST** Digital simulation
- **Probe** Analog and digital probing software
- **ICED** IC layout editor
- **Micrel 1** Component Library ("LIBRARY") symbol and model libraries
- **Micrel 2** Digital Macro Library ("DIGIMAC 1 & 2") macro symbol and model libraries
- **Micrel 3** Analog Macro Library ("ANAMAC 1 & 2") macro symbol and model libraries
- **Micrel 4** MPD8020 Base Library ("BASE") source, drain, poly, and base layers
- **Micrel 5** Macro Layout Libraries ("MACRO") analog, digital, and power layout libraries

Recommended MPD8020 Design Hardware

- IBM PC (286 or 386 based machine)
- 4M memory
- 20 MHz cache memory system
- 1.2M floppy
- 88M hard disk
- VGA card with monitor
- 20 MHz math co-processor
- Mouse and printer

Interfacing with Micrel

After discovering Micrel's MPD8020 and deciding that you can achieve a significant market advantage by using the MPD8020, follow these steps to complete the chip design and fabrication process:

Note: for jobs for Regional Design Centers (RDC) or in-house Corporate Design Centers (CDC) substitute RDC or CDC for Micrel in steps 2, 3, 4, and 6, 7, 8, 9, 10.

1. Contact Micrel or one of our customer representatives and request literature on the MPD8020. We have a data sheet and other literature available. Call Micrel at (408) 245-2500.
2. To further explore the MPD8020 solution, call Micrel for consultation on technical feasibility for use of the MPD8020 to meet design needs.
3. Send a schematic or a block diagram with a functional description or a breadboard. At this time or before the final design is completed, test vectors (also known as a table of parameters) must be submitted.
4. Micrel's marketing department reviews the business picture and general feasibility. Our design engineers evaluate feasibility of design and convert the schematic or block diagram to a schematic on the 8020 circuit using the advantages of the smart power IC solution. They also generate a chip utilization estimate.
5. With the MPD8020 schematic, the chip utilization estimate, and the customer's statement for package type and volume projections, Micrel's marketing department develops a price quote.
6. The customer's engineering group and purchasing area receives a firm quote from Micrel on price, delivery, and feasibility. You now have the information necessary for decision making.
7. Customer approval cycles are completed and a purchase order is issued to Micrel.
8. Micrel begins the design simulation stage which includes consultation with the customer when needed. This phase of design and simulation is completed.
9. The Preliminary Design Review (PDR) is completed and after any design modifications from the customer a Final Design Review (FDR) occurs. During these reviews you sit down with the Micrel engineers for up to two days and final design and testing requirements are reviewed and finalized. Note that all design modifications have to be finalized at this stage.
10. The chip is sent to layout, and through the use of Micrel's CAD tools, a pin-out is prepared. The bondability of the pin-out in the proposed assembly package is confirmed.
11. A complete continuity check is made of the layout with the schematic.
12. The circuit is sent out for masks. The masks are applied to three wafers in Micrel's fabrication facility. The chip is finalized and these first silicon chips are examined on Micrel's probe stations. Simultaneously, the automatic test equipment program for testing the chip is debugged and tested.
13. With the successful completion of these two programs, you are sent either dice or packaged units as specified for approval and integration into your system. Prototype assembly takes one week and production assembly takes four to five weeks.
14. For full military programs a 1,000 hour life and all other requirements for military standard 883 are now initiated.

MPD8020-0011

3-ϕ DC Brushless Motor Pre-Driver

Design Concept

Functional Description

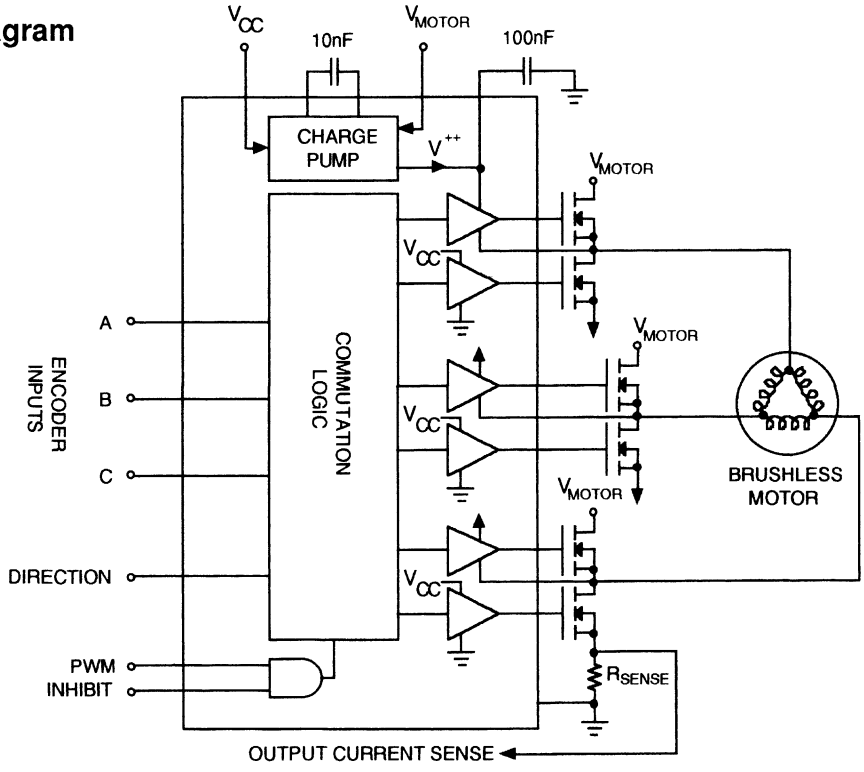
The MPD8020-0011 is a pre-driver for DC brushless motor controllers. Working with Hall-effect or optical feedback, the MPD8020-0011 develops the appropriate drive signals for directional and pulse-width modulation control of a motor. Inputs are included for implementing short circuit protection and for allowing the motor to freewheel.

The chip drives external quasi-complementary, N-channel power MOSFET output devices. An on-chip charge pump develops the necessary gate drive potential for the high side source followers, while low side gate drive is derived from the 15V (V_{CC}) chip supply.

Features

- Drives quasi-complementary, N-channel MOSFETs
- Full commutation logic with independent PWM and inhibit inputs
- On-chip charge pump for high side drivers eliminates the need for an external gate supply.
- 64V motor supply capability
- Mil spec part available
- Compatible with 60° sensor spacing

Block Diagram



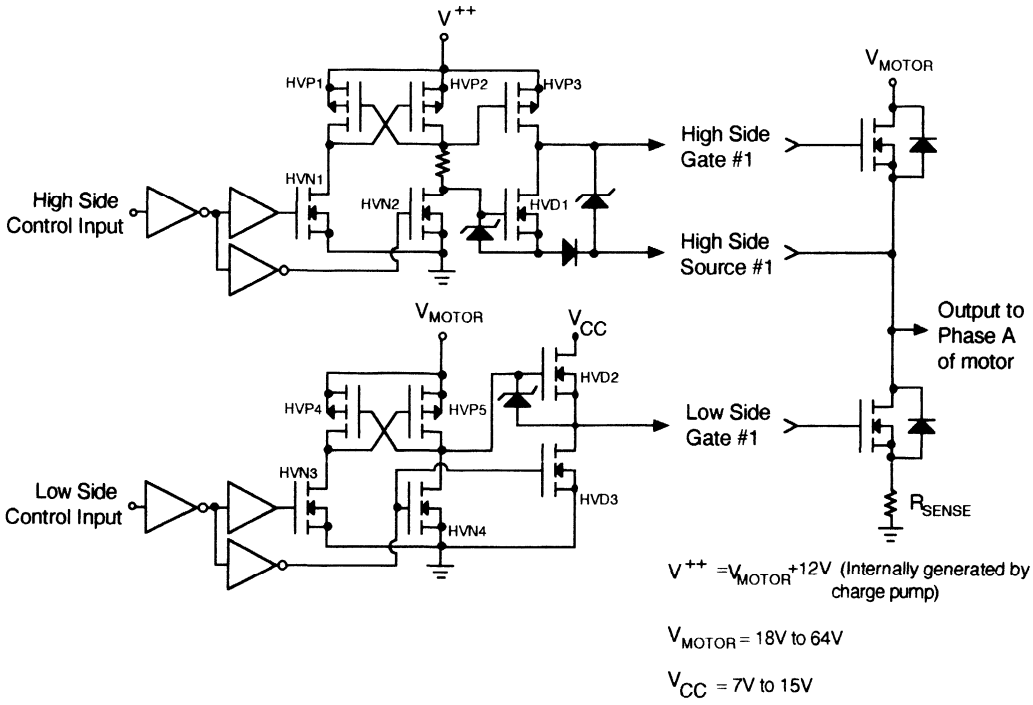


Figure 1. MPD8020-0011 Output Stage (one of three)

5

MPD8020-0012

8-Channel Low Side Driver with Diagnostics

Design Concept

Functional Description

The MPD8020-0012 is a high voltage, high current, microprocessor interface circuit for high reliability systems. Extensive self-diagnostic circuitry allows rapid detection and announcement of open loads, shorted loads, current overloads, and thermal problems. Included are 8 channels of open drain, N-channel DMOS power FETs that are controlled by individual inputs and a common chip enable. Each channel has a 200 mA current limit as well as full diagnostics. The circuit is implemented on Micrel's proprietary CMOS/DMOS/Bipolar process.

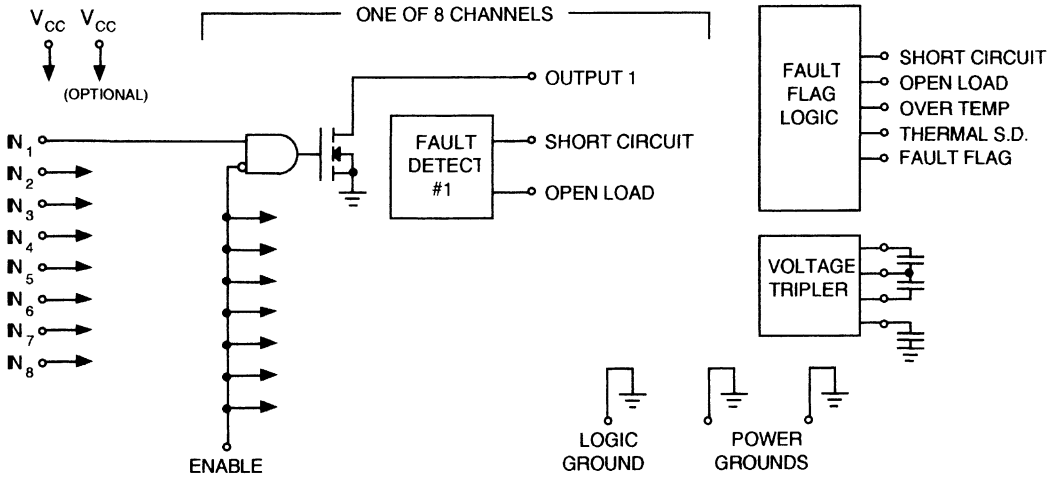
Features

- 8 open drain, N-channel outputs
- 80V, 200 mA outputs
- Logic compatible CMOS inputs with hysteresis
- Short-circuit proof
- Individual open load flags
- Individual short circuit flags
- Overtemperature warning flag and shutdown
- Summary data for short circuit, open load, and thermal flags

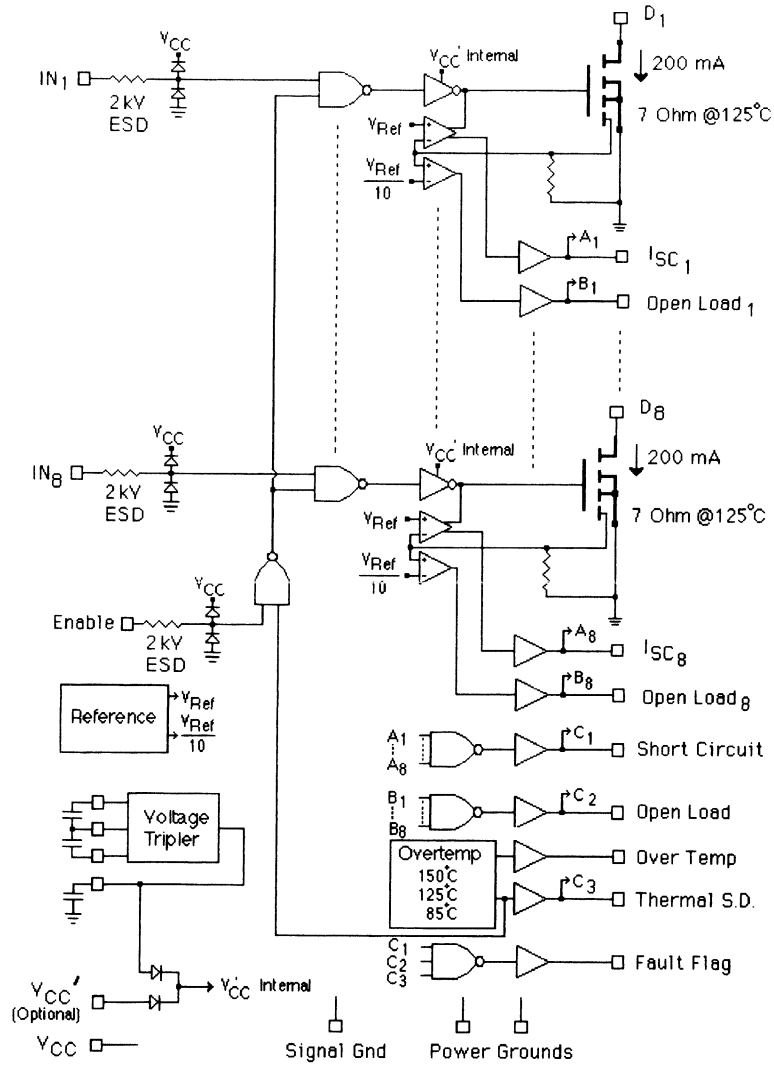
Applications

- Fault tolerant interface circuits
- A bullet-proof driver for relays, lamps, solenoids, print heads, displays

Block Diagram



Detailed Block Diagram



5

MPD8020-0013

PWM "Smart" Lamp Driver

Design Concept

General Description

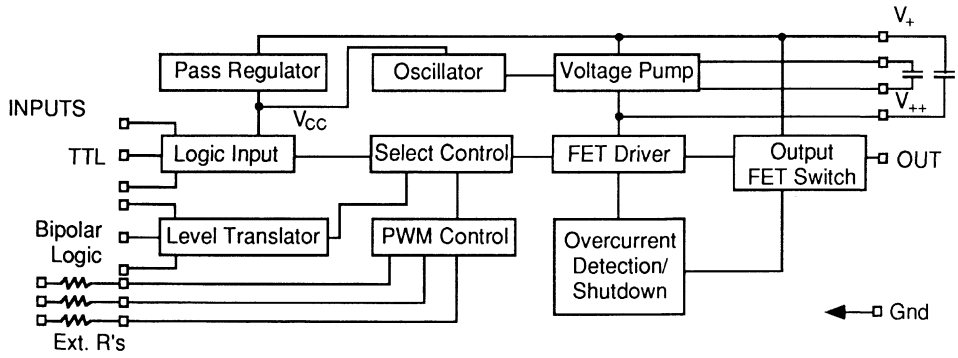
The MPD8020-0013 lamp driver is designed to operate from a 28 Volt DC, aircraft power source and drive up to four (4) 28 VDC incandescent lamps. Three duty cycle control modes set up the lamp intensities for different ambient conditions. In COM mode (100%) the lamps are full on for high ambient light. DIM mode (25%) accomodates reduced light and NV (10%) mode is used for very low ambient light. The PWM controlled intensity may be trimmed using external resistors. The intensity is controlled by logic input, either TTL/CMOS compatible or a relay/switch closure to system ground. The drive pulse rise and fall time is set at about 50 µS to reduce current spikes and minimize EMI. The lamp driver is a high side switch for ground referenced load applications. This helps minimize corrosion due to moisture on lamp socket contacts, and potential arcing during lamp replacement. Overcurrent protection prevents damage to the IC should the lamp socket be accidently shorted to ground while the lamp is on.

Features

The PWM Lamp Driver is a monolithic IC designed to drive 28 Volt incandescent lamps from an aircraft power source. The circuit has the following features:

- High side operation with lamp(s) connected to ground
- Input logic compatible with TTL/CMOS or switch closures
- Pre-driver with voltage pump, control and N-Channel FET Switch
- PWM to control lamp intensity from input logic
- PWM adjustment with external resistor or potentiometer
- Overcurrent detection and shutdown
- MIL STD 714A transient voltage protection
- MIL STD 883 qualification
- 16 pin ceramic side braze DIP package
- Bipolar logic compatible, <-5, >+5

Block Diagram



Technology

The fabrication technology chosen is CMOS/DMOS/Bipolar. It is the process of choice when combining analog, digital, and power MOSFET functions on a single IC. This technology is ideal for applications requiring interface between a microcontroller and electromechanical loads. The analog cells provide load current detection and control by using op-amps, comparators, a voltage regulator and a precision voltage reference. The N-Channel FETs provide high voltage (120V), high current up to 2 Amps. The digital gate array provides logic interface to a microcontroller and output logic. Status output signals are accessed through the digital interface.

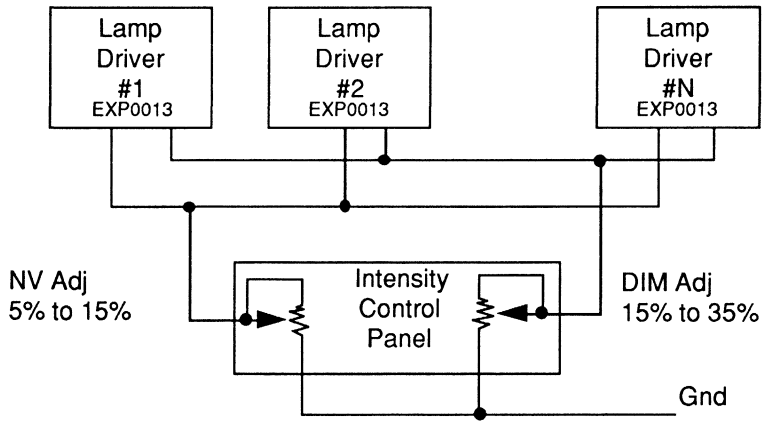
The CMOS/DMOS/Bipolar process technology is available for full custom and semicustom development programs requiring the use of intelligent control and power interface capability. Packaging is available for special needs.

Specifications

Operating Voltage ..... 28 Volts nominal (18 to 31 V)
Load Current ..... 500 mA Max (4 incandescent Lamps)
Logic Input (TTL) ..... V_{ss}/+1.0V to 3.5/V_{cc}
Logic Input(Bipolar) ..... "1">+5V, "0"<-5V
Switch Control Input ..... -5V/+5V to 100K Ohm
DIM Mode ..... 25% Duty Cycle +/-2% over temperature range
NV Mode ..... 10% Duty Cycle +/-2% over temperature range
Pulse Rise and Fall time ..... 30µS min to 100µS max.
Output Noise ..... 200mV P-P
Voltage Transient Protection ..... 80V with +/-1-100V/10µS pulse
Overcurrent Protection ..... 700 mA
Overtemperature Protection ..... 155 deg C max.

Lamp Driver Intensity Control

5



MPD8020-0014

High Current Sink/Source Driver

Design Concept

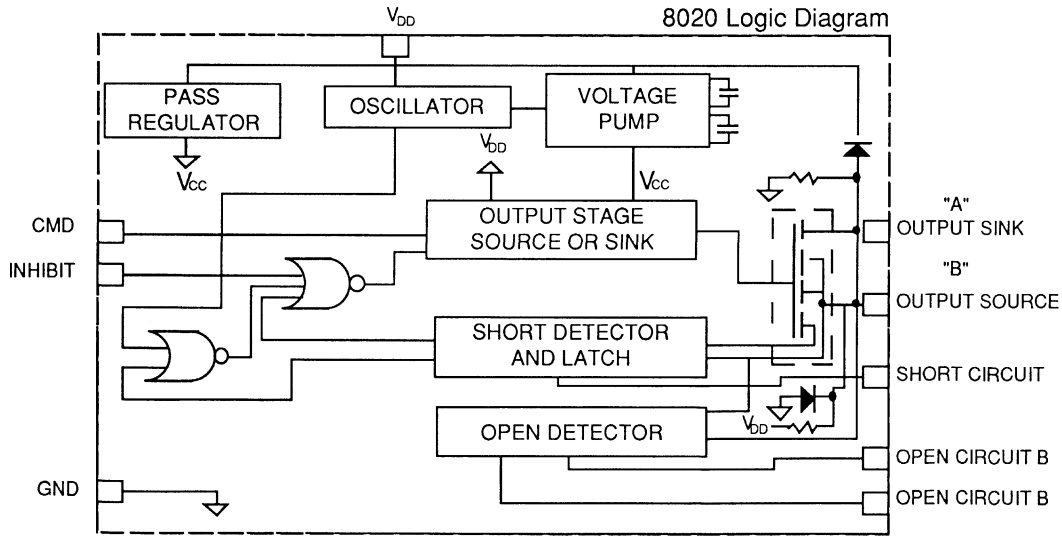
General Description:

The MPD8020-0014 High Current Driver is designed to drive a single N Channel Power MOSFET in either a Sink or Source load configuration. It is designed to operate from a Mil-STD-704D Avionics 28 volt bus, and includes transient voltage protection circuitry. An input logic high turns ON the Power MOSFET selected to meet the $RDS_{(ON)}$ and load current required for the application. A sense circuit determines if the load is in sink or source configuration. The FET sense lead generates current proportional to the load, and a reference voltage and comparator determines the current value for overcurrent protection. Flags are generated to indicate an open or short circuit load. The overcurrent detector turns off the driver, and periodically monitors the overcurrent condition, preventing damage to the MOSFET driver.

Features

- Smart Drive for Solenoid or Relays
- Input Logic Compatible with TTL or CMOS
- 16 Pin Side Braze Ceramic DIP package
- Operation Temperature of 55°C to +125°C
- Configurable to drive loads of 5 to 500 Amps
- High Side or Low Side Operation
- Short or Open Circuit Detection and Shutdown with Internal Reset
- Avionic Mil-STD-704D Voltage with Transient Protection
- Switch Load Current of 5 Amps
- Mil-STD-883 Qualification

Block Diagram



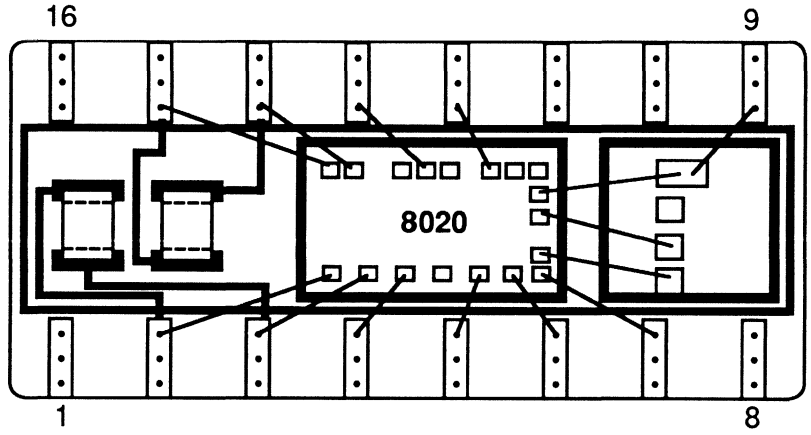
TECHNOLOGY

The process technology is CMOS/DMOS, combining analog, digital and power MOSFET driver macros on a monolithic microcircuit.

The technology is ideal for applications requiring interface between a microcontroller and electromechanical loads, and operating from an avionics 28 volt power bus.

The analog macros provide load current detection and control using op-amps, comparators, voltage regulator and precision voltage reference. A voltage doubler provides gate voltage enhancement for the MOSFET gate drive. Cross coupled pairs interface low level digital logic to high voltage drivers. Status output signals are accessed through digital buffers.

16 Pin Sidebraze (300mil width)



MPD8020-0015

Current Mode Buck Switching Regulator Controller

Design Concept

General Description

The MPD8020-0015 is a complete current mode controller for buck switching regulator applications, It contains additional features for external control as well as fault and status outputs in a single 28-pin package. The device is fabricated using Micrel's proprietary BCD* process and the MPD8020 array. Included are the high voltage and current interface stages that drive two external Power MOSFETs in the buck regulator circuit topology. A mode select line allows setting of single or two-phase drive operation.

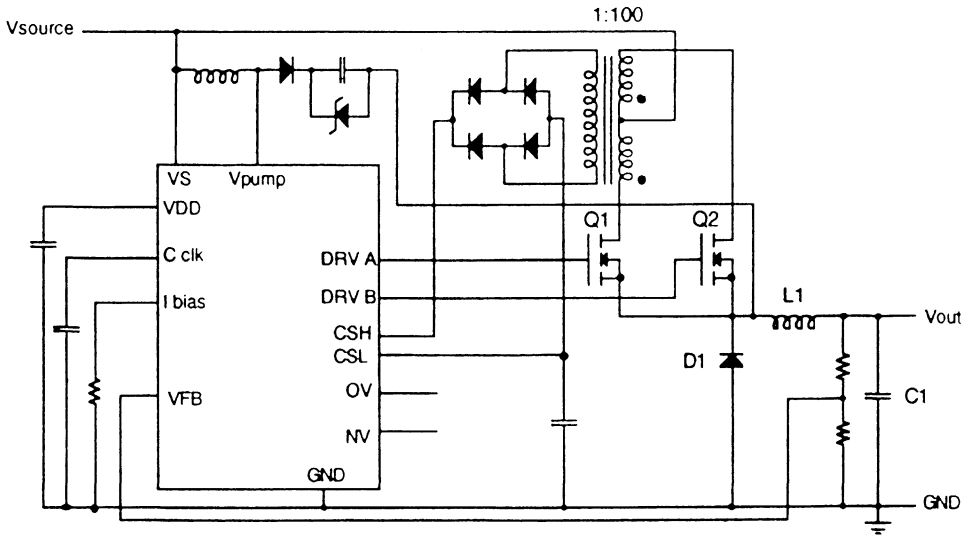
Configured within the gate array portion of the IC is the clock generator and digital timing generator that control the drive output synchronization, deadband pulse duration, and drive pre-drive for the voltage pump. The analog portion of the IC contains a bandgap voltage reference, error amplifier, and threshold comparators. Status outputs for over, under, and normal output conditions can drive LED indicators. An on-board pass regulator powers the lower voltage portions of the IC.

Features

- Up to 50 Volt operation
- Fully optioned current-mode control capability
- Dual DMOS Translator/ Power MOSFET drivers
- Digitally generated synchronization and deadband pulses
- Selectable single- or two-phase output drive modes
- Over-voltage and Under-voltage shutdown
- Over-voltage and Normal voltage status indicator drivers
- On-board regulator for analog and logic sections

* BCD is an advanced Bipolar, CMOS, and DMOS integrated processing technology.

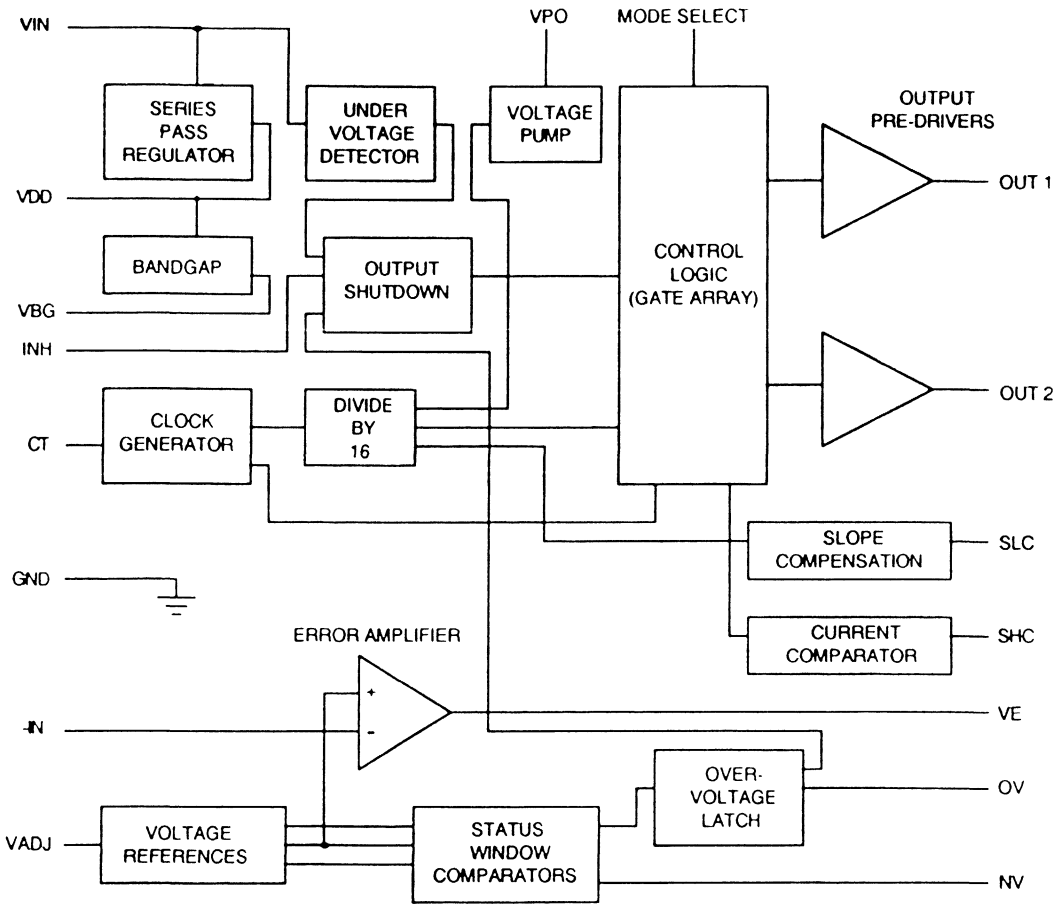
Application Schematic Diagram



Specifications

Operating Voltage	20 to 50V
Output Pre-driver	Tr = 60nS (@ 250mA) Tf = 30nS (@ −470mA) (Where C_L = 1500pF, Vr = 1 to 11V, and Vf = 15 to 5V
Drive Method	High-side, External N Channel MOSFETs
Bandgap	6.25V, ±10%, at I_{BG} = 1mA
Clock Frequency	2MHz, where Ct = 100pF, Blanking pulse = fo/16, Voltage Pump (VPO) = fo/4
Shutdown	Drivers held low, VPO OFF
Voltage References	Vh = 5.2V Vr = 5.0V Vl = 4.8V Ext. set and VBG = 6.25V
Amplifier/buffer	Avo > 50dB @ 100Hz Vos << 100mV Slew Rate > 4V/µS Iout = 5mA (typ.)
Comparator	Vth = 500mV Response Time = 100nS
Series Regulator	Vout = 12 to 15V, Isource = 25mA

Block Diagram



Note : Option pins not shown

SECTION 6: LOW DROP-OUT LINEAR VOLTAGE REGULATORS

Low-Dropout Voltage Regulator Selector Guide

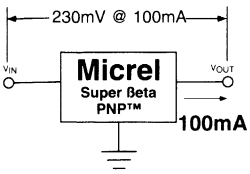
Device	V_{OUT}							Accuracy	I_{OUT} (mA)	Dropout Voltage @ I (Max. @ 25°C)	Features						Package
	3.0	3.3	4.85	5.0	12	15	Adjust.				I_{LIM}	Therm Protect	Error Flag	Logic Control	Reverse Supply	Load Dump	
MIC5200	•	•	•	•				1.0%	100	450mV	•	•		•	•		SO-8, SOT-223
MIC5202	•	•	•	•				1.0%	100 dual	450mV	•	•		•	•		SO-8
LP2950				•				0.5%	100	450mV	•	•					TO-92
								1.0%		@ 100mA							
LP2951							1.2 to 29	0.5%			•	•	•	•			P DIP, Cer DIP, SO-8
								1.0%									
MIC2950				•				0.5%	150	300mV	•	•			•	•	TO-92
								1.0%		@ 100mA							
MIC2951							1.2 to 29	0.5%			•	•	•	•	•	•	P DIP, CerDIP, SO-8
								1.0%									
MIC5201	•	•	•	•				1.0%	200	450mV	•	•		•	•		SO-8, SOT-223
MIC2954				•			1.2 to 29	0.5%	250	500mV	•	•	•	•	•	•	TO-92, TO-220
								1.0%		@ 250mA							SOT-223, SO-8
MIC2920A		•	•	•	•			1.0%	400	450mV	•	•			•	•	TO-220, SOT-223
MIC29201		•	•	•	•					@ 250mA	•	•	•	•	•	•	TO-220-5, TO-263-5
MIC29202							1.2 to 26			370mV typ.	•	•		•	•	•	TO-220-5, TO-263-5
MIC29203							1.2 to 26				•	•	•		•	•	TO-220-5, TO-263-5
MIC29204							1.2 to 26				•	•	•	•	•	•	P DIP, CerDIP, SO-8
MIC2937A		•		•	•	•		1.0%	750	450mV	•	•			•	•	TO-220, TO-263
										@ 500mA							
MIC29371		•		•	•	•				325mV typ	•	•	•	•	•	•	TO-220-5, TO-263-5
MIC29372							1.2 to 26				•	•		•	•	•	TO-220-5, TO-263-5
MIC29373							1.2 to 26				•	•	•		•	•	TO-220-5, TO-263-5
MIC2940A		•		•	•			1.0%	1250	450mV	•	•			•	•	TO-3, TO-220, TO-263
MIC2941A							1.2 to 26				•	•		•	•	•	TO-3, TO-220-5, TO-263-5

Low-Dropout Voltage Regulator Selector Guide

Device	V_{OUT}							Accuracy	I_{OUT} (A)	Dropout Voltage @ I (Max. @ 25°C)	Features						Package
	3.0	3.3	4.85	5.0	12	15	Adjust.				I_{LIM}	Therm Protect	Error Flag	Logic Control	Reverse Supply	Load Dump	
MIC29150		•		•	•			1%	1.5A	450mV	•	•			•	•	TO-220, TO-263, TO-3
MIC29151		•		•	•			1%	1.5A	450mV	•	•	•	•	•	•	TO-220, TO-263, TO-3
MIC29152							•	1%	1.5A	450mV	•	•		•	•	•	TO-220, TO-263
MIC29153							•	1%	1.5A	450mV	•	•	•		•	•	TO-220, TO-263
MIC29300		•		•	•			1%	3A	450mV	•	•			•	•	TO-220, TO-263, TO-3
MIC29301		•		•	•			1%	3A	450mV	•	•	•	•	•	•	TO-220, TO-263, TO-3
MIC29302							•	1%	3A	450mV	•	•		•	•	•	TO-220, TO-263
MIC29303							•	1%	3A	450mV	•	•	•		•	•	TO-220, TO-263
MIC29500		•		•	•			1%	5A	450mV	•	•			•	•	TO-220, TO-263, TO-3
MIC29501		•		•	•			1%	5A	450mV	•	•	•	•	•	•	TO-220, TO-263, TO-3
MIC29502							•	1%	5A	450mV	•	•		•	•	•	TO-220, TO-263
MIC29503							•	1%	5A	450mV	•	•	•		•	•	TO-220, TO-263
MIC29750		•		•	•			1%	7.5A	450mV	•	•			•	•	TO-3
MIC29751		•		•	•			1%	7.5A	450mV	•	•	•	•	•	•	TO-3
MIC29752							•	1%	7.5A	450mV	•	•		•	•	•	TO-3
MIC29753							•	1%	7.5A	450mV	•	•	•		•	•	TO-3
MIC5156		•		•			•	1%	①	①	•		•	•			SOIC, P DIP, CerDIP
MIC5157		②		②	②			1%	①	①	•		•	•			① Max. I_{OUT} and dropout determined by choice of extermal MOSFET
MIC5158				③			③	1%	①	①	•		•	•			② Selectable: 3.3V/5V/12V
																	③ Selectable: 5V/adjustable

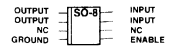
Micrel Super ßeta PNP™ LDO Family

MIC5200/5202



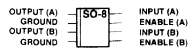
- Guaranteed 100mA output
- 3.3V, 4.5V, 4.75V, and 5.0V fixed
- 230mV drop out at 100mA
- Super ßeta PNP™ provides minimum ground current
- MIC5200 Single is available in SO-8 and SOT-223 Packages
- MIC5202 Dual is available in SO-8

MIC5200

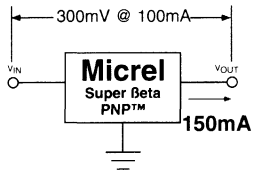


MIC5200

MIC5202



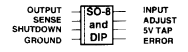
MIC2950



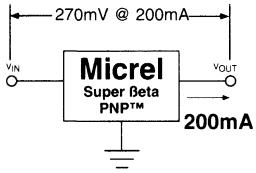
- Guaranteed 150mA output
- 5.0V fixed plus adjustable
- 370mV drop out at 150mA
- Super ßeta PNP™ provides minimum ground current
- Available in SO-8 and TO-92 Packages

MIC2950

MIC2951

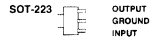


MIC5201

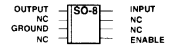


- Guaranteed 200mA output
- 3.3V, 4.5V, 4.75V, and 5.0V fixed
- <400mV drop out at 200mA
- Super ßeta PNP™ provides minimum ground current
- Available in SO-8 and SOT-223 Packages

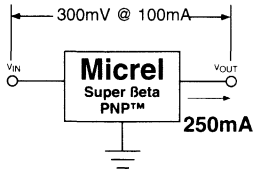
MIC5201



MIC5201



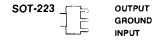
MIC2954



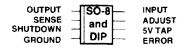
- Guaranteed 250mA output
- 5.0V fixed plus adjustable
- <450mV drop out at 250mA
- Super ßeta PNP™ provides minimum ground current
- Available in SO-8 and SOT-223, DIP, TO-220, and TO-92 Packages

MIC2954

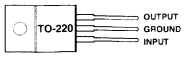
MIC2954



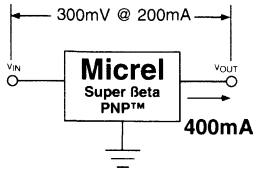
MIC2954



MIC2954

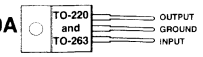


MIC2920A

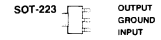


- Guaranteed 400mA output
- 3.3V, 4.85V, 5V, 12V fixed plus adjustable
- 450mV Drop out at 400mA
- Super ßeta PNP™ provides minimum ground current
- Available in SO-8, DIP, TO-220, and SOT-223 Packages

MIC2920A

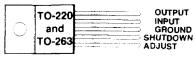


MIC2920A



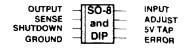
MIC29201

MIC29202



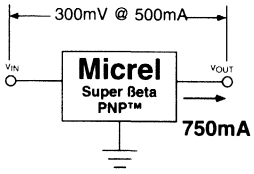
MIC29203

MIC29204

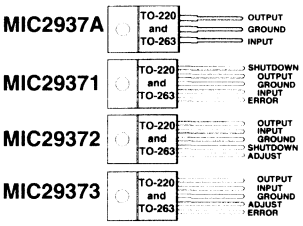


Micrel Super ßeta PNP™ LDO Family

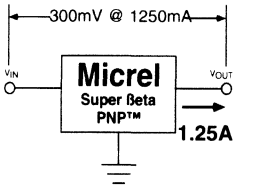
MIC2937A



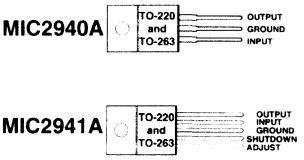
- Guaranteed 750mA output
- 3.3V, 5V, 12V fixed plus adjustable
- 370mV Drop out at 750mA
- Super ßeta PNP™ provides minimum ground current
- Available in TO-220 and TO-263 Packages



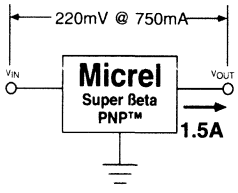
MIC2940A



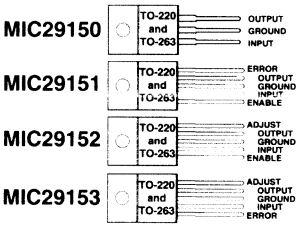
- Guaranteed 1250mA output
- 3.3V, 5V, 12V fixed plus adjustable
- 300mV Drop out at 1.25A
- Super ßeta PNP™ provides minimum ground current
- Available in TO-220, TO-263, and TO-3 Packages



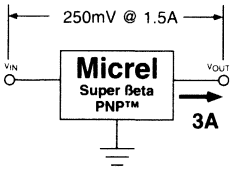
MIC29150



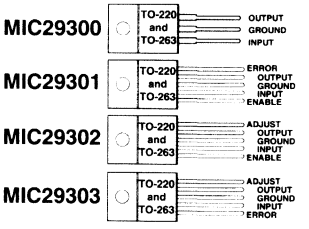
- Guaranteed 1.5A output
- 3.3V, 5V, 12V fixed plus adjustable
- <450mV Drop out at 1.5A
- Zero power shutdown mode
- Super ßeta PNP™ provides minimum ground current
- Available in TO-220 and TO-263 Packages



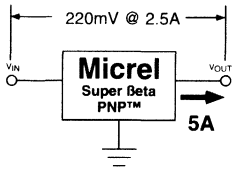
MIC29300



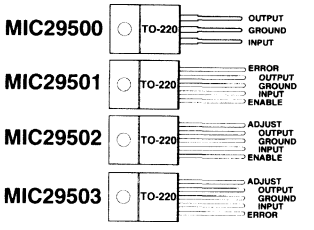
- Guaranteed 3A output
- 3.3V, 5V, 12V fixed plus adjustable
- <450mV Drop out at 3A
- Zero power shutdown mode
- Super ßeta PNP™ provides minimum ground current
- Available in TO-220 and TO-263 Packages



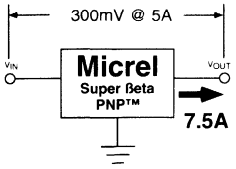
MIC29500



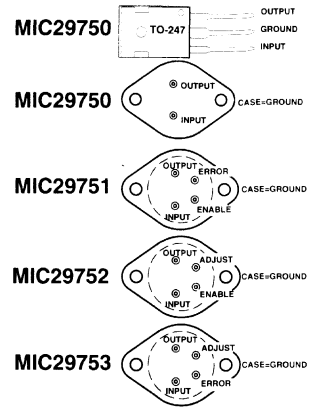
- Guaranteed 5A output
- 3.3V, 5V, 12V fixed plus adjustable
- <450mV Drop out at 5A
- Zero power shutdown mode
- Super ßeta PNP™ provides minimum ground current
- Available in TO-3 and TO-220 Packages (See MIC29750 for TO-3 pinout)



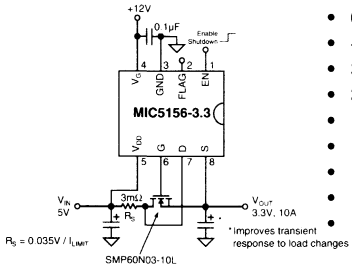
MIC29750



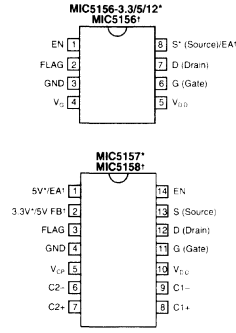
- Guaranteed 7.5A output
- 3.3V, 5V, 12V fixed plus adjustable
- 350mV Drop out at 7.5A
- Zero power shutdown mode
- Super ßeta PNP™ provides minimum ground current
- Available in TO-3 and TO-247 Packages



MIC5156/5157/5158



- 6mA typical operating current
- <1µA typical standby current
- 3.3V, 5V fixed output (MIC5156)
- 3.3V, 5V, 12V fixed output (MIC5157)
- 1.3V to 36V adjustable output (MIC5156/8)
- 1% initial output voltage tolerance
- Enable/shutdown control
- Internal gate-to-source protective clamp
- DIP and SOIC packages



LP2950 and LP2951

100mA Low Drop Out Voltage Regulator

General Description

The LP2950 and LP2951 are micropower voltage regulators with very low dropout voltage (typically 40mV at light loads and 380mV at 100mA), and very low quiescent current (75µA typical). The quiescent current of the LP2950/LP2951 increases only slightly in dropout, thus prolonging battery life. This feature, among others, makes the LP2950 and LP2951 ideally suited for use in battery-powered systems.

Available in a 3-Pin TO-92 package, the LP2950 is pin-compatible with the older 5V regulators. Plastic or ceramic DIP packages and additional system functions such as programmable output voltage and logic controlled shutdown are available with the 8-lead LP2951.

Applications

- Automotive Electronics
- Voltage Reference
- Avionics

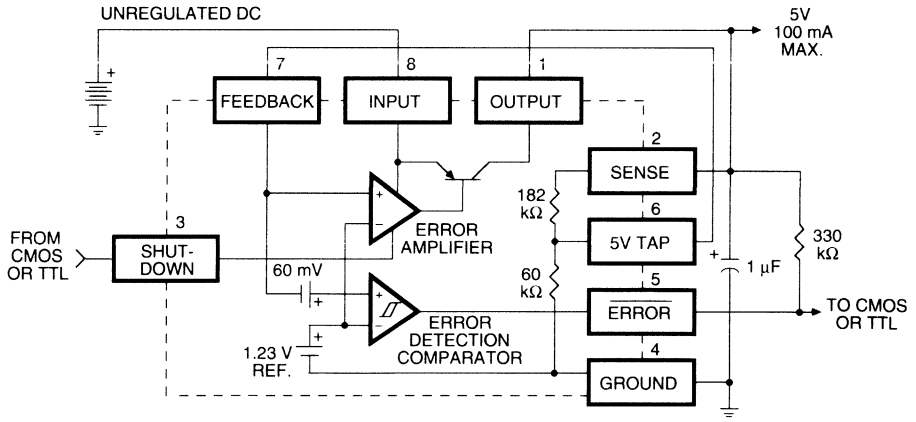
Features

- High accuracy 5V, guaranteed 100 mA output
- Extremely low quiescent current
- Low dropout voltage
- Extremely tight load and line regulation
- Very low temperature coefficient
- Use as regulator or reference
- Needs only 1µF for stability
- Current and thermal limiting

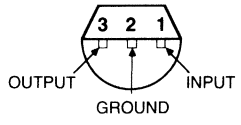
LP2951 Versions Only

- Error flag warns of output dropout
- Logic-controlled electronic shutdown
- Output programmable from 1.24 to 29V

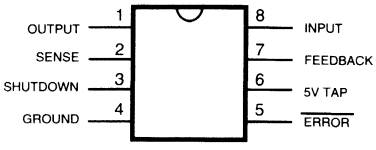
Block Diagram and Pin Configurations



LP2950 and LP2951 Block Diagram
(Pin Numbers Refer to LP2951)



TO-92 Plastic Package Bottom View
(BZ)



DIP and SO Packages
(AJ, BN, and BM)

See MIC2950 for a part with 1) higher output (150 mA), 2) transient protection (60V), and 3) reverse input protection to –20V)

Additional features available with the LP2951 also include an error flag output that warns of a low output voltage, which is often due to failing batteries on the input. This may also be used as a power-on reset. A logic-compatible shutdown input is also available which enables the regulator to be switched on and off. This part may also be pin-strapped for a 5V output, or programmed from 1.24V to 29V with the use of two external resistors.

The LP2950 is available as either an -02 or -03 version. The -02 and -03 versions are guaranteed for junction temperatures from –40°C to +125°C; the -02 version has a tighter output and reference voltage specification range over temperature. The LP2951 is available as an -01, -02 , or -03 version. The -01 version is guaranteed for junction temperatures from –55°C to +150°C, and has slightly different specifications limits over the full operating temperature range.

The LP2950 and LP2951 have a tight initial tolerance (0.5% typical), a very low output voltage temperature coefficient which allows use as a low-power voltage reference, and extremely good load and line regulation (0.05% typical). This greatly reduces the error in the overall circuit, and is the result of careful design techniques and process control.

Ordering Information

Part Number	Temperature Range*	Package
LP2950-02BZ LP2950-03BZ	–40°C to +125°C	3-pin TO-92 plastic
LP2951-02BM LP2951-03BM	–40°C to +125°C	8-pin SO-8
LP2951-01AJ	–55°C to +150°C	8-pin CERDIP
LP2951-02BJ LP2951-03BJ	–40°C to +125°C	8-pin CERDIP
LP2951-02BN LP2951-03BN	–40°C to +125°C	8-pin Plastic DIP

* Junction temperatures

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact your local Micrel representative/distributor for availability and specifications.

Power dissipation	Internally Limited
Lead Temperature (Soldering, 5 seconds)	260°C
Storage Temperature Range	–65°C to +150°C
Operating Junction Temperature Range (Note 8)	
LP2951-01	–55°C to +150°C
LP2950-02/LP2950-03, LP2951-02/LP2951-03	–40°C to +125°C
Input Supply Voltage	–0.3V to +30V
Feedback Input Voltage (Notes 9 and 10)	–1.5V to +30V
Shutdown Input Voltage (Note 9)	–0.3V to +30V
Error Comparator Output Voltage (Note 9)	–0.3V to +30V

ESD Rating is to be determined.

Electrical Characteristics (Note 1)

Parameter	Conditions (Note 2)	LP2951-01 Typ.	LP2951-01 Tested Limit (Note 3)	LP2950-02 LP2951-02 Typ.	LP2950-02 LP2951-02 Tested Limit (Note 3)	LP2950-02 LP2951-02 Design Limit (Note 4)	LP2950-03 LP2951-03 Typ.	LP2950-03 LP2951-03 Tested Limit (Note 3)	LP2950-03 LP2951-03 Design Limit (Note 4)	Units
Output Voltage	T_J = 25°C	5.000	5.025 4.975	5.000	5.025 4.975		5.000	5.050 4.950		V max V min
	–25°C ≤ T_J ≤ 85°C					5.050 4.950			5.075 4.925	V max V min
	Full Operating Temperature Range		**5.060** **4.940**			**5.060** **4.940**			**5.100** **4.900**	V max V min
Output Voltage	100µA ≤ I_L ≤ 100mA T_J ≤ $T_{J_{MAX}}$		**5.075** **4.925**			**5.070** **4.930**			**5.120** **4.880**	V max V min
Output Voltage Temperature Coefficient	(Note 12)	**20**	**120**	**20**		**100**	**50**		**150**	ppm/°C
Line Regulation (Note 14)	6V ≤ V_{IN} ≤ 30V (Note 15)	0.03	0.10 **0.50**	0.03	0.10	**0.20**	0.04	0.20	**0.40**	% max % max
Load Regulation (Note 14)	100µA ≤ I_L ≤ 100mA	0.04	0.10 **0.30**	0.04	0.10	**0.20**	0.10	0.20	**0.30**	% max % max
Dropout Voltage (Note 5)	I_L = 100µA	50	80 **150**	50	80	**150**	50	80	**150**	mV max mV max
	I_L = 100mA	380	450 **600**	380	450	**600**	380	450	**600**	mV max mV max
Ground Current	I_L = 100µA	100	150 **200**	100	150	**200**	100	150	**200**	µA max µA max
	I_L = 100mA	8	12 **14**	8	12	**14**	8	12	**14**	mA max mA max
Dropout Ground Current	V_{IN} = 4.5V I_L = 100µA	180	250 **310**	180	250	**310**	180	250	**310**	µA max µA max
Current Limit	V_{OUT} = 0V	160	200 **220**	160	200	**220**	160	200	**220**	mA max mA max
Thermal Regulation	(Note 13)	0.05	0.20	0.05	0.20		0.05	0.20		%/W max
Output Noise, 10 Hz to 100 kHz	C_L = 1µF	430		430			430			µV rms
	C_L = 200µF	160		160			160			µV rms
	C_L = 3.3µF (Bypass = 0.01µF Pins 7–1 (LP2951))	100		100			100			µV rms

6

Electrical Characteristics (Note 1) (Continued)

Parameter	Conditions (Note 2)	LP2951-01 Typ.	LP2951-01 Tested Limit (Note 3)	LP2951-02 Typ.	LP2951-02 Tested Limit (Note 3)	LP2951-02 Design Limit (Note 4)	LP2951-03 Typ.	LP2951-03 Tested Limit (Note 3)	LP2951-03 Design Limit (Note 4)	Units
Reference Voltage		1.235	1.250 **1.260** 1.220 **1.200**	1.235	1.250 1.220	 **1.260** **1.200**	1.235	1.260 1.210	 **1.270** **1.200**	V max V max V min V min
Reference Voltage	(Note 7)		**1.270** **1.190**			**1.270** **1.190**			**1.285** **1.185**	V max V min
Feedback Pin Bias Current		20	40 **60**	20	40	 **60**	20	40	 **60**	nA max nA max
Reference Voltage Temperature Coefficient	(Note 12)	20		20			50			ppm/°C
Feedback Pin Bias Current Temperature Coefficient		0.1		0.1			0.1			nA/°C
Output Leakage Current	V_{OH} = 30V	0.01	1.00 **2.00**	0.01	1.00	 **2.00**	0.01	1.00	 **2.00**	µA max µA max
Output Low Voltage	V_{IN} = 4.5V I_{OL} = 400µA	150	250 **400**	150	250	 **400**	150	250	 **400**	mV max mV max
Upper Threshold Voltage	(Note 6)	60	40 **25**	60	40	 **25**	60	40	 **25**	mV min mV min
Lower Threshold Voltage	(Note 6)	75	95 **140**	75	95	 **140**	75	95	 **140**	mV max mV max
Hysteresis(Note 6)		15		15			15			mV
Input Logic Voltage	 Low High	1.3	 **0.6** **2.0**	1.3		 **0.7** **2.0**	1.3		 **0.7** **2.0**	V V max V min
Shutdown Pin Input Current	$V_{SHUTDOWN}$ = 2.4V	30	50 **100**	30	50	 **100**	30	50	 **100**	µA max µA max
	$V_{SHUTDOWN}$ = 30V	450	600 **750**	450	600	 **750**	450	600	 **750**	µA max µA max
Regulator Output Current in Shutdown	(Note 11)	3	10 **20**	3	10	 **20**	3	10	 **20**	µA max µA max

Note 1: Boldface limits apply at temperature extremes.

Note 2: Unless otherwise specified all limits guaranteed for T_J = 25°C, V_{IN} = 6V, I_L = 100µA and C_L = 1µF. Additional conditions for the 8-pin versions are Feedback tied to 5V Tap and Output tied to Output Sense (V_{OUT} = 5V) and $V_{SHUTDOWN} \leq 0.8V$.

Note 3: Guaranteed and 100% production tested.

Note 4: Guaranteed but not 100% production tested. These limits are not used to calculate outgoing AQL levels.

Note 5: Dropout Voltage is defined as the input to output differential at which the output voltage drops 100mV below its nominal value measured at 1V differential. At very low values of programmed output voltage, the minimum input supply voltage of 2V (2.3V over temperature) must be taken into account.

Note 6: Comparator thresholds are expressed in terms of a voltage differential at the Feedback terminal below the nominal reference voltage measured at 6V input. To express these thresholds in terms of output voltage change, multiply by the error amplifier gain = V_{OUT}/V_{REF} = (R1 + R2)/R2. For example, at a programmed output voltage of 5V, the Error output is guaranteed to go low when the output drops by 95mV x 5V/1.235V = 384mV. Thresholds remain constant as a percent of VOUT as VOUT is varied, with the dropout warning occurring at typically 5% below nominal, 7.5% guaranteed.

Note 7: $V_{REF} \leq V_{OUT} \leq (V_{IN} - 1\ V)$, $2.3V \leq V_{IN} \leq 30V$, $100\mu A < I_L \leq 100mA$, $T_J \leq T_{JMAX}$.

Note 8: The junction-to-ambient thermal resistance of the TO-92 package is 180°C/W with 0.4" leads and 160°C/W with 0.25" leads to a PC board. The thermal resistances of the 8-Pin DIP packages are 105°C/W for the molded plastic (N) and 130°C/W for the CERAMIC DIP (J) junction to ambient when soldered directly to a PC board. Junction to ambient thermal resistance for the S.O. (M) package is 160°C/W.

Note 9: May exceed input supply voltage.

Note 10: When used in dual-supply systems where the output terminal sees loads returned to a negative supply, the output voltage should be diode-clamped to ground.

Note 11: $V_{SHUTDOWN} \geq 2V$, $V_{IN} \leq 30\ V$, $V_{OUT} = 0$, with Feedback pin tied to 5V Tap.

Note 12: Output or reference voltage temperature coefficient is defined as the worst case voltage change divided by the total temperature range.

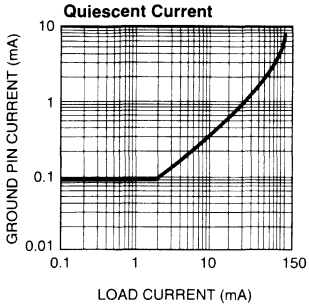
Note 13: Thermal regulation is defined as the change in output voltage at a time T after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for a 50mA load pulse at V_{IN} = 30V (1.25W pulse) for T = 10mS.

Note 14: Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered in the specification for thermal regulation.

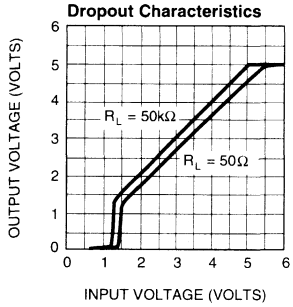
Note 15: Line regulation for the LP2951 is tested at 150°C for I_L = 1mA. For I_L = 100µA and T_J = 125°C, line regulation is guaranteed by design to 0.2%. See Typical Performance Characteristics for line regulation versus temperature and load current.

Typical Performance Characteristics

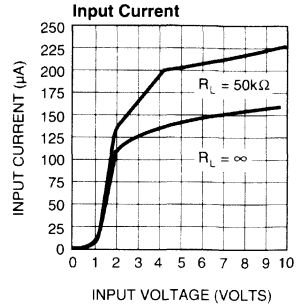
Quiescent Current



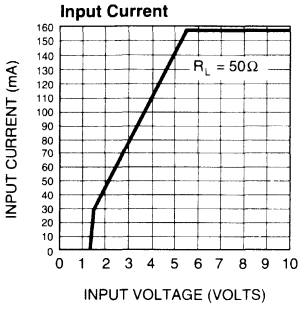
Dropout Characteristics



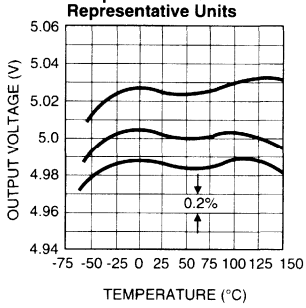
Input Current



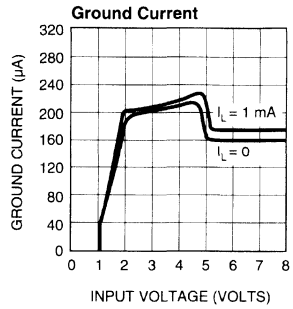
Input Current



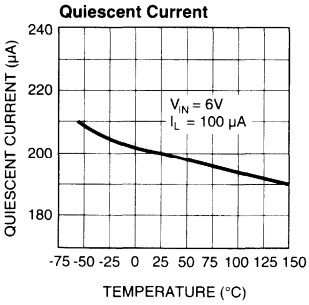
Output Voltage vs. Temperature of 3 Representative Units



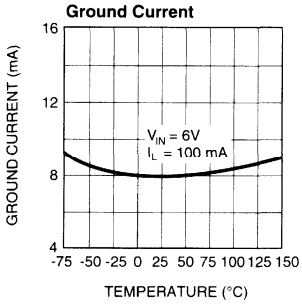
Ground Current



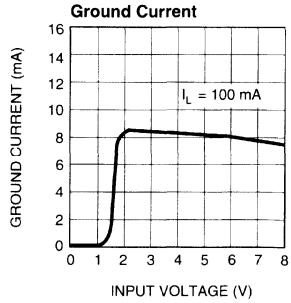
Quiescent Current



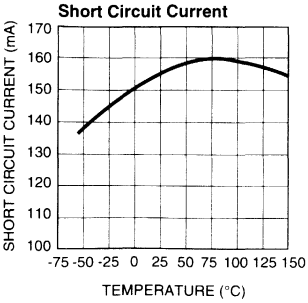
Ground Current



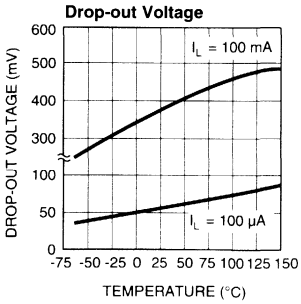
Ground Current



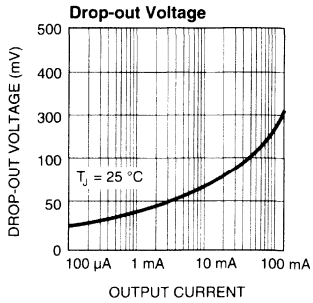
Short Circuit Current



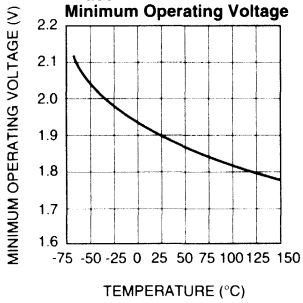
Drop-out Voltage



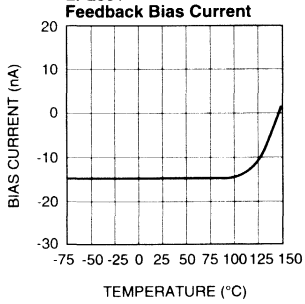
Drop-out Voltage



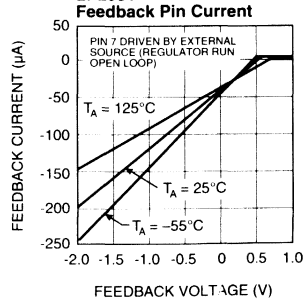
LP2951
Minimum Operating Voltage



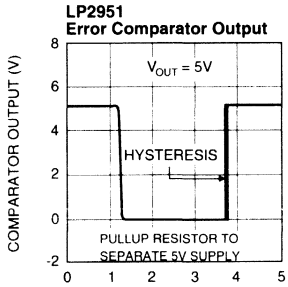
LP2951
Feedback Bias Current



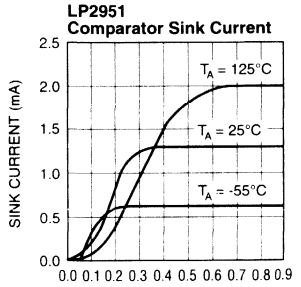
LP2951
Feedback Pin Current



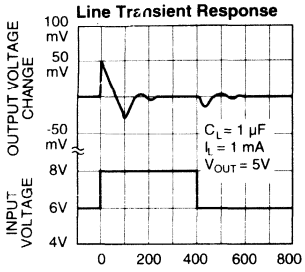
LP2951
Error Comparator Output



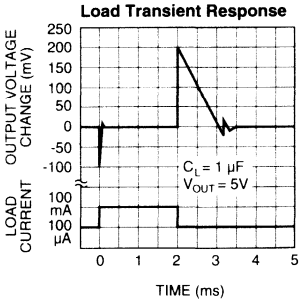
LP2951
Comparator Sink Current



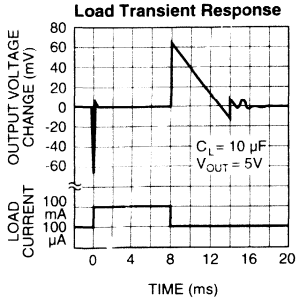
Line Transient Response



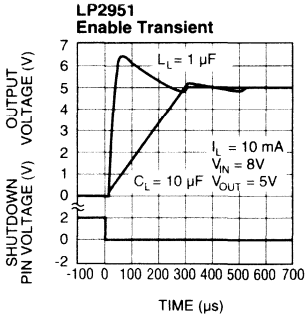
Load Transient Response



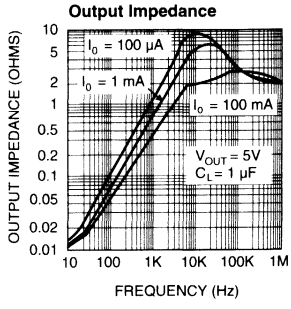
Load Transient Response



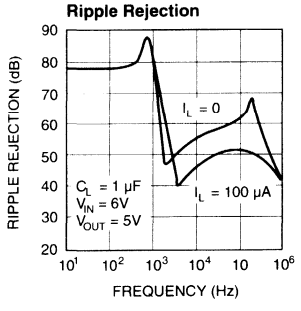
LP2951
Enable Transient



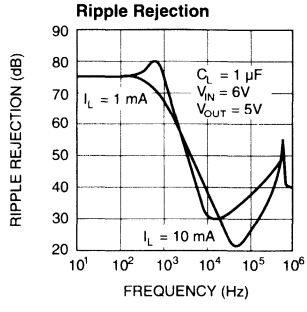
Output Impedance



Ripple Rejection



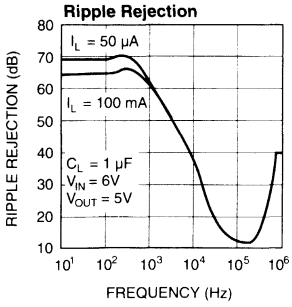
Ripple Rejection



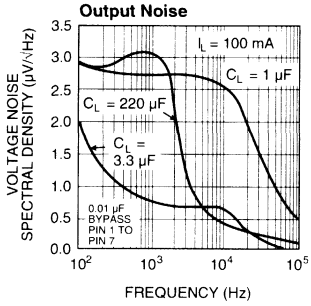
6

Typical Performance Characteristics (Continued)

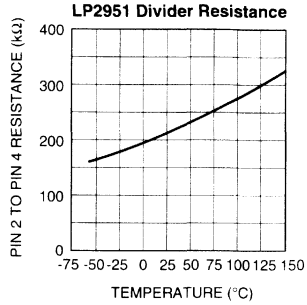
Ripple Rejection



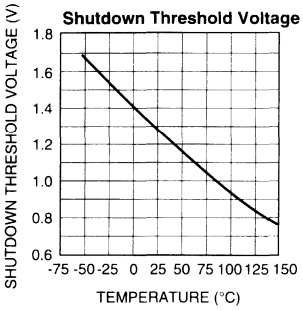
Output Noise



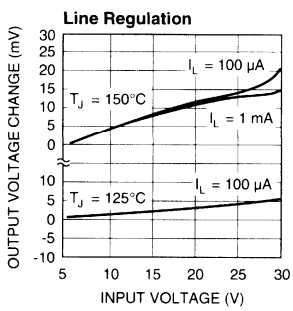
LP2951 Divider Resistance



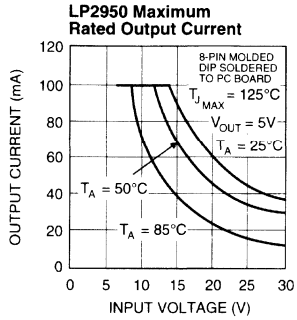
Shutdown Threshold Voltage



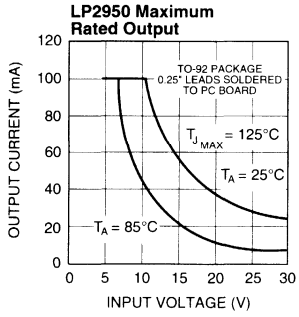
Line Regulation



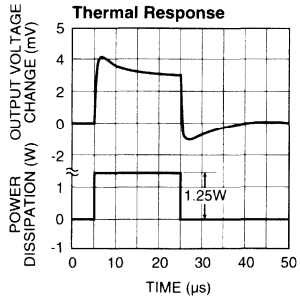
LP2950 Maximum Rated Output Current



LP2950 Maximum Rated Output



Thermal Response



Applications Information

External Capacitors

A 1.0µF (or greater) capacitor is required between the LP2950/LP2951 output and ground to prevent oscillations due to instability. Most types of tantalum or aluminum electrolytics will be adequate; film types will work, but are costly and therefore not recommended. Many aluminum electrolytics have electrolytes that freeze at about –30°C, so solid tantalum capacitors are recommended for operation below –25°C. The important parameters of the capacitor are an effective series resistance of about 5Ω or less and a resonant frequency above 500kHz. The value of this capacitor may be increased without limit.

At lower values of output current, less output capacitance is required for output stability. The capacitor can be reduced to 0.33µF for current below 10mA or 0.1µF for currents below 1mA. Using the 8-Pin versions at voltages below 5V runs the error amplifier at lower gains so that more output capacitance is needed. For the worst-case situation of a 100mA load at 1.23V output (Output shorted to Feedback) a 3.3µF (or greater) capacitor should be used.

The LP2950 will remain stable and in regulation with no load in addition to the internal voltage divider, unlike many other voltage regulators. This is especially important in CMOS RAM keep-alive applications. When setting the output voltage of the LP2951 version with external resistors, a minimum load of 1µA is recommended.

A 0.1µF capacitor should be placed from the LP2950/LP2951 input to ground if there is more than 10 inches of wire between the input and the AC filter capacitor or if a battery is used as the input.

Stray capacitance to the LP2951 Feedback terminal (pin 7) can cause instability. This may especially be a problem when using high value external resistors to set the output voltage. Adding a 100pF capacitor between Output and Feedback and increasing the output capacitor to at least 3.3µF will remedy this.

Error Detection Comparator Output

A logic low output will be produced by the comparator whenever the LP2951 output falls out of regulation by more than approximately 5%. This figure is the comparator's built-in offset of about 60mV divided by the 1.235V reference voltage. (Refer to the block diagram on Page 1). This trip level remains "5% below normal" regardless of the programmed output voltage of the LP2951. For example, the error flag trip level is typically 4.75V for a 5V output or 11.4V for a 12V output. The out of regulation condition may be due either to low input voltage, current limiting, or thermal limiting.

Figure 1 is a timing diagram depicting the $\overline{\text{ERROR}}$ signal and the regulated output voltage as the LP2951 input is ramped up and down. The $\overline{\text{ERROR}}$ signal becomes valid (low) at about 1.3V input. It goes high at about 5V input (the input voltage at which V_{OUT} = 4.75V). Since the LP2951's dropout voltage is load-dependent (see curve in Typical Performance Characteristics), the input voltage trip point (about 5V) will vary with the load current. The output voltage trip point (approximately 4.75V) does not vary with load.

The error comparator has an open-collector output which requires an external pull-up resistor. Depending on system requirements, this resistor may be returned to the 5V output or some other supply voltage. In determining a value for this resistor, note that while the output is rated to sink 400µA, this sink current adds to battery drain in a low battery condition. Suggested values range from 100k to 1MΩ. The resistor is not required if this output is unused.

In shutdown mode, $\overline{\text{ERROR}}$ will go high if it has been pulled up to an external 5V supply. To avoid this invalid response, ERROR should be pulled up to V_{OUT} (See figure 2).

Programming the Output Voltage (LP2951)

The LP2951 may be pin-strapped for 5V using its internal voltage divider by tying Pin 1 (output) to Pin 2 (SENSE) and Pin 7 (FEEDBACK) to Pin 6 (5V TAP). Alternatively, it may be programmed for any output voltage between its 1.235V reference and its 30V maximum rating. An external pair of resistors is required, as shown in Figure 2.

The complete equation for the output voltage is

$$V_{OUT} = V_{REF} \times \{ 1 + R_1/R_2 \} + I_{FB} R_2$$

where V_{REF} is the nominal 1.235 reference voltage and I_{FB} is the feedback pin bias current, nominally 20 nA. The minimum recommended load current of 1 µA forces an upper limit of 1.2 MΩ on the value of R_2, if the regulator must work with no load (a condition often found in CMOS in standby), I_{FB} will produce a 2% typical error in V_{OUT} which may be eliminated at room temperature by trimming R_1. For better accuracy, choosing R_2 = 100kΩ reduces this error to 0.17% while increasing the resistor program current to 12µA. Since the LP2951 typically draws 60 µA at no load with Pin 2 open-circuited, this is a small price to pay.

Reducing Output Noise

In reference applications it may be advantageous to reduce the AC noise present at the output. One method is to reduce the regulator bandwidth by increasing the size of the output capacitor. This is the only method by which noise can be reduced on the 3 lead LP2950 and is relatively inefficient, as increasing the capacitor from 1µF to 220µF only decreases the noise from 430µV to 160µV rms for a 100kHz bandwidth at 5V output.

Noise can be reduced fourfold by a bypass capacitor across R_1, since it reduces the high frequency gain from 4 to unity. Pick

$$C_{BYPASS} \cong \frac{1}{2\pi R_1 \bullet 200\ Hz}$$

or about 0.01 µF. When doing this, the output capacitor must be increased to 3.3 µF to maintain stability. These changes reduce the output noise from 430µV to 100µV rms for a 100kHz bandwidth at 5V output. With the bypass capacitor added, noise no longer scales with output voltage so that improvements are more dramatic at higher output voltages.

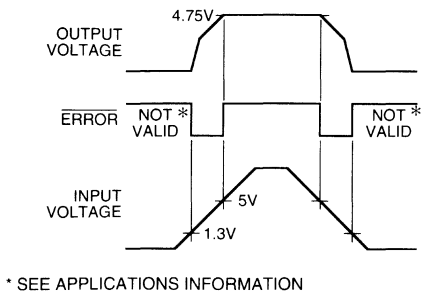


Figure 1. ERROR Output Timing

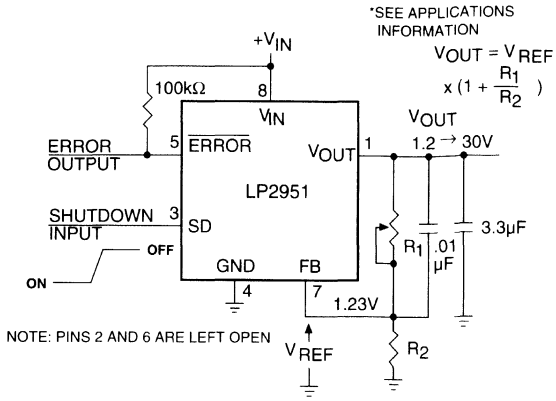
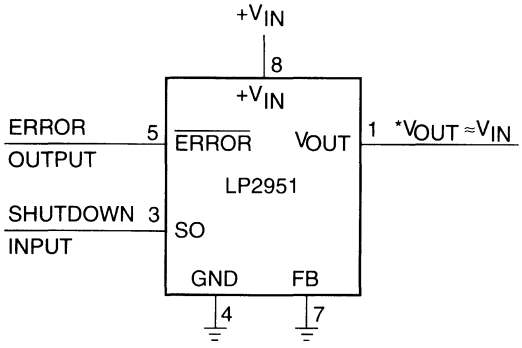


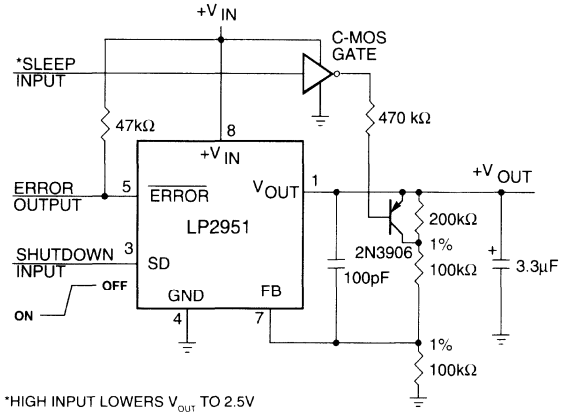
Figure 2. Adjustable Regulator

Typical Applications



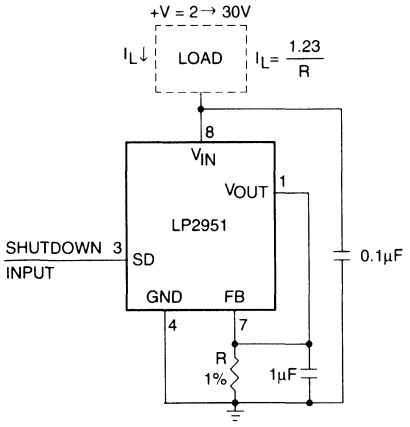
*MINIMUM INPUT-OUTPUT VOLTAGE RANGES FROM 40mV TO 400mV, DEPENDING ON LOAD CURRENT. CURRENT LIMIT IS TYPICALLY 160mA.

Wide Input Voltage Range Current Limiter

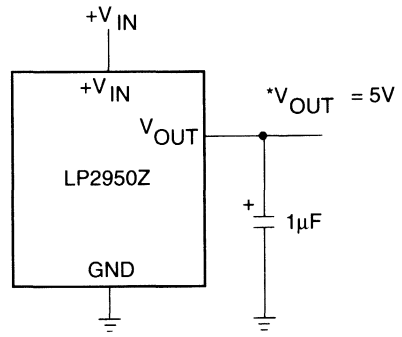


*HIGH INPUT LOWERS V_{OUT} TO 2.5V

5 V Regulator with 2.5 V Sleep Function

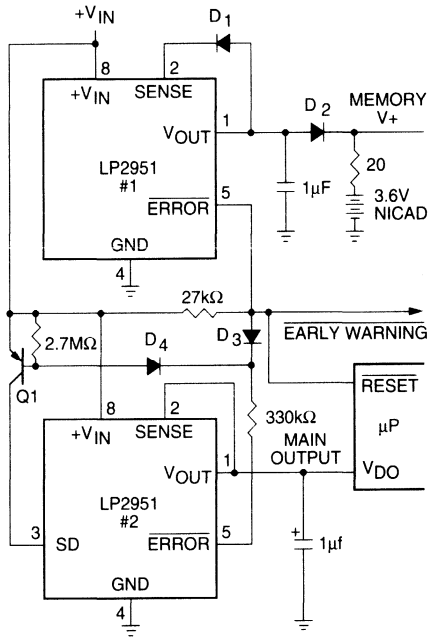


Low Drift Current Source



5 Volt Current Limiter

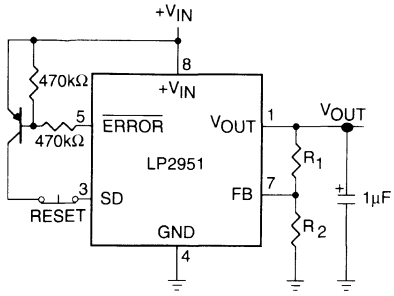
* MINIMUM INPUT-OUTPUT VOLTAGE RANGES FROM 40mV TO 400mV, DEPENDING ON LOAD CURRENT.



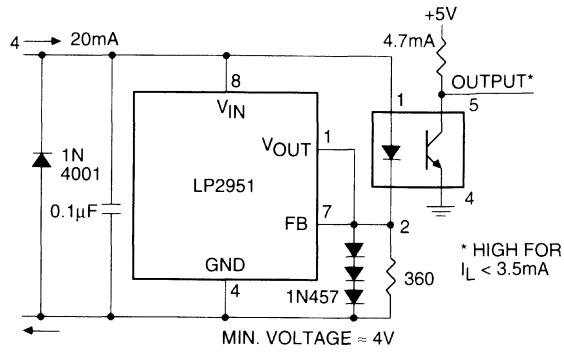
Regulator with Early Warning and Auxiliary Output

- EARLY WARNING FLAG ON LOW INPUT VOLTAGE
- MAIN OUTPUT LATCHES OFF AT LOWER INPUT VOLTAGES
- BATTERY BACKUP ON AUXILIARY OUTPUT

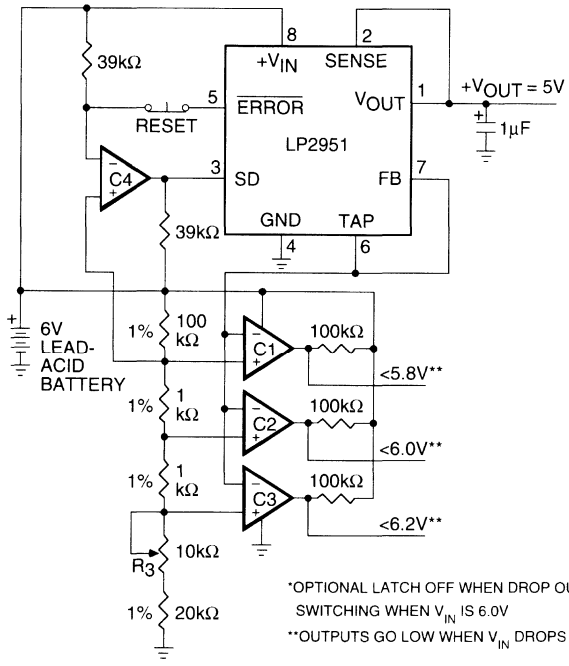
OPERATION: REG. #1'S V_{OUT} IS PROGRAMMED ONE DIODE DROP ABOVE 5 V. ITS ERROR FLAG BECOMES ACTIVE WHEN $V_{IN} \leq 5.7$ V. WHEN V_{IN} DROPS BELOW 5.3 V, THE ERROR FLAG OF REG. #2 BECOMES ACTIVE AND VIA Q1 LATCHES THE MAIN OUTPUT OFF. WHEN V_{IN} AGAIN EXCEEDS 5.7 V REG. #1 IS BACK IN REGULATION AND THE EARLY WARNING SIGNAL RISES, UNLATCHING REG. #2 VIA D3.



Latch Off When Error Flag Occurs



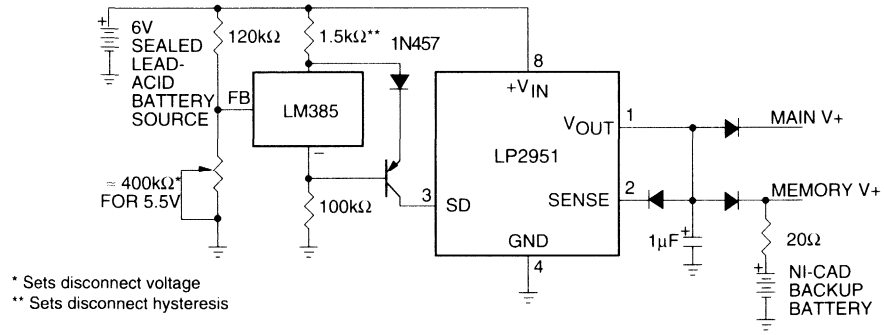
Open Circuit Detector for 4mA to 20mA Current Loop



*OPTIONAL LATCH OFF WHEN DROP OUT OCCURS. ADJUST R3 FOR C2 SWITCHING WHEN V_{IN} IS 6.0V

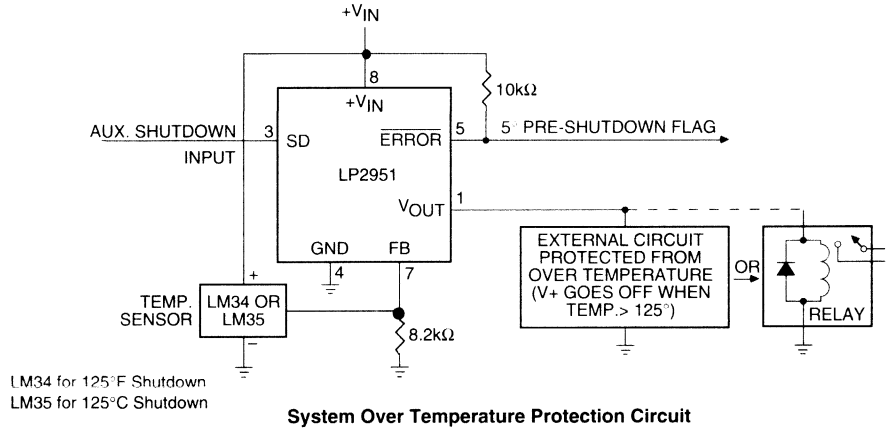
**OUTPUTS GO LOW WHEN V_{IN} DROPS BELOW DESIGNATED THRESHOLDS.

Regulator with State-of-Charge Indicator



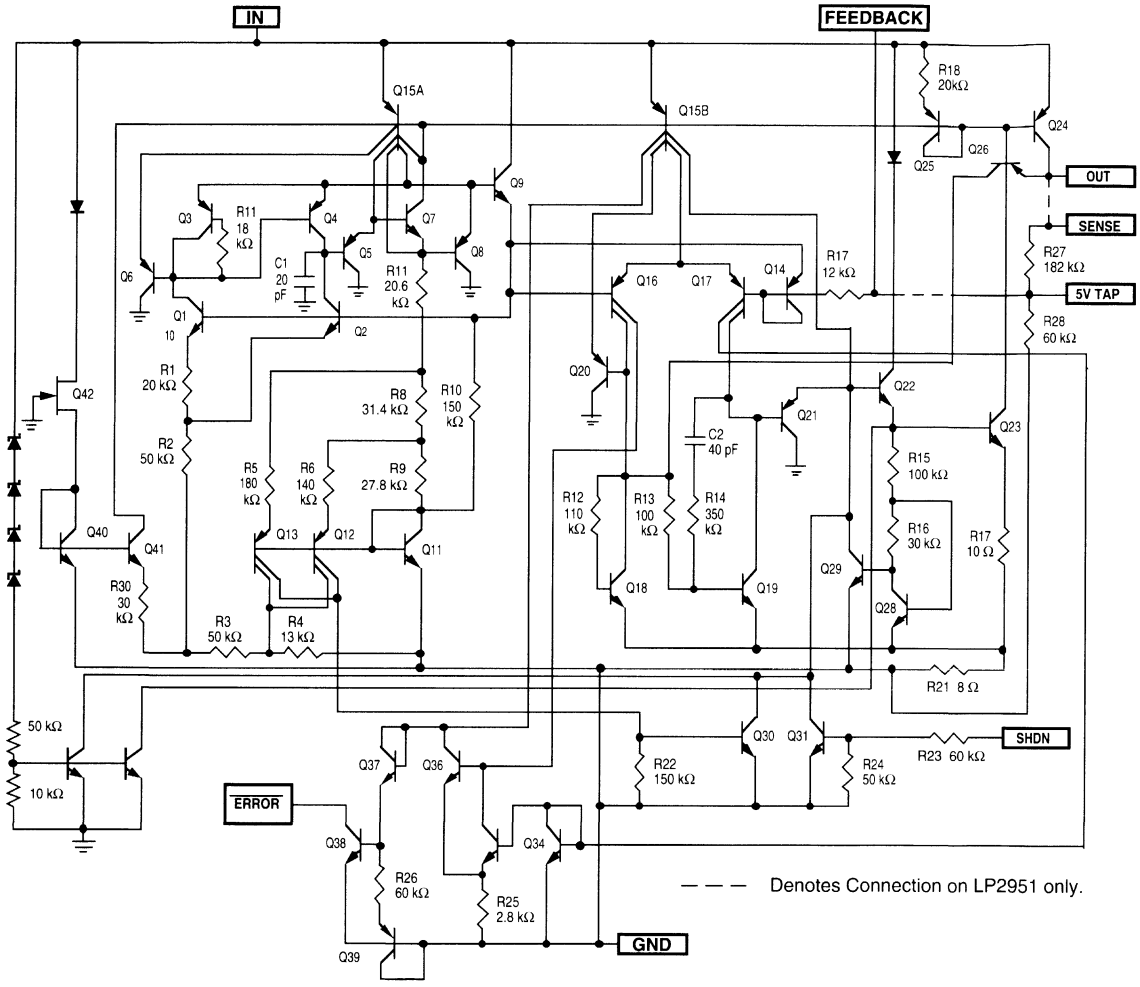
Low Battery Disconnect

For values shown, Regulator shuts down when V_{IN} < 5.5 V and turns on again at 6.0 V. Current drain in disconnected mode is 150µA.



System Over Temperature Protection Circuit

6


IN
FEEDBACK
Q15A
Q15B
R18
20kΩ
Q24
Q26
Q25
OUT
SENSE
R27
182 kΩ
5V TAP
R28
60 kΩ
Q9
Q3
R11
18
kΩ
Q4
Q7
Q5
Q8
Q6
C1
20
pF
R11
20.6
kΩ
Q1
10
Q2
R17
12 kΩ
Q16
Q17
Q14
Q20
Q22
Q21
Q23
C2
40 pF
R15
100 kΩ
R1
20 kΩ
R8
31.4 kΩ
R10
150
kΩ
Q42
R2
50 kΩ
R5
180
kΩ
R6
140
kΩ
R9
27.8 kΩ
R12
110
kΩ
R13
100
kΩ
R14
350
kΩ
R16
30 kΩ
R17
10 Ω
Q40
Q41
Q13
Q12
Q11
Q18
Q19
Q29
Q28
R30
30
kΩ
R3
50 kΩ
R4
13 kΩ
R21 8 Ω
50 kΩ
10 kΩ
Q30
Q31
SHDN
R23 60 kΩ
R22
150 kΩ
R24
50 kΩ
Q37
Q36
ERROR
Q38
Q34
R26
60 kΩ
R25
2.8 kΩ
Q39
GND
— — — Denotes Connection on LP2951 only.

MIC29150/300/500/750 Series

High Current Low Drop Out Regulators

Preliminary Information–Production Q2 '94

General Description

The MIC29150/29300/29500/29750 are high current, high accuracy, low drop out voltage regulators. Using Micrel's proprietary Super ßeta PNP™ process with a PNP pass element, these regulators feature 300mV (full load) dropout voltages and very low ground currents. Designed for high current loads, these devices also find applications in lower current, extremely low dropout-critical systems, where their tiny dropout voltage and ground current values are important attributes.

The MIC29150/29300/29500/29750 are fully protected against over-current faults, reversed input polarity, reversed lead insertion, over temperature operation, and positive and negative transient voltage spikes. Four and five pin fixed voltage versions feature logic level ON/OFF control and an error flag which signals whenever the output falls out of regulation. Flagged states include low input voltage (dropout), output current limit, overtemperature shutdown, and extremely high voltage spikes on the input.

On the MIC29xx1 and MIC29xx2, the ENABLE pin may be tied to V_{IN} if it is not required for ON/OFF control.

Features

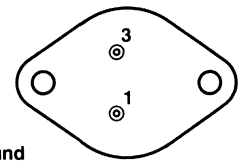
- High Current Capability
  - MIC29150/29151/29152/29153 ..... 1.5A
  - MIC29300/29301/29302/29303 ..... 3A
  - MIC29500/29501/29502/29503 ..... 5A
  - MIC29750/29751/29752/29753 ..... 7.5A
- Low Drop Out Voltage ..... <600mV at Full Load
- Low Ground Current
- Accurate 1% Guaranteed Tolerance
- Reverse-battery and "Load Dump" Protection
- Zero-Current Shutdown Mode (4 & 5 Pin versions)
- Error Flag Signals Output Out-of- Regulation (4 & 5 Pin versions)
- Also Characterized For Smaller Loads With Industry-Leading Performance Specifications
- Fixed Voltage and Adjustable Versions

Applications

- Battery Powered Equipment
- High Efficiency "Green" Computer Systems
- Automotive Electronics
- High Efficiency Linear Power Supplies
- High-Efficiency Post-Regulator For Switching Supply

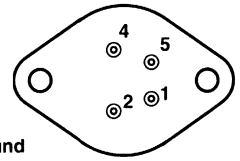
6

Pin Configuration



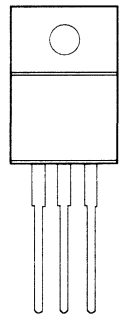
Case = Ground
(Bottom View)

MIC29500/29750BK



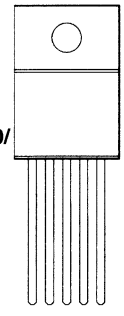
Case = Ground
(Bottom View)

MIC29501/29502/29503BK
MIC29751/29752/29753BK



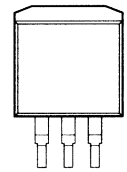
1 2 3

MIC29150/29300/29500BT



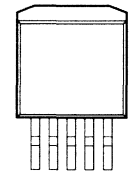
1 2 3 4 5

MIC29151/29152/29153BT
MIC29301/29302/29303BT
MIC29501/29502/29503BT



1 2 3

MIC29150/29300BU



1 2 3 4 5

MIC29151/29152/29153BU
MIC29301/29302/29303BU

Pinout **On all devices, the Tab is grounded.**

MIC29150/29300/29500/29750 Three Terminal Devices:

Pin 1 = Input, 2 = Ground, 3 = Output

MIC29151/29301/29501/29751 Four & Five Terminal Fixed Voltage Devices:

Pin 1 = Enable, 2 = Input, 3 = Ground, 4 = Output, 5 = Flag

MIC29152/29302/29502/29752 Adjustable with ON/OFF Control

Pin 1 = Enable, 2 = Input, 3 = Ground, 4 = Output, 5 = Adjust

MIC29153/29303/29503/29753 Adjustable with Flag

Pin 1 = Flag, 2 = Input, 3 = Ground, 4 = Output, 5 = Adjust

Ordering Information

Part Number	Temp. Range*	Volts	Current	Package
MIC29150-3.3BK	–40 to +125°C	3.3	1.5A	TO-3
MIC29150-5.0BK	–40 to +125°C	5.0	1.5A	TO-3
MIC29150-12BK	–40 to +125°C	12	1.5A	TO-3
MIC29150-3.3BT	–40 to +125°C	3.3	1.5A	TO-220
MIC29150-3.6BT	–40 to +125°C	3.6	1.5A	TO-220
MIC29150-5.0BT	–40 to +125°C	5.0	1.5A	TO-220
MIC29150-12BT	–40 to +125°C	12	1.5A	TO-220
MIC29150-3.3BU	–40 to +125°C	3.3	1.5A	TO-263
MIC29150-5.0BU	–40 to +125°C	5.0	1.5A	TO-263
MIC29150-12BU	–40 to +125°C	12	1.5A	TO-263
MIC29151-3.3BK	–40 to +125°C	3.3	1.5A	TO-3-4
MIC29151-5.0BK	–40 to +125°C	5.0	1.5A	TO-3-4
MIC29151-12BK	–40 to +125°C	12	1.5A	TO-3-4
MIC29151-3.3BT	–40 to +125°C	3.3	1.5A	TO-220-5
MIC29151-3.6BT	–40 to +125°C	3.6	1.5A	TO-220-5
MIC29151-5.0BT	–40 to +125°C	5.0	1.5A	TO-220-5
MIC29151-12BT	–40 to +125°C	12	1.5A	TO-220-5
MIC29151-3.3BU	–40 to +125°C	3.3	1.5A	TO-263-5
MIC29151-5.0BU	–40 to +125°C	5.0	1.5A	TO-263-5
MIC29151-12BU	–40 to +125°C	12	1.5A	TO-263-5
MIC29152BT	–40 to +125°C	Adj	1.5A	TO-220-5
MIC29152BU	–40 to +125°C	Adj	1.5A	TO-263-5
MIC29153BT	–40 to +125°C	Adj	1.5A	TO-220-5
MIC29153BU	–40 to +125°C	Adj	1.5A	TO-263-5
MIC29300-3.3BK	–40 to +125°C	3.3	3.0A	TO-3
MIC29300-5.0BK	–40 to +125°C	5.0	3.0A	TO-3
MIC29300-12BK	–40 to +125°C	12	3.0A	TO-3
MIC29300-3.3BT	–40 to +125°C	3.3	3.0A	TO-220
MIC29300-5.0BT	–40 to +125°C	5.0	3.0A	TO-220
MIC29300-12BT	–40 to +125°C	12	3.0A	TO-220
MIC29300-3.3BU	–40 to +125°C	3.3	3.0A	TO-263
MIC29300-5.0BU	–40 to +125°C	5.0	3.0A	TO-263
MIC29300-12BU	–40 to +125°C	12	3.0A	TO-263
MIC29301-3.3BK	–40 to +125°C	3.3	3.0A	TO-3-4
MIC29301-5.0BK	–40 to +125°C	5.0	3.0A	TO-3-4
MIC29301-12BK	–40 to +125°C	12	3.0A	TO-3-4
MIC29301-3.3BT	–40 to +125°C	3.3	3.0A	TO-220-5
MIC29301-5.0BT	–40 to +125°C	5.0	3.0A	TO-220-5
MIC29301-12BT	–40 to +125°C	12	3.0A	TO-220-5
MIC29301-3.3BU	–40 to +125°C	3.3	3.0A	TO-263-5
MIC29301-5.0BU	–40 to +125°C	5.0	3.0A	TO-263-5
MIC29301-12BU	–40 to +125°C	12	3.0A	TO-263-5

Part Number	Temp. Range*	Volts	Current	Package
MIC29302BT	–40 to +125°C	Adj	3.0A	TO-220-5
MIC29302BU	–40 to +125°C	Adj	3.0A	TO-263-5
MIC29303BT	–40 to +125°C	Adj	3.0A	TO-220-5
MIC29303BU	–40 to +125°C	Adj	3.0A	TO-263-5
MIC29500-3.3BK	–40 to +125°C	3.3	5.0A	TO-3
MIC29500-5.0BK	–40 to +125°C	5.0	5.0A	TO-3
MIC29500-12BK	–40 to +125°C	12	5.0A	TO-3
MIC29500-3.3BT	–40 to +125°C	3.3	5.0A	TO-220
MIC29500-5.0BT	–40 to +125°C	5.0	5.0A	TO-220
MIC29500-12BT	–40 to +125°C	12	5.0A	TO-220
MIC29501-3.3BK	–40 to +125°C	3.3	5.0A	TO-3-4
MIC29501-5.0BK	–40 to +125°C	5.0	5.0A	TO-3-4
MIC29501-12BK	–40 to +125°C	12	5.0A	TO-3-4
MIC29501-3.3BT	–40 to +125°C	3.3	5.0A	TO-220-5
MIC29501-5.0BT	–40 to +125°C	5.0	5.0A	TO-220-5
MIC29501-12BT	–40 to +125°C	12	5.0A	TO-220-5
MIC29501-3.3BU	–40 to +125°C	3.3	5.0A	TO-263-5
MIC29501-5.0BU	–40 to +125°C	5.0	5.0A	TO-263-5
MIC29501-12BU	–40 to +125°C	12	5.0A	TO-263-5
MIC29502BT	–40 to +125°C	Adj	5.0A	TO-220-5
MIC29502BU	–40 to +125°C	Adj	5.0A	TO-263-5
MIC29503BT	–40 to +125°C	Adj	5.0A	TO-220-5
MIC29503BU	–40 to +125°C	Adj	5.0A	TO-263-5
MIC29750-3.3BK	–40 to +125°C	3.3	7.5A	TO-3
MIC29750-5.0BK	–40 to +125°C	5.0	7.5A	TO-3
MIC29750-12BK	–40 to +125°C	12	7.5A	TO-3
MIC29751-3.3BK	–40 to +125°C	3.3	7.5A	TO-3-4
MIC29751-5.0BK	–40 to +125°C	5.0	7.5A	TO-3-4
MIC29751-12BK	–40 to +125°C	12	7.5A	TO-3-4
MIC29752BK	–40 to +125°C	Adj	7.5A	TO-3-4
MIC29753BK	–40 to +125°C	Adj	7.5A	TO-3-4

* Junction Temperature

MIC29xx0 versions are three terminal fixed voltage devices. MIC29xx1 are fixed voltage devices with ENABLE and ERROR flag. MIC29xx2 are adjustable regulators with ENABLE control. MIC29xx3 are adjustables with an ERROR flag.

Absolute Maximum Ratings

Power Dissipation ..... Internally Limited
Lead Temperature (Soldering, 5 seconds) ..... 260°C
Storage Temperature Range ..... –65°C to +150°C
Input Supply Voltage (Note 1) ..... –20V to +60V

Operating Ratings

Operating Junction Temperature ..... –40°C to +125°C
TO-220 θ_{JC} ..... 2 °C/W
TO-263 θ_{JC} ..... 2 °C/W
TO-247 θ_{JC} ..... 1.5 °C/W
TO-3 θ_{JC} ..... 1 °C/W

Electrical Characteristics

All measurements at T_J = 25°C unless otherwise noted. **Bold** values are guaranteed across the operating temperature range.

Parameter	Condition	Min	Typ	Max	Units
Output Voltage	I_O = 10mA	–1		1	%
	10mA ≤ I_O ≤ I_{FL}, (V_{OUT} + 1V) ≤ V_{IN} ≤ 25V	**–2**		**2**	%
Line Regulation	I_O = 10mA, (V_{OUT} + 1V) ≤ V_{IN} ≤ 26V		0.06	0.5	%
Load Regulation	V_{IN} = V_{OUT} + 5V, 10mA ≤ I_{OUT} ≤ $I_{FULL\ LOAD}$ (Note 6)		0.2	1	%
ΔV_O / ΔT	Output Voltage (Note 6) Temperature Coef.		**20**	**100**	ppm/°C
Dropout Voltage	ΔV_{OUT} = – 1%, (Note 3)				
	MIC29150 I_O = 100mA		80	**200**	mV
	I_O = 750mA		220		
	I_O = 1.5A			**600**	
	MIC29300 I_O = 100mA		80	**175**	
	I_O = 1.5A		250		
	I_O = 3A		370	**600**	
	MIC29500 I_O = 250mA		125	**250**	
	I_O = 2.5A		220		
	I_O = 5A		370	**600**	
	MIC29750 I_O = 250mA		80	**200**	
	I_O = 4A		240		
	I_O = 7.5A		350	**600**	
Ground Current	MIC29150 I_O = 750mA, V_{IN} = V_{OUT} + 1V		8	**20**	mA
	I_O = 1.5A		25		
	MIC29300 I_O = 1.5A, V_{IN} = V_{OUT} + 1V		10	**35**	mA
	I_O = 3A		37		
	MIC29500 I_O = 2.5A, V_{IN} = V_{OUT} + 1V		15	**50**	mA
	I_O = 5A		70	**85**	
	MIC29750 I_O = 4A, V_{IN} = V_{OUT} + 1V		28	**75**	mA
	I_O = 7.5A		70		
I_{GNDDO} Ground Pin Current at Dropout	V_{IN} = 0.5V less than specified V_{OUT}. I_{OUT} = 10mA		180	**300**	µA
Current Limit	MIC29150 V_{OUT} = 0V (Note 4)	1.5	2.1		A
	MIC29300 V_{OUT} = 0V (Note 4)	3.0	4.5		A
	MIC29500 V_{OUT} = 0V (Note 4)	5.0	7.5		A
	MIC29750 V_{OUT} = 0V (Note 4)	7.5	9.5		A
e_n, Output Noise Voltage (10Hz to 100kHz) I_L = 100mA	C_L = 10µF		400		µV RMS
	C_L = 33µF		260		

6

Electrical Characteristics (Continued)

Reference **MIC29xx2/MIC29xx3**

Parameter	Conditions	Min	Typical	Max	Units
Reference Voltage		1.210 **1.200**	1.235	1.260 **1.270**	V V max
Reference Voltage	(Note 8)	**1.185**		**1.285**	V
Adjust Pin Bias Current			20	40 **60**	nA
Reference Voltage Temperature Coefficient	(Note 7)		20		ppm/°C
Adjust Pin Bias Current Temperature Coefficient			0.1		nA/°C
Error Comparator	**MIC29xx1/29xx3**				
Output Leakage Current	V_{OH} = 26V		0.01	1.00 **2.00**	µA
Output Low Voltage	Deviceset for 5V. V_{IN} = 4.5V I_{OL} = 250µA		220	300 **400**	mV
Upper Threshold Voltage	Deviceset for 5V (Note 9)	40 **25**	60		mV
Lower Threshold Voltage	Deviceset for 5V (Note 9)		75	95 **140**	mV
Hysteresis	Deviceset for 5V (Note 9)		15		mV
ENABLE Input	**MIC29xx1/MIC29xx2**				
Input Logic Voltage Low (OFF) High (ON)		 **2.4**		**0.8**	V
ENABLE Pin Input Current	$V_{SHUTDOWN}$ = 26V		15	30 **75**	µA
	$V_{SHUTDOWN}$ =0.8V		–	1 **2**	µA
Regulator Output Current in Shutdown	(Note 10)		10	 **20**	µA

Notes

Note1: Maximum positive supply voltage of 60V must be of limited duration (<100msec) and duty cycle (≤1%). The maximum continuous supply voltage is 26V.

Note 2: Full Load current is defined as 1.5A for the MIC29150, 3A for the MIC29300, 5A for the MIC29500, and 7.5A for the MIC29750 families.

Note 3: Dropout voltage is defined as the input-to-output differential when the output voltage drops to 99% of its nominal value with V_{OUT} + 1V applied to V_{IN}

Note 4: V_{IN} is the larger of 8V or V_{OUT} + 3V

Note 5: Ground pin current is the regulator quiescent current. The total current drawn from the source is the sum of the load current plus the ground pin current.

Note 6: Output voltage temperature coefficient is defined as the worst case voltage change divided by the total temperature range.

Note 7: Thermal regulation is defined as the change in output voltage at a time T after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for a 200mA load pulse at V_{IN} = 20V (a 4W pulse) for T = 10ms.

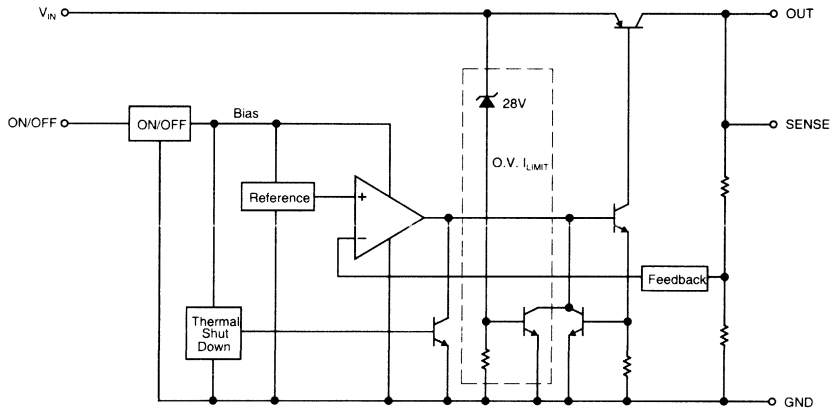
Note 8: $V_{REF} \leq V_{OUT} \leq (V_{IN} - 1\ V)$, $2.3V \leq V_{IN} \leq 26V$, $5mA < I_L \leq 1.25A$, $T_J \leq T_{J\ MAX}$.

Note 9: Comparator thresholds are expressed in terms of a voltage differential at the Adjust terminal below the nominal reference voltage measured at 6V input. To express these thresholds in terms of output voltage change, multiply by the error amplifier gain = V_{OUT} /V_{REF} = (R1 + R2)/R2. For example, at a programmed output voltage of 5V, the Error output is guaranteed to go low when the output drops by 95 mV x 5V/1.235 V = 384 mV. Thresholds remain constant as a percent of V_{OUT} as V_{OUT} is varied, with the dropout warning occurring at typically 5% below nominal, 7.5% guaranteed.

Note 10: $V_{ENABLE} \leq 0.8V$ and $V_{IN} \leq 26V$, $V_{OUT} = 0$.

Note 11: When used in dual supply systems where the regulator load is returned to a negative supply, the output voltage must be diode clamped to ground.

Block Diagram



Typical Applications

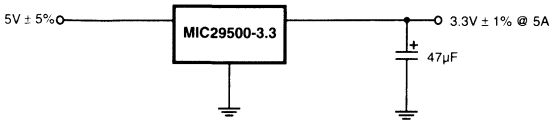
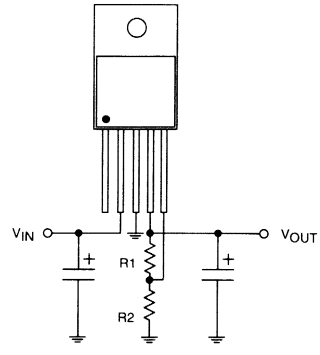


Figure 1. Fixed output voltage.

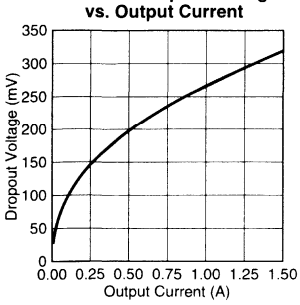


$V_{OUT} = 1.235V \times [1 + (R1 / R2)]$

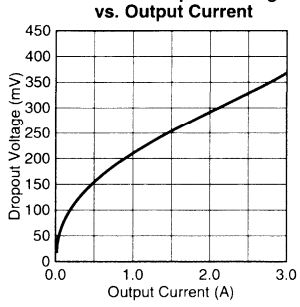
Figure 2. Adjustable output voltage configuration. For best results, the total series resistance should be small enough to pass the minimum regulator load current.

Typical Characteristics

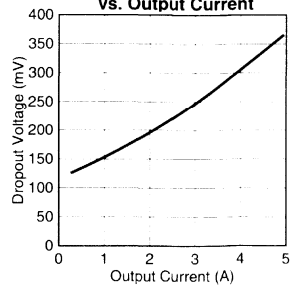
MIC29150 Dropout Voltage vs. Output Current



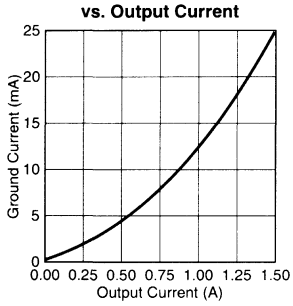
MIC29300 Dropout Voltage vs. Output Current



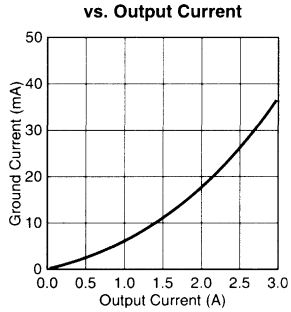
MI29500 Dropout Voltage vs. Output Current



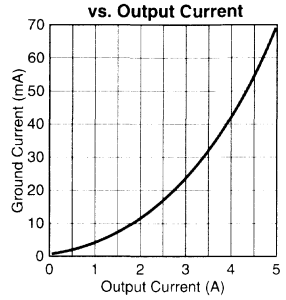
MIC29150 Ground Current vs. Output Current



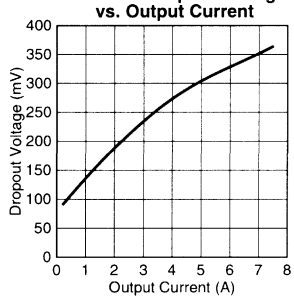
MIC29300 Ground Current vs. Output Current



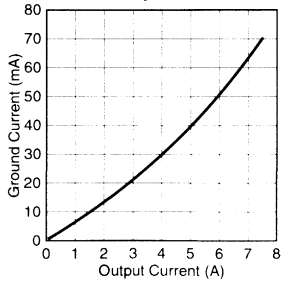
MIC29500 Ground Current vs. Output Current



MIC29750 Dropout Voltage vs. Output Current



MIC29750 Ground Current vs. Output Current



MIC2920A, 29201/202/203/204

400mA Low Drop Out Voltage Regulator

Preliminary Information–Production Q1 '94

General Description

The MIC2920A family are "bulletproof" efficient voltage regulators with very low drop out voltage (typically 40mV at light loads and 300mV at 250mA), and very low quiescent current (90µA typical). The quiescent current of the MIC2920A increases only slightly in dropout, thus prolonging battery life. Key MIC2920A features include protection against reversed battery, fold-back current limiting, and automotive "load dump" protection (60V positive transient).

The MIC2920 is available in several configurations. The MIC2920A-xx devices are three pin fixed voltage regulators. The MIC29201 is a fixed regulator offering logic compatible ON/OFF switching input and an error flag output. This flag may also be used as a power-on reset signal. A logic-compatible shutdown input is provided on the adjustable MIC29202, which enables the regulator to be switched on and off. The MIC29203 is a five pin adjustable version that includes an error flag output that warns of a low output voltage, which is often due to failing batteries on the input. The eight pin DIP and SOIC adjustable version, the MIC29204, includes both shutdown and error flag pins, and may be pin-strapped for 5V output, or programmed from 1.24 V to 29 V with the use of two external resistors.

Features

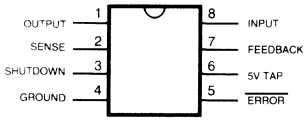
- High output voltage accuracy
- Guaranteed 400mA output
- Low quiescent current
- Low dropout voltage
- Extremely tight load and line regulation
- Very low temperature coefficient
- Current and thermal limiting
- Input can withstand –20V reverse battery and +60V positive transients
- Error flag warns of output dropout
- Logic-controlled electronic shutdown
- Output programmable from 1.24V to 26V (MIC29202/ MIC29203/MIC29204)
- Available in TO-220, TO-220-5, DIP, CerDIP, and Surface Mount TO-263-5, SOT-223, and SO-8 packages.

Applications

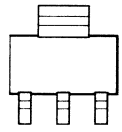
- Battery Powered Equipment
- Cellular Telephones
- Laptop, Notebook, and Palmtop Computers
- PCMCIA V_{CC} and V_{PP} Regulation/Switching
- Bar Code Scanners
- Automotive Electronics
- SMPS Post-Regulator/ DC to DC Modules
- Voltage Reference
- High Efficiency Linear Power Supplies

6

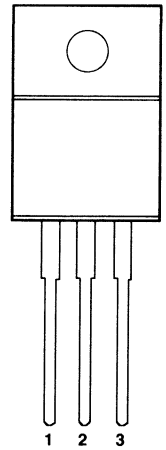
Pin Configuration



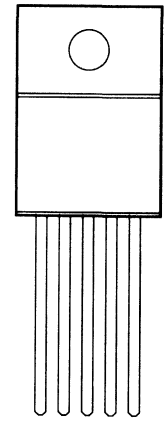
SO/DIP Packages (MIC29204BJ/M/N)



SOT-223 Package (MIC2920A-xxBS)



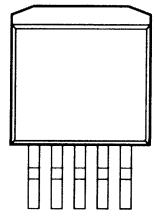
TO-220 Package (MIC2920A-xxBT)



TO-220-5 Package (MIC29201/29202/29203BT)

Five Lead Package Pin Functions:

	MIC29201	MIC29202	MIC29203
1)	Error	Adjust	Error
2)	Input	Shutdown	Adjust
3)	Ground	Ground	Ground
4)	Output	Input	Input
5)	Shutdown	Output	Output



TO-263-5 Package (MIC29201/29202/29203BU)

The TAB is Ground on the SOT-223, TO-220, and TO-263 packages.

Ordering Information

Part Number	Voltage	Temperature Range*	Package
MIC2920A-3.3BS	3.3	–40°C to +125°C	SOT-223
MIC2920A-3.3BT	3.3	–40°C to +125°C	TO-220
MIC2920A-4.8BS	4.85	–40°C to +125°C	SOT-223
MIC2920A-4.8BT	4.85	–40°C to +125°C	TO-220
MIC2920A-5.0BS	5.0	–40°C to +125°C	SOT-223
MIC2920A-5.0BT	5.0	–40°C to +125°C	TO-220
MIC2920A-12BS	12	–40°C to +125°C	SOT-223
MIC2920A-12BT	12	–40°C to +125°C	TO-220
MIC29201-3.3BT	3.3	–40°C to +125°C	TO-220-5
MIC29201-3.3BU	3.3	–40°C to +125°C	TO-263-5
MIC29201-4.8BT	4.85	–40°C to +125°C	TO-220-5
MIC29201-4.8BU	4.85	–40°C to +125°C	TO-263-5
MIC29201-5.0BT	5.0	–40°C to +125°C	TO-220-5
MIC29201-5.0BU	5.0	–40°C to +125°C	TO-263-5
MIC29201-12BT	12	–40°C to +125°C	TO-220-5
MIC29201-12BU	12	–40°C to +125°C	TO-263-5
MIC29202BT	Adj	–40°C to +125°C	TO-220-5
MIC29202BU	Adj	–40°C to +125°C	TO-263-5
MIC29203BT	Adj	–40°C to +125°C	TO-220-5
MIC29203BU	Adj	–40°C to +125°C	TO-263-5
MIC29204BJ	5 and Adj	–40°C to +125°C	8-pin CerDIP
MIC29204BM	5 and Adj	–40°C to +125°C	SO-8
MIC29204BN	5 and Adj	–40°C to +125°C	8-pin PDIP

* Junction temperatures

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact your local Micrel representative/distributor for availability and specifications.

Power Dissipation (Note 1)	Internally Limited
Lead Temperature (Soldering, 5 seconds)	260°C
Storage Temperature Range	–65°C to +150°C
Operating Junction Temperature Range	–40°C to +125°C
Input Supply Voltage	–20V to +60V
Operating Input Supply Voltage	2V† to 26V
Adjust Input Voltage (Notes 9 and 10)	–1.5V to +26V
Shutdown Input Voltage	–0.3V to +30V
Error Comparator Output Voltage	–0.3V to +30V
ESD Rating	>±2000V

† Across the full operating temperature, the minimum input voltage range for full output current is 4.3V to 26V. Output will remain in-regulation at lower output voltages and low current loads down to an input of 2V at 25°C.

Electrical Characteristics

Limits in standard typeface are for T_J = 25°C and limits in **boldface** apply over the full operating temperature range. Unless otherwise specified, $V_{IN} = V_{OUT} + 1V$, I_L = 1mA, C_L = 10µF. Adjustable version are set for an output of 5V. The MIC29203 $V_{SHUTDOWN} \leq 0.7V$. The eight pin MIC29204 is configured with the Adjust pin tied to the 5V Tap, the Output is tied to Output Sense (V_{OUT} = 5V), and $V_{SHUTDOWN} \leq 0.7V$.

Symbol	Parameter	Conditions	Min	Typical	Max	Units
V_O	Output Voltage Accuracy	Variation from factory trimmed V_{OUT}	–1 **–2**		1 **2**	%
		1mA ≤ I_L ≤ 400mA	**–2.5**		**2.5**	
$\frac{\Delta V_O}{\Delta T}$	Output Voltage Temperature Coef.	(Note 2)		**20**	**100**	ppm/°C
$\frac{\Delta V_O}{V_O}$	Line Regulation	$V_{IN} = V_{OUT}$ + 1V to 26V		0.03	0.10 **0.40**	%
$\frac{\Delta V_O}{V_O}$	Load Regulation	I_L = 1 to 250mA (Note 3)		0.04	0.16 **0.30**	%
$V_{IN} - V_O$	Dropout Voltage (Note 4)	I_L = 1mA I_L = 100mA I_L = 250mA I_L = 400mA		60 250 370 450	100 **150** 300 **420** 450 **600**	mV
I_{GND}	Ground Pin Current (Note 5)	I_L = 1mA I_L = 100mA I_L = 250mA I_L = 400mA		120 1 5.1 11	200 **300** 1.5 **2** 6 **8**	µA mA
I_{GNDDO}	Ground Pin Current at Dropout (Note 5)	V_{IN} = 0.5V less than designed V_{OUT} ($V_{OUT} \geq 3.3V$)		180	**300**	µA
I_{LIMIT}	Current Limit	V_{OUT} = 0V (Note 6)	 **500**	640	1000 **1200**	mA
$\frac{\Delta V_O}{\Delta P_D}$	Thermal Regulation	(Note 7)		0.05	0.2	%/W
e_n	Output Noise Voltage (10Hz to 100kHz) I_L = 100mA	C_L = 10µF C_L = 100µF		400 260		µV RMS

Electrical Characteristics (Continued)

MIC29202, MIC29203, MIC29204

Parameter	Conditions	Typ.	Min	Max	Units
Reference Voltage		1.235	1.210 **1.200**	1.260 **1.270**	V
Reference Voltage	(Note 8)		**1.185**	**1.285**	V
Adjust Pin Bias Current		20		40 **60**	nA
Reference Voltage Temperature Coefficient	(Note 7)	20			ppm/°C
Adjust Pin Bias Current Temperature Coefficient		0.1			nA/°C
Error Comparator	**MIC29201, MIC29203, MIC29204**				
Output Leakage Current	V_{OH} = 26V	0.01		1.00 **2.00**	µA
Output Low Voltage	V_{IN} = 4.5V I_{OL} = 250µA	150		250 **400**	mV
Upper Threshold Voltage	(Note 9)	60	40 **25**		mV
Lower Threshold Voltage	(Note 9)	75		95 **140**	mV
Hysteresis	(Note 9)	15			mV
Shutdown Input	**MIC29201, MIC29202, MIC29204**				
Input Logic Voltage	Low (ON) High (OFF)	1.3	 **2.0**	**0.7**	V
Shutdown Pin Input Current	$V_{SHUTDOWN}$ = 2.4V	30		50 **100**	µA
	$V_{SHUTDOWN}$ = 26V	450		600 **750**	µA
Regulator Output Current in Shutdown	(Note 10)	3		10 **20**	µA

Note 1: Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device outside of its rated operating conditions. The maximum allowable power dissipation is a function of the maximum junction temperature, $T_{J(MAX)}$, the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using: $P_{(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the regulator will go into thermal shutdown. The junction to ambient thermal resistance of the MIC29204BM is 160°C/W mounted on a PC board.

Note 2: Output voltage temperature coefficient is defined as the worst case voltage change divided by the total temperature range.

Note 3: Regulation is measured at constant junction temperature using low duty cycle pulse testing. Changes in output voltage due to heating effects are covered by the thermal regulation specification.

Note 4: Dropout Voltage is defined as the input to output differential at which the output voltage drops 100mV below its nominal value measured at 1V differential. At low values of programmed output voltage, the minimum input supply voltage of 4.3V over temperature must be taken into account. The MIC2920A operates down to 2V of input at reduced output current at 25°C.

Note 5: Ground pin current is the regulator quiescent current. The total current drawn from the supply is the sum of the load current plus the ground pin current.

Note 6: The MIC2920A features fold-back current limiting. The short circuit (V_{OUT} = 0V) current limit is less than the maximum current with normal output voltage.

Note 7: Thermal regulation is defined as the change in output voltage at a time T after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for a 200mA load pulse at V_{IN} = 20V (a 4W pulse) for T = 10ms.

Note 8: $V_{REF} \leq V_{OUT} \leq (V_{IN} - 1\ V)$, $4.3V \leq V_{IN} \leq 26V$, $1\ mA < I_L \leq 400\ mA$, $T_J \leq T_{J\ MAX}$.

Note 9: Comparator thresholds are expressed in terms of a voltage differential at the Adjust terminal below the nominal reference voltage measured at 6V input. To express these thresholds in terms of output voltage change, multiply by the error amplifier gain = V_{OUT} / V_{REF} = (R1 + R2)/R2. For example, at a programmed output voltage of 5V, the Error output is guaranteed to go low when the output drops by 95 mV x 5V/1.235 V = 384 mV. Thresholds remain constant as a percent of VOUT as VOUT is varied, with the dropout warning occurring at typically 5% below nominal, 7.5% guaranteed.

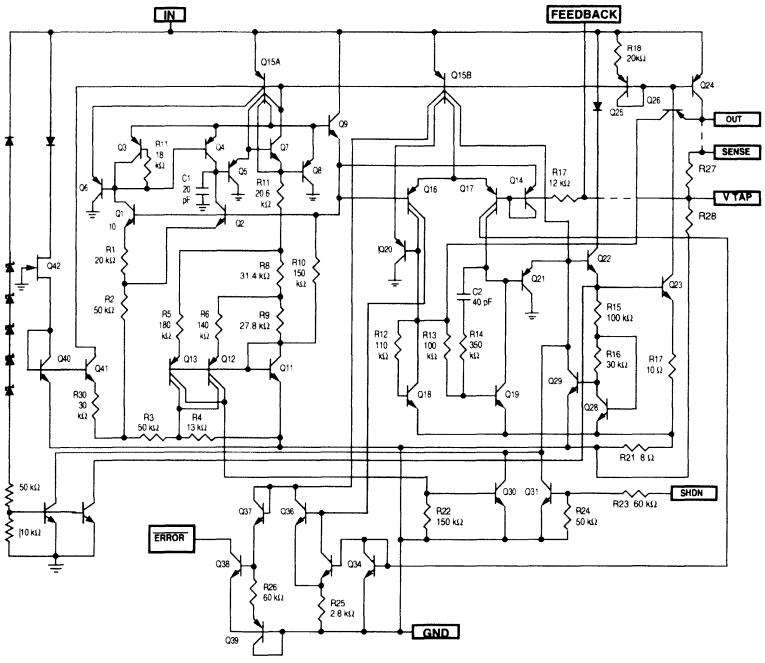
Note 10: $V_{SHUTDOWN} \geq 2V$, $V_{IN} \leq 26V$, $V_{OUT} = 0$, with Adjust pin tied to 5V Tap or to the R1, R2 junction (see Figure 3) with R1 ≥ 150kΩ.

Note 11: When used in dual supply systems where the regulator load is returned to a negative supply, the output voltage must be diode clamped to ground.

Note 12: Maximum positive supply voltage of 60V must be of limited duration (< 100ms) and duty cycle (≤ 1%). The maximum continuous supply voltage is 26V.

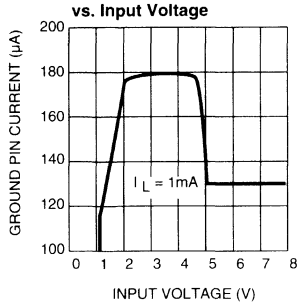
6

Schematic Diagram

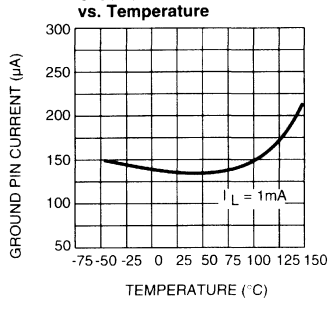


Typical Characteristics

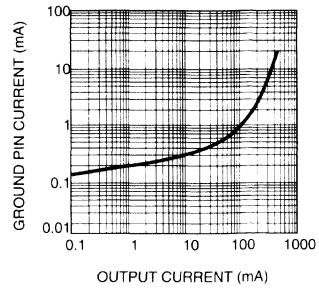
Ground Pin Current vs. Input Voltage



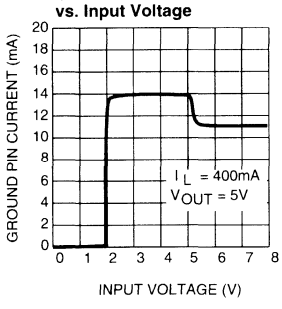
Ground Pin Current vs. Temperature



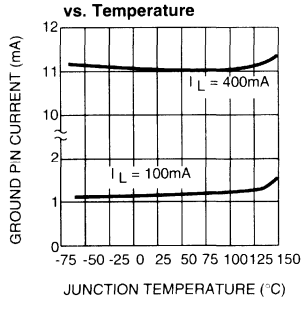
Ground Pin Current vs. Load



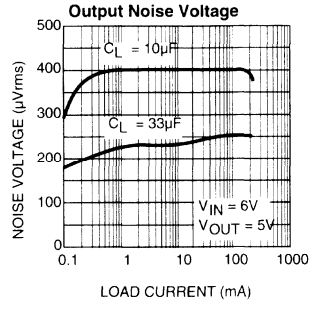
Ground Pin Current vs. Input Voltage



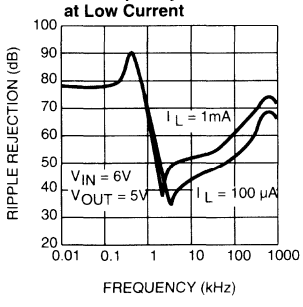
Ground Pin Current vs. Temperature



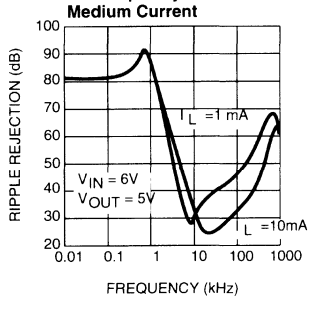
Output Noise Voltage



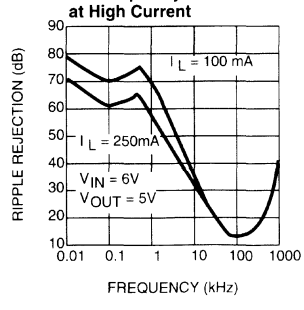
Ripple Rejection vs. Frequency at Low Current



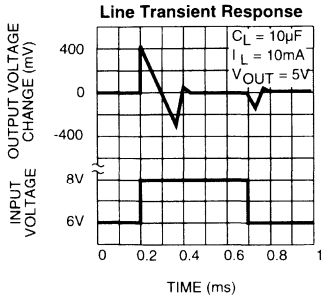
Ripple Rejection vs. Frequency at Medium Current



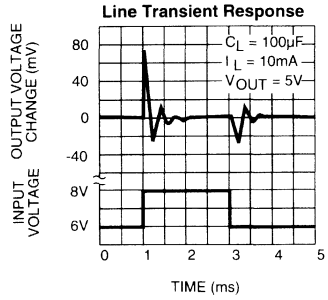
Ripple Rejection vs. Frequency at High Current



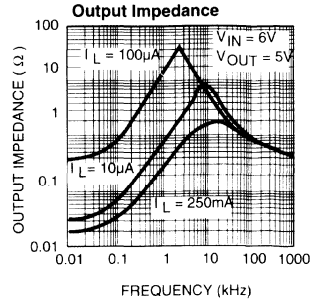
Line Transient Response



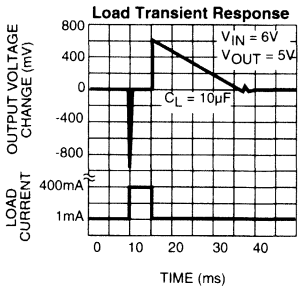
Line Transient Response

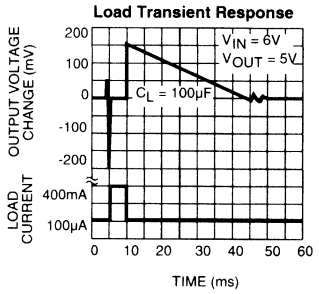


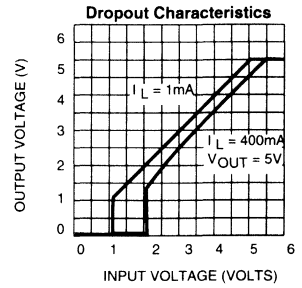
Output Impedance

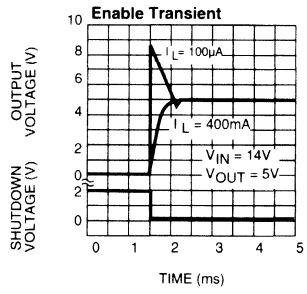


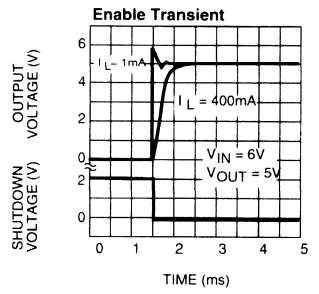
Typical Characteristics, Continued

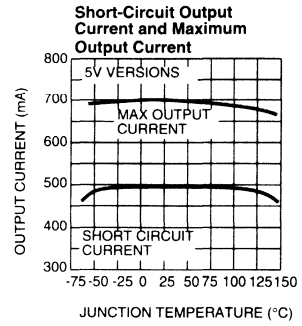


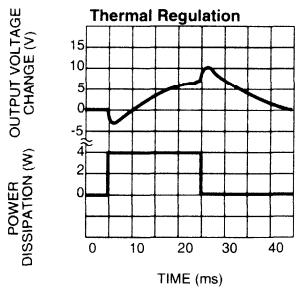


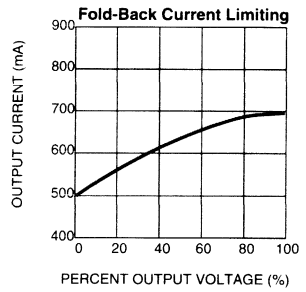


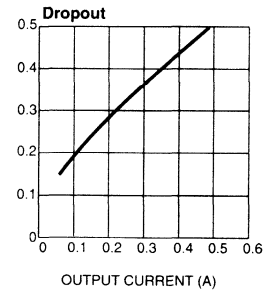












6

Applications Information

External Capacitors

A 10µF (or greater) capacitor is required between the MIC2920A output and ground to prevent oscillations due to instability. Most types of tantalum or aluminum electrolytics will be adequate; film types will work, but are costly and therefore not recommended. Many aluminum electrolytics have electrolytes that freeze at about –30°C, so solid tantalums are recommended for operation below –25°C. The important parameters of the capacitor are an effective series resistance of about 5Ω or less and a resonant frequency above 500kHz. The value of this capacitor may be increased without limit.

At lower values of output current, less output capacitance is required for output stability. The capacitor can be reduced to 2.2µF for current below 10mA or 1µF for currents below 1 mA. Adjusting the MIC29202/29203/29204 to voltages below 5V runs the error amplifier at lower gains so that more output capacitance is needed. For the worst-case situation of a 500mA load at 1.23V output (Output shorted to Adjust) a 47µF (or greater) capacitor should be used.

The MIC2920A will remain stable and in regulation with no D.C. load in addition to the internal voltage divider, unlike many other voltage regulators. This is especially important in CMOS RAM keep-alive applications. When setting the output voltage of the MIC29202/29203/29204 version with external resistors, a minimum load of 1µA is recommended.

A 1µF capacitor should be placed from the MIC2920A input to ground if there is more than 10 inches of wire between the input and the AC filter capacitor or if a battery is used as the input.

Stray capacitance to the MIC29202/29203/29204 Adjust terminal can cause instability. This may especially be a problem when using high value external resistors to set the output voltage. Adding a 100pF capacitor between Output and Adjust and increasing the output capacitor to at least 3.3µF will remedy this.

Error Detection Comparator Output (MIC29201/ MIC29203/MIC29204)

A logic low output will be produced by the comparator whenever the MIC29201/29203/29204 output falls out of regulation by more than approximately 5%. This figure is the comparator's built-in offset of about 60mV divided by the 1.235V reference voltage. (Refer to the block diagram on Page 1). This trip level remains "5% below normal" regardless of the programmed output voltage of the MIC29201/29203/29204. For example, the error flag trip level is typically 4.75V for a 5V output or 11.4V for a 12V output. The out of regulation condition may be due either to low input voltage, extremely high input voltage, current limiting, or thermal limiting.

Figure 1 is a timing diagram depicting the $\overline{\text{ERROR}}$ signal and the regulated output voltage as the MIC29201/29203/29204 input is ramped up and down. The $\overline{\text{ERROR}}$ signal becomes valid (low) at about 1.3V input. It goes high at about 5V input (the input voltage at which V_{OUT} = 4.75). Since the MIC29201/29203/29204's dropout voltage is load-dependent (see curve in Typical Performance Characteristics), the input voltage trip point (about 5V) will vary with the load current. The output voltage trip point (approximately 4.75V) does not vary with load.

The error comparator has an open-collector output which requires an external pull-up resistor. Depending on system requirements, this resistor may be returned to the 5V output or some other supply voltage. In determining a value for this resistor, note that while the output is rated to sink 250µA, this sink current adds to battery drain in a low battery condition. Suggested values range from 100k to 1MΩ. The resistor is not required if this output is unused.

In shutdown mode, $\overline{\text{ERROR}}$ will go high if it has been pulled up to an external supply. To avoid this invalid response, $\overline{\text{ERROR}}$ should be pulled up to V_{OUT}.

Programming the Output Voltage (MIC29202/ MIC29203/29204)

The MIC239202/29203/29204 may be programmed for any output voltage between its 1.235V reference and its 26V maximum rating, using an external pair of resistors, as shown in Figure 3.

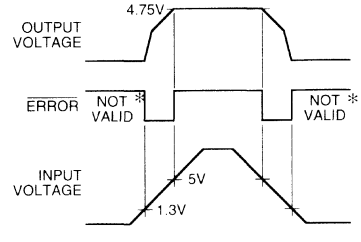
The complete equation for the output voltage is

$$V_{OUT} = V_{REF} \times \{ 1 + R_1/R_2 \} + I_{FB} R_1$$

where V_{REF} is the nominal 1.235 reference voltage and I_{FB} is the Adjust pin bias current, nominally 20nA. The minimum recommended load current of 1 µA forces an upper limit of 1.2MΩ on the value of R_2, if the regulator must work with no load (a condition often found in CMOS in standby), I_{FB} will produce a 2% typical error in V_{OUT} which may be eliminated at room temperature by trimming R_1. For better accuracy, choosing R_2 = 100k reduces this error to 0.17% while increasing the resistor program current to 12 µA. Since the MIC29202/29203/29204 typically draws 110µA at no load with SHUTDOWN open-circuited, this is a negligible addition. The MIC29204 may be pin-strapped for 5V using the internal voltage divider by tying Pin 1 (output) to Pin 2 (sense) and Pin 7 (Adjust) to Pin 6 (V Tap).

Reducing Output Noise

In reference applications it may be advantageous to reduce the AC noise present at the output. One method is to reduce the regulator bandwidth by increasing the size of the output



* SEE APPLICATIONS INFORMATION

Figure 1. $\overline{\text{ERROR}}$ Output Timing

capacitor. This is relatively inefficient, as increasing the capacitor from 1 µF to 220 µF only decreases the noise from 430µV to 160µV_{RMS} for a 100kHz bandwidth at 5V output. Noise can be reduced fourfold by a bypass capacitor across R_1, since it reduces the high frequency gain from 4 to unity. Pick

$$C_{BYPASS} \cong \frac{1}{2\pi R_1 \bullet 200\ Hz}$$

or about 0.01 µF. When doing this, the output capacitor must be increased to 10 µF to maintain stability. These changes reduce the output noise from 430 µV to 100 µV rms for a 100 kHz bandwidth at 5V output. With the bypass capacitor added, noise no longer scales with output voltage so that improvements are more dramatic at higher output voltages.

Automotive Applications

The MIC2920A is ideally suited for automotive applications for a variety of reasons. It will operate over a wide range of input voltages with very low dropout voltages (40mV at light loads), and very low quiescent currents (100µA typical). These features are necessary for use in battery powered systems, such as automobiles. It is a "bulletproof" device with the ability to survive both reverse battery (negative transients up to 20V below ground), and load dump (positive transients up to 60V) conditions. A wide operating temperature range with low temperature coefficients is yet another reason to use these versatile regulators in automotive designs.

Typical Applications

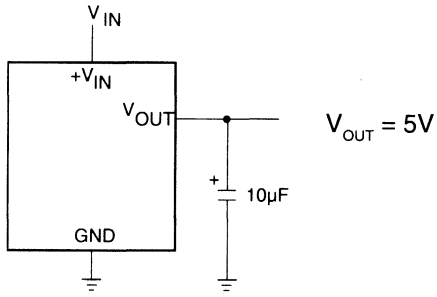
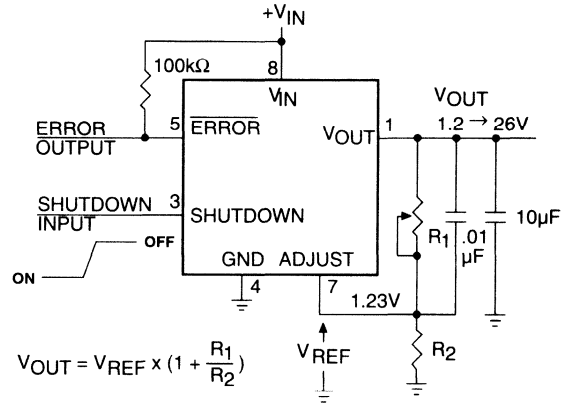
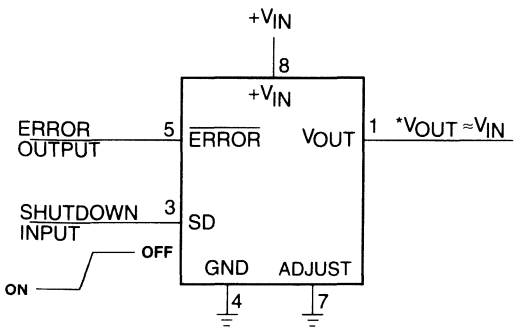


Figure 2. MIC2920A-5.0 Fixed +5V Regulator



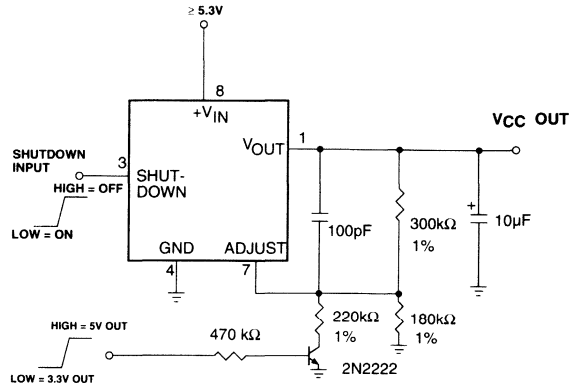
NOTE: PINS 2 AND 6 ARE LEFT OPEN

Figure 3. MIC29202/29203/29204 Adjustable Regulator. Pinout is for MIC29204.



*MINIMUM INPUT-OUTPUT VOLTAGE RANGES FROM 40mV TO 400mV, DEPENDING ON LOAD CURRENT.

Figure 4. MIC29204 Wide Input Voltage Range Current Limiter



PIN 3 LOW= ENABLE OUTPUT. Q1 ON = 3.3V, Q1 OFF = 5.0V.

Figure 5. MIC29202/29203/29204 5.0V or 3.3V Selectable Regulator with Shutdown. Pinout is for MIC29204.

MIC2937A,29371,29372,29373

750mA Low Drop Out Voltage Regulator

Preliminary Information–Production Q1 '94

General Description

The MIC2937A family are "bulletproof" efficient voltage regulators with very low dropout voltage (typically 40mV at light loads and 300mV at 500mA), and very low quiescent current (90μA typical). The quiescent current of the MIC2937A increases only slightly in dropout, thus prolonging battery life. Key MIC2937A features include protection against reversed battery, fold-back current limiting, and automotive "load dump" protection (60V positive transient).

The MIC2937 is available in several configurations. The MIC2937A-xx devices are three pin fixed voltage regulators. The MIC29371 is a fixed regulator offering logic compatible ON/OFF switching input and an error flag output. This flag may also be used as a power-on reset signal. A logic-compatible shutdown input is provided on the adjustable MIC29372, which enables the regulator to be switched on and off. The MIC29373 is a five pin adjustable version that includes an error flag output that warns of a low output voltage, which is often due to failing batteries on the input.

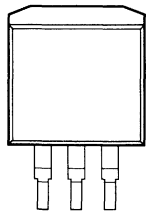
Features

- High output voltage accuracy
- Guaranteed 750mA output
- Low quiescent current
- Low dropout voltage
- Extremely tight load and line regulation
- Very low temperature coefficient
- Current and thermal limiting
- Input can withstand –20V reverse battery and +60V positive transients
- Error flag warns of output dropout
- Logic-controlled electronic shutdown
- Output programmable from 1.24V to 26V(MIC29372/ MIC29373)
- Available in TO-220, TO-263, TO-220-5, and TO-263-5 packages.

Applications

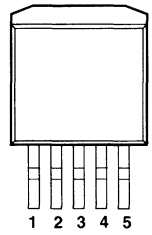
- Battery Powered Equipment
- Cellular Telephones
- Laptop, Notebook, and Palmtop Computers
- PCMCIA V_{CC} and V_{PP} Regulation/Switching
- Bar Code Scanners
- Automotive Electronics
- SMPS Post-Regulator/ DC to DC Modules
- High Efficiency Linear Power Supplies

Pin Configuration



INPUT GROUND OUTPUT

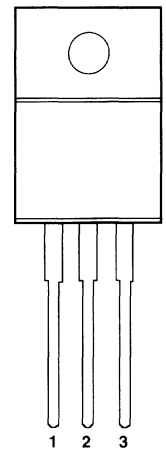
TO-263 Package (MIC2937A-xxBU)



TO-263-5 Package (MIC29371/29372/29373BU)

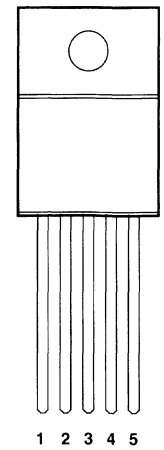
Five Lead Package Pin Functions:

	MIC29371	MIC29372	MIC29373
1)	Error	Adjust	Error
2)	Input	Shutdown	Adjust
3)	Ground	Ground	Ground
4)	Output	Input	Input
5)	Shutdown	Output	Output



INPUT GROUND OUTPUT

TO-220 Package (MIC2937A-xxBT)



TO-220-5 Package (MIC29371/29372/29373BT)

The TAB is Ground on the TO-220 and TO-263 packages.

Ordering Information

Part Number	Voltage	Temperature Range*	Package
MIC2937A-3.3BU	3.3	–40°C to +125°C	TO-263-3
MIC2937A-3.3BT	3.3	–40°C to +125°C	TO-220
MIC2937A-5.0BU	5.0	–40°C to +125°C	TO-263-3
MIC2937A-5.0BT	5.0	–40°C to +125°C	TO-220
MIC2937A-12BU	12	–40°C to +125°C	TO-263-3
MIC2937A-12BT	12	–40°C to +125°C	TO-220
MIC2937A-15BU	15	–40°C to +125°C	TO-263-3
MIC2937A-15BT	15	–40°C to +125°C	TO-220
MIC29371-3.3BT	3.3	–40°C to +125°C	TO-220-5
MIC29371-3.3BU	3.3	–40°C to +125°C	TO-263-5
MIC29371-5.0BT	5.0	–40°C to +125°C	TO-220-5
MIC29371-5.0BU	5.0	–40°C to +125°C	TO-263-5
MIC29371-12BT	12	–40°C to +125°C	TO-220-5
MIC29371-12BU	12	–40°C to +125°C	TO-263-5
MIC29371-15BT	15	–40°C to +125°C	TO-220-5
MIC29371-15BU	15	–40°C to +125°C	TO-263-5
MIC29372BT	Adj	–40°C to +125°C	TO-220-5
MIC29372BU	Adj	–40°C to +125°C	TO-263-5
MIC29373BT	Adj	–40°C to +125°C	TO-220-5
MIC29373BU	Adj	–40°C to +125°C	TO-263-5

* Junction temperatures

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact your local Micrel representative/distributor for availability and specifications.

Power Dissipation (Note 1)	Internally Limited
Lead Temperature (Soldering, 5 seconds)	260°C
Storage Temperature Range	–65°C to +150°C
Operating Junction Temperature Range	–40°C to +125°C
Input Supply Voltage	–20V to +60V
Operating Input Supply Voltage	2V† to 26V
Adjust Input Voltage (Notes 9 and 10)	–1.5V to +26V
Shutdown Input Voltage	–0.3V to +30V
Error Comparator Output Voltage	–0.3V to +30V
ESD Rating	>±2000V

† Across the full operating temperature, the minimum input voltage range for full output current is 4.3V to 26V. Output will remain in-regulation at lower output voltages and low current loads down to an input of 2V at 25°C.

6

Electrical Characteristics

Limits in standard typeface are for T_J = 25°C and limits in **boldface** apply over the full operating temperature range. Unless otherwise specified, $V_{IN} = V_{OUT} + 1V$, I_L = 5mA, C_L = 10µF. The MIC29372 and MIC29373 are programmed for a 5V output voltage, and $V_{SHUTDOWN} \leq 0.6V$ (MIC29372 only).

Symbol	Parameter	Conditions	Min	Typical	Max	Units
V_O	Output Voltage (5.0 or adjustable versions)		4.950	5.00	5.050	V
			4.900		**5.100**	
		5mA ≤ I_L ≤ 500mA	**4.880**	**5.00**	**5.120**	
	Output Voltage Accuracy	Variation from designed V_{OUT}	–1		1	%
			–2		**2**	
		5mA ≤ I_L ≤ 500mA	**–2.5**		**2.5**	
$\frac{\Delta V_O}{\Delta T}$	Output Voltage Temperature Coef.	(Note 2)		**20**	**100**	ppm/°C
$\frac{\Delta V_O}{V_O}$	Line Regulation	$V_{IN} = V_{OUT} + 1V$ to 26V		0.03	0.10	%
					0.40	
$\frac{\Delta V_O}{V_O}$	Load Regulation	I_L = 5 to 750mA		0.04	0.16	%
					0.20	
		(Note 3)				
$V_{IN} - V_O$	Dropout Voltage (Note 4)	I_L = 5mA		60	100	mV
					150	
		I_L = 100mA		150	200	
					320	
		I_L = 500mA		300	450	
					600	
		I_L = 750mA		370		
I_{GND}	Ground Pin Current (Note 5)	I_L = 5mA		90	150	µA
					180	
		I_L = 100mA		1	2	mA
					3	
		I_L = 500mA		8	13	
					16	
		I_L = 750mA		15		
I_{GNDDO}	Ground Pin Current at Dropout (Note 5)	V_{IN} = 0.5V less than designed V_{OUT} ($V_{OUT} \geq 3.3V$)		180	**300**	µA
I_{LIMIT}	Current Limit	V_{OUT} = 0V (Note 6)		1.0	1.5	A
					2	
$\frac{\Delta V_O}{\Delta P_D}$	Thermal Regulation	(Note 7)		0.05	0.2	%/W
e_n	Output Noise Voltage (10Hz to 100kHz) I_L = 100mA	C_L = 2.2µF		400		µV RMS
		C_L = 33µF		260		

Electrical Characteristics (Continued)

MIC29372/MIC29373

Parameter	Conditions	Min	Typical	Max	Units
Reference Voltage		1.210 **1.200**	1.235	1.260 **1.270**	V V max
Reference Voltage	(Note 8)	**1.185**		**1.285**	V
Adjust Pin Bias Current			20	40 **60**	nA
Reference Voltage Temperature Coefficient	(Note 7)		20		ppm/°C
Adjust Pin Bias Current Temperature Coefficient			0.1		nA/°C
Error Comparator	**MIC29371/29373**				
Output Leakage Current	V_{OH} = 30V		0.01	1.00 **2.00**	µA
Output Low Voltage	V_{IN} = 4.5V I_{OL} = 250µA		150	250 **400**	mV
Upper Threshold Voltage	(Note 9)	40 **25**	60		mV
Lower Threshold Voltage	(Note 9)		75	95 **140**	mV
Hysteresis	(Note 9)		15		mV
Shutdown Input	**MIC29371/MIC29372**				
Input Logic Voltage Low (ON)	 High (OFF)	 **2.0**	1.3	 **0.7**	V
Shutdown Pin Input Current	$V_{SHUTDOWN}$ = 2.4V		30	50 **100**	µA
	$V_{SHUTDOWN}$ = 30V		450	600 **750**	µA
Regulator Output Current in Shutdown	(Note 10)		3	10 **20**	µA

6

Note 1: Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device outside of its rated operating conditions. The maximum allowable power dissipation is a function of the maximum junction temperature, $T_{J(MAX)}$, the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using: $P_{(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the regulator will go into thermal shutdown.

Note 2: Output voltage temperature coefficient is defined as the worst case voltage change divided by the total temperature range.

Note 3: Regulation is measured at constant junction temperature using low duty cycle pulse testing. Changes in output voltage due to heating effects are covered by the thermal regulation specification.

Note 4: Dropout Voltage is defined as the input to output differential at which the output voltage drops 100 mV below its nominal value measured at 1V differential. At low values of programmed output voltage, the minimum input supply voltage of 4.3V over temperature must be taken into account. The MIC2937A operates down to 2V of input at reduced output current at 25°C.

Note 5: Ground pin current is the regulator quiescent current. The total current drawn from the source is the sum of the load current plus the ground pin current.

Note 6: The MIC2937A features fold-back current limiting. The short circuit (V_{OUT} = 0V) current limit is less than the maximum current with normal output voltage.

Note 7: Thermal regulation is defined as the change in output voltage at a time T after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for a 200mA load pulse at V_{IN} = 20V (a 4W pulse) for T = 10ms.

Note 8: $V_{REF} \le V_{OUT} \le (V_{IN} - 1\ V)$, $4.3V \le V_{IN} \le 26V$, $5mA < I_L \le 750\ mA$, $T_J \le T_{J\ MAX}$.

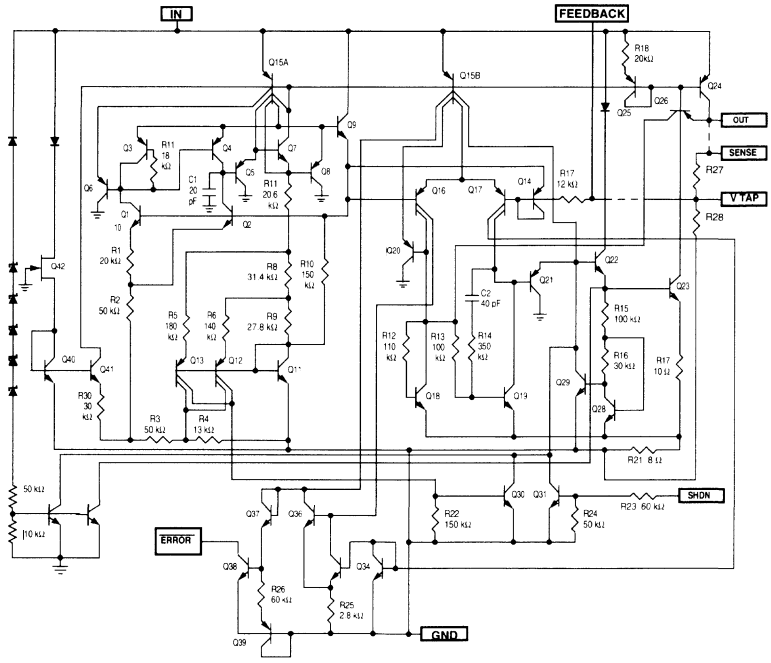
Note 9: Comparator thresholds are expressed in terms of a voltage differential at the Adjust terminal below the nominal reference voltage measured at 6V input (for a 5V regulator). To express these thresholds in terms of output voltage change, multiply by the error amplifier gain = V_{OUT} / V_{REF} = (R1 + R2)/R2. For example, at a programmed output voltage of 5V, the Error output is guaranteed to go low when the output drops by 95 mV x 5V/1.235 V = 384 mV. Thresholds remain constant as a percent of VOUT as VOUT is varied, with the dropout warning occurring at typically 5% below nominal, 7.5% guaranteed.

Note 10: Circuit of Figure 3 with R1 ≥ 150kΩ. $V_{SHUTDOWN} \ge 2V$ and $V_{IN} \le 26V$, $V_{OUT} = 0$.

Note 11: When used in dual supply systems where the regulator load is returned to a negative supply, the output voltage must be diode clamped to ground.

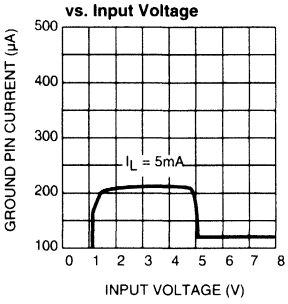
Note 12: Maximum positive supply voltage of 60V must be of limited duration (< 100ms) and duty cycle (≤ 1%). The maximum continuous supply voltage is 26V.

Schematic Diagram

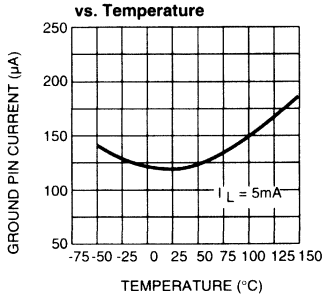


Typical Characteristics

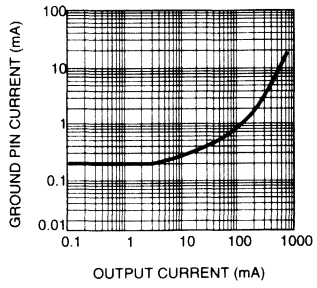
Ground Pin Current vs. Input Voltage



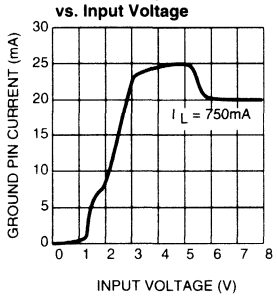
Ground Pin Current vs. Temperature



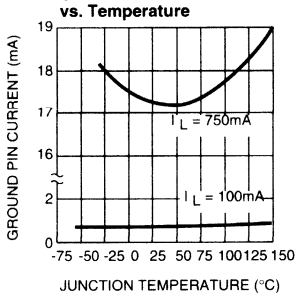
Ground Pin Current vs. Load



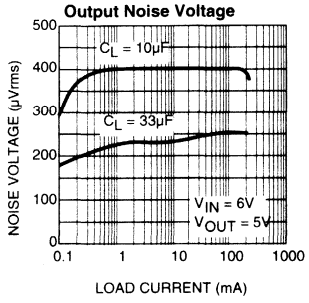
Ground Pin Current vs. Input Voltage



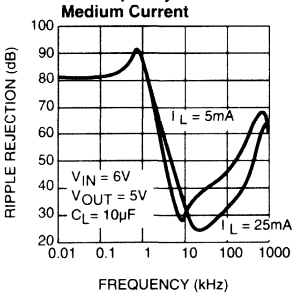
Ground Pin Current vs. Temperature



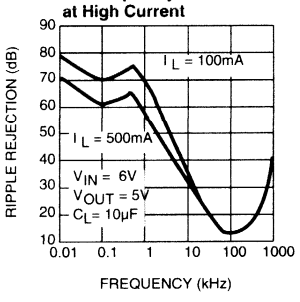
Output Noise Voltage



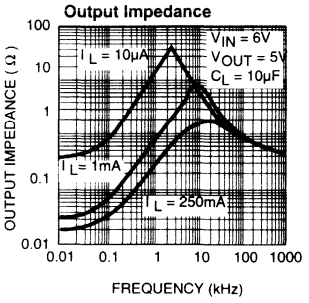
Ripple Rejection vs. Frequency at Medium Current



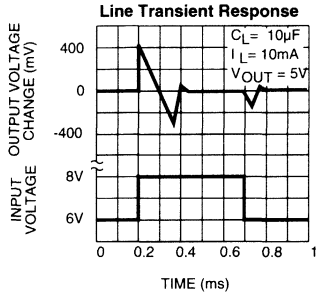
Ripple Rejection vs. Frequency at High Current



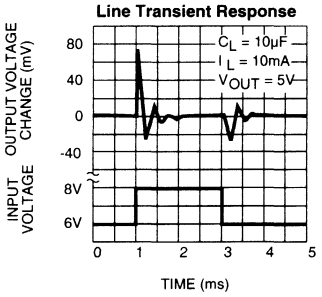
Output Impedance



Line Transient Response

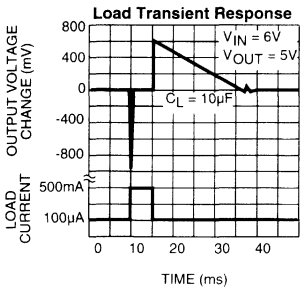


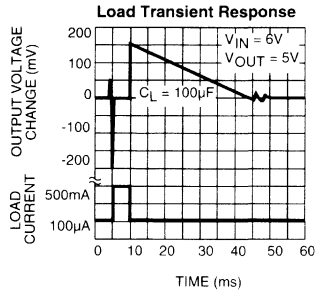
Line Transient Response

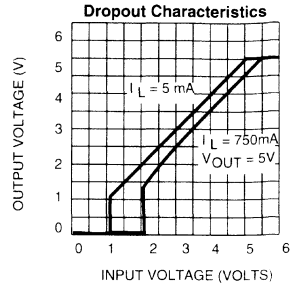


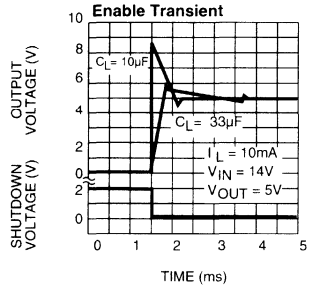
6

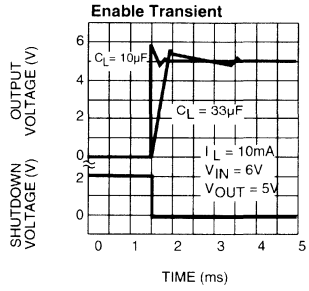
Typical Characteristics, Continued

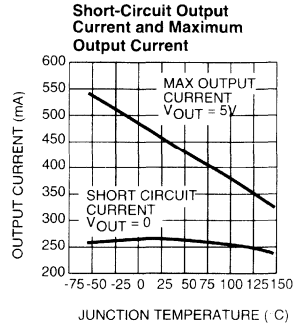


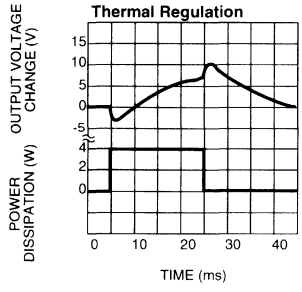


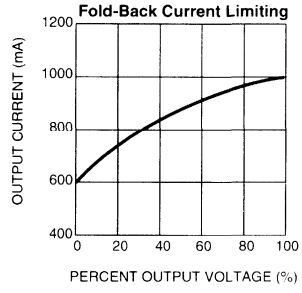


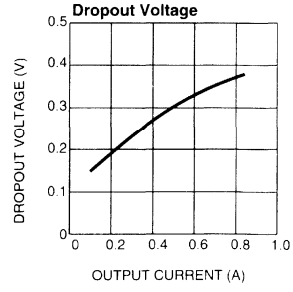












Applications Information

External Capacitors

A 10µF (or greater) capacitor is required between the MIC2937A output and ground to prevent oscillations due to instability. Most types of tantalum or aluminum electrolytics will be adequate; film types will work, but are costly and therefore not recommended. Many aluminum electrolytics have electrolytes that freeze at about –30°C, so solid tantalums are recommended for operation below –25°C. The important parameters of the capacitor are an effective series resistance of about 5Ω or less and a resonant frequency above 500kHz. The value of this capacitor may be increased without limit.

At lower values of output current, less output capacitance is required for output stability. The capacitor can be reduced to 0.5µF for current below 10mA or 0.15µF for currents below 1 mA. Adjusting the MIC29372/29373 to voltages below 5V runs the error amplifier at lower gains so that more output capacitance is needed. For the worst-case situation of a 750mA load at 1.23V output (Output shorted to Adjust) a 22µF (or greater) capacitor should be used.

The MIC2937A will remain stable and in regulation with no load in addition to the internal voltage divider, unlike many other voltage regulators. This is especially important in CMOS RAM keep-alive applications. When setting the output voltage of the MIC29372/29373 version with external resistors, a minimum load of 1mA is recommended.

A 1µF capacitor should be placed from the input to ground if there is more than 10 inches of wire between the input and the AC filter capacitor or if a battery is used as the input.

Stray capacitance to the MIC29372/29373 Adjust terminal (pin 7) can cause instability. This may especially be a problem when using high value external resistors to set the output voltage. Adding a 100pF capacitor between Output and Adjust and increasing the output capacitor to at least 22µF will remedy this.

Error Detection Comparator Output (MIC29371/ MIC29373)

A logic low output will be produced by the comparator whenever the MIC29371/29373 output falls out of regulation by more than approximately 5%. This figure is the comparator's built-in offset of about 60mV divided by the 1.235V reference voltage. (Refer to the block diagram on Page 1). This trip level remains "5% below normal" regardless of the programmed output voltage of the MIC29371/29373. For example, the error flag trip level is typically 4.75V for a 5V output or 11.4V for a 12V output. The out of regulation condition may be due either to low input voltage, extremely high input voltage, current limiting, or thermal limiting.

Figure 1 is a timing diagram depicting the $\overline{\text{ERROR}}$ signal and the regulated output voltage as the MIC29371/29373 input is ramped up and down. The $\overline{\text{ERROR}}$ signal becomes valid (low) at about 1.3V input. It goes high at about 5V input (the input voltage at which V_{OUT} = 4.75). Since the MIC29371/29373's dropout voltage is load-dependent (see curve in Typical Performance Characteristics), the input voltage trip point (about 5V) will vary with the load current. The output voltage trip point (approximately 4.75V) does not vary with load.

The error comparator has an open-collector output which requires an external pull-up resistor. Depending on system requirements, this resistor may be returned to the 5V output or some other supply voltage. In determining a value for this resistor, note that while the output is rated to sink 250µA, this sink current adds to battery drain in a low battery condition. Suggested values range from 100k to 1MΩ. The resistor is not required if this output is unused.

In shutdown mode, $\overline{\text{ERROR}}$ will go high if it has been pulled up to an external supply. To avoid this invalid response, $\overline{\text{ERROR}}$ should be pulled up to V_{OUT}.

Programming the Output Voltage (MIC29372/ MIC29373)

The MIC29372/29373 may programmed for any output voltage between its 1.235V reference and its 26V maximum rating. An external pair of resistors is required, as shown in Figure 3.

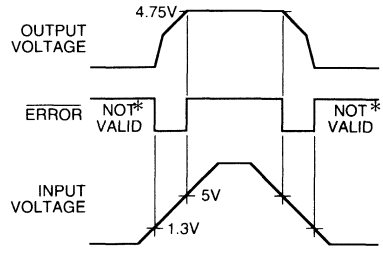
The complete equation for the output voltage is

$$V_{OUT} = V_{REF} \times \{ 1 + R_1/R_2 \} + I_{FB} R_1$$

where V_{REF} is the nominal 1.235 reference voltage and I_{FB} is the Adjust pin bias current, nominally 20nA. The minimum recommended load current of 1µA forces an upper limit of 1.2MΩ on the value of R_2, if the regulator must work with no load (a condition often found in CMOS in standby), I_{FB} will produce a 2% typical error in V_{OUT} which may be eliminated at room temperature by trimming R_1. For better accuracy, choosing R_2 = 100k reduces this error to 0.17% while increasing the resistor program current to 12µA. Since the MIC29372/29273 typically draws 100µA at no load with SHUTDOWN open-circuited, this is a negligible addition.

Reducing Output Noise

In reference applications it may be advantageous to reduce the AC noise present at the output. One method is to reduce the regulator bandwidth by increasing the size of the output capacitor. This is relatively inefficient, as increasing the capacitor from 1µF to 220µF only decreases the noise from 430µV to 160µV_{RMS} for a 100kHz bandwidth at 5V output. Noise can be reduced by a factor of four with the adjustable



* SEE APPLICATIONS INFORMATION

Figure 1. $\overline{\text{ERROR}}$ Output Timing

regulators with a bypass capacitor across R_1, since it reduces the high frequency gain from 4 to unity. Pick

$$C_{BYPASS} \cong \frac{1}{2\pi R_1 \bullet 200\ Hz}$$

or about 0.01µF. When doing this, the output capacitor must be increased to 10µF to maintain stability. These changes reduce the output noise from 430µV to 100μV_{RMS} for a 100 kHz bandwidth at 5V output. With the bypass capacitor added, noise no longer scales with output voltage so that improvements are more dramatic at higher output voltages.

Automotive Applications

The MIC2937A is ideally suited for automotive applications for a variety of reasons. It will operate over a wide range of input voltages with very low dropout voltages (40mV at light loads), and very low quiescent currents (100µA typical). These features are necessary for use in battery powered systems, such as automobiles. It is a "bulletproof" device with the ability to survive both reverse battery (negative transients up to 20V below ground), and load dump (positive transients up to 60V) conditions. A wide operating temperature range with low temperature coefficients is yet another reason to use these versatile regulators in automotive designs.

Typical Applications

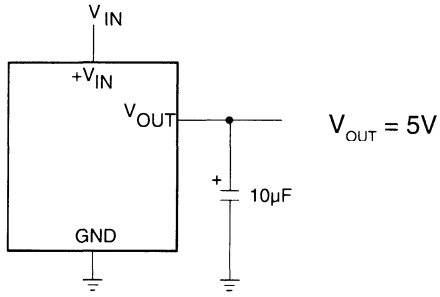


Figure 2. MIC2937A-5.0 Fixed +5V Regulator

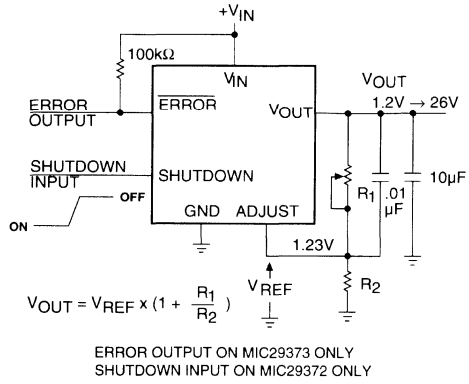
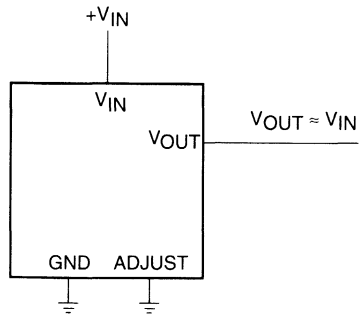
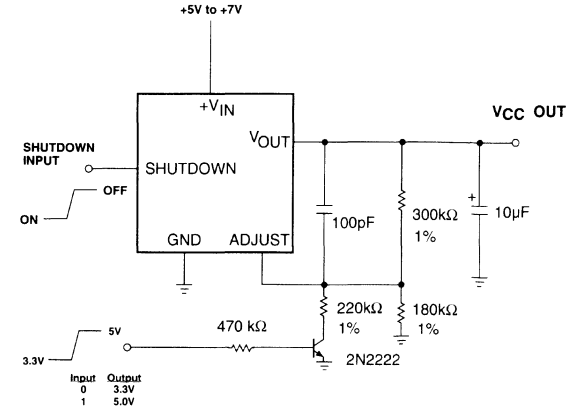


Figure 3. MIC29372/29373 Adjustable Regulator



*MINIMUM INPUT-OUTPUT VOLTAGE RANGES FROM 40mV TO 400mV, DEPENDING ON LOAD CURRENT.

Figure 4. MIC29372/29373 Wide Input Voltage Range Current Limiter



SHUTDOWN PIN LOW= ENABLE OUTPUT. Q1 ON = 3.3V, Q1 OFF = 5.0V.

Figure 5. MIC29372 5.0V or 3.3V Selectable Regulator with Shutdown.

MIC2940A and MIC2941A

1.25A Low Drop Out Voltage Regulator

Preliminary Information–Production Q1 '94

General Description

The MIC2940A and MIC2941A are "bulletproof" efficient voltage regulators with very low dropout voltage (typically 40mV at light loads and 280mV at 1A), and very low quiescent current (90μA typical). The quiescent current of the MIC2940A increases only slightly in dropout, thus prolonging battery life. Key MIC2940A features include protection against reversed battery, fold-back current limiting, and automotive "load dump" protection (60V positive transient).

The MIC2940 is available in both fixed voltage and adjustable voltage configurations. The MIC2940A-xx devices are three pin fixed voltage regulators. A logic-compatible shutdown input is provided on the adjustable MIC2941A, which enables the regulator to be switched on and off.

Features

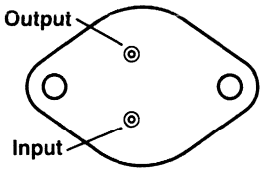
- High output voltage accuracy
- Guaranteed 1.2A output
- Low quiescent current
- Low dropout voltage
- Extremely tight load and line regulation
- Very low temperature coefficient
- Current and thermal limiting
- Input can withstand –20V reverse battery and +60V positive transients
- Logic-controlled electronic shutdown
- Output programmable from 1.24V to 26V(MIC2941A)
- Available in TO-220, TO-263, TO-220-5, TO-263-5, TO-3, and TO-3-4 packages.

Applications

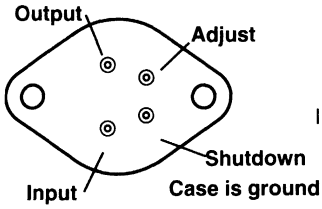
- Battery Powered Equipment
- Cellular Telephones
- Laptop, Notebook, and Palmtop Computers
- PCMCIA V_{CC} and V_{PP} Regulation/Switching
- Bar Code Scanners
- Automotive Electronics
- SMPS Post-Regulator/ DC to DC Modules
- Voltage Reference
- High Efficiency Linear Power Supplies

6

Pin Configuration



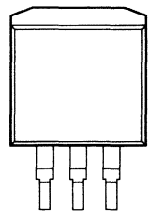
TO-3 Package
(MIC2940A-xxBK)



TO-3-5 Package
(MIC2941ABK)

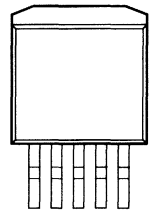
MIC2941A Pinout

1) **Adjust**
2) **Shutdown**
3) **Ground**
4) **Input**
5) **Output**

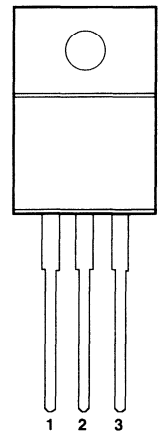


INPUT GROUND OUTPUT

TO-263 Package
(MIC2940A-xxBU)

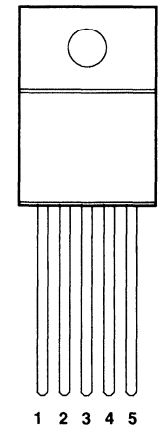


TO-263-5 Package
(MIC2941ABU)



INPUT GROUND OUTPUT

TO-220 Package
(MIC2940A-xxBT)



TO-220-5 Package
(MIC2941ABT)

Tab is Ground on TO-220 and TO-263 packages

Ordering Information

Part Number	Voltage	Temperature Range*	Package
MIC2940A-3.3BK	3.3	–40°C to +125°C	TO-3
MIC2940A-3.3BT	3.3	–40°C to +125°C	TO-220
MIC2940A-3.3BU	3.3	–40°C to +125°C	TO-263
MIC2940A-5.0BK	5.0	–40°C to +125°C	TO-3
MIC2940A-5.0BT	5.0	–40°C to +125°C	TO-220
MIC2940A-5.0BU	5.0	–40°C to +125°C	TO-263
MIC2940A-12BK	12	–40°C to +125°C	TO-3
MIC2940A-12BT	12	–40°C to +125°C	TO-220
MIC2940A-12BU	12	–40°C to +125°C	TO-263
MIC2941ABK	Adj	–40°C to +125°C	TO-3-4
MIC2941ABT	Adj	–40°C to +125°C	TO-220-5
MIC2941ABU	Adj	–40°C to +125°C	TO-263-5

* Junction temperatures

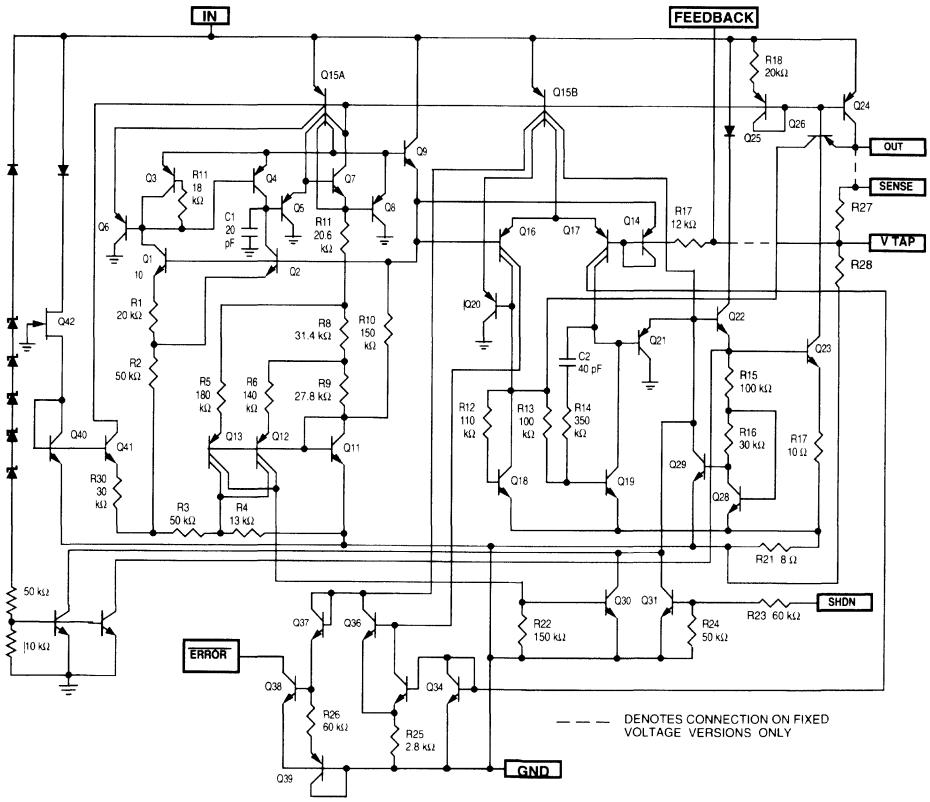
Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact your local Micrel representative/distributor for availability and specifications.

Power Dissipation (Note 1)	Internally Limited
Lead Temperature (Soldering, 5 seconds)	260°C
Storage Temperature Range	–65°C to +150°C
Operating Junction Temperature Range	–40°C to +125°C
Input Supply Voltage	–20V to +60V
Operating Input Supply Voltage	2V† to 26V
Adjust Input Voltage (Notes 9 and 10)	–1.5V to +26V
Shutdown Input Voltage	–0.3V to +30V
Error Comparator Output Voltage	–0.3V to +30V
ESD Rating	>±2000V

† Across the full operating temperature, the minimum input voltage range for full output current is 4.3V to 26V. Output will remain in-regulation at lower output voltages and low current loads down to an input of 2V at 25°C.

Schematic Diagram



Electrical Characteristics

Limits in standard typeface are for T_J = 25°C and limits in **boldface** apply over the full operating temperature range. Unless otherwise specified, $V_{IN} = V_{OUT} + 1V$, I_L = 1000mA, C_L = 10µF. The MIC2941A is programmed to output 5V and has $V_{SHUTDOWN} \leq 0.6V$.

Symbol	Parameter	Conditions	Min	Typical	Max	Units
V_O	Output Voltage (5.0 or adjustable versions)		4.950	5.00	5.050	V
			4.900		**5.100**	
		5 mA ≤ I_L ≤ 1A	**4.880**	**5.00**	**5.120**	
	Output Voltage Accuracy	Variation from designed V_{OUT}	–1		1	%
			–2		**2**	
		5 mA ≤ I_L ≤ 1A	**–2.5**		**2.5**	
$\frac{\Delta V_O}{\Delta T}$	Output Voltage Temperature Coef.	(Note 2)		**20**	**100**	ppm/°C
$\frac{\Delta V_O}{V_O}$	Line Regulation	$V_{IN} = V_{OUT} + 1V$ to 26V		0.03	0.10	%
					0.40	
$\frac{\Delta V_O}{V_O}$	Load Regulation	I_L = 5mA to 1A		0.04	0.16	%
					0.20	
		(Note 3)				
$V_{IN} - V_O$	Dropout Voltage (Note 4)	I_L = 5mA		60	100	mV
					150	
		I_L = 250mA		150	200	
					320	
		I_L = 1000mA		280	450	
					600	
		I_L = 1250mA		300		
I_{GND}	Ground Pin Current (Note 5)	I_L = 5mA		90	150	µA
					180	
		I_L = 250mA		3	4.5	mA
					6	
		I_L = 1000mA		22	35	
					45	
		I_L = 1250mA		35		
I_{GNDDO}	Ground Pin Current at Dropout (Note 5)	V_{IN} = 0.5V less than designed V_{OUT} ($V_{OUT} \geq 3.3V$)		180	**300**	µA
I_{LIMIT}	Current Limit	V_{OUT} = 0V (Note 6)		1.6	2	A
					2.4	
$\frac{\Delta V_O}{\Delta P_D}$	Thermal Regulation	(Note 7)		0.05	0.2	%/W
e_n	Output Noise Voltage (10Hz to 100kHz) I_L = 100mA	C_L = 10µF		400		µV RMS
		C_L = 33µF		260		

6

Electrical Characteristics (MIC2941A Only)

Parameter	Conditions	Min	Typical	Max	Units
Reference Voltage		1.210 **1.200**	1.235	1.260 **1.270**	V V max
Reference Voltage	(Note 9)	**1.185**		**1.285**	V
Adjust Pin Bias Current			20	40 **60**	nA
Reference Voltage Temperature Coefficient	(Note 8)		20		ppm/°C
Adjust Pin Bias Current Temperature Coefficient			0.1		nA/°C
Shutdown Input					
Input Logic Voltage	Low (ON) High (OFF)	 **2.0**	1.3	 **0.7**	V
Shutdown Pin Input Current	$V_{SHUTDOWN}$ = 2.4V		30	50 **100**	µA
	$V_{SHUTDOWN}$ = 30V		450	600 **750**	µA
Regulator Output Current in Shutdown	(Note 11)		3	10 **20**	µA

Note 1: Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device outside of its rated operating conditions. The maximum allowable power dissipation is a function of the maximum junction temperature, $T_{J(MAX)}$, the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using: $P_{(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the regulator will go into thermal shutdown.

Note 2: Output voltage temperature coefficient is defined as the worst case voltage change divided by the total temperature range.

Note 3: Regulation is measured at constant junction temperature using low duty cycle pulse testing. Changes in output voltage due to heating effects are covered by the thermal regulation specification.

Note 4: Dropout Voltage is defined as the input to output differential at which the output voltage drops 100 mV below its nominal value measured at 1V differential. At low values of programmed output voltage, the minimum input supply voltage of 4.3V over temperature must be taken into account.

Note 5: Ground pin current is the regulator quiescent current. The total current drawn from the source is the sum of the load current plus the ground pin current.

Note 6: The MIC2940A features fold-back current limiting. The short circuit (V_{OUT} = 0V) current limit is less than the maximum current with normal output voltage.

Note 7: Thermal regulation is defined as the change in output voltage at a time T after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for a 200mA load pulse at V_{IN} = 20V (a 4W pulse) for T = 10ms.

Note 8: $V_{REF} \leq V_{OUT} \leq (V_{IN} - 1\ V)$, $4.3V \leq V_{IN} \leq 26V$, $5mA < I_L \leq 1.25A$, $T_J \leq T_{J\ MAX}$.

Note 9: Comparator thresholds are expressed in terms of a voltage differential at the Adjust terminal below the nominal reference voltage measured at 6V input. To express these thresholds in terms of output voltage change, multiply by the error amplifier gain = V_{OUT} / V_{REF} = (R1 + R2)/R2. For example, at a programmed output voltage of 5V, the Error output is guaranteed to go low when the output drops by 95 mV x 5V/1.235 V = 384 mV. Thresholds remain constant as a percent of VOUT as VOUT is varied, with the dropout warning occurring at typically 5% below nominal, 7.5% guaranteed.

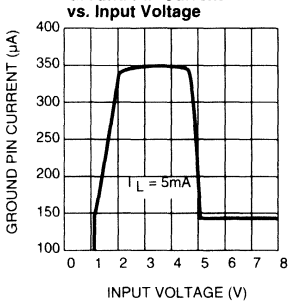
Note 10: Circuit of Figure 3 with R1 ≥ 150kΩ. $V_{SHUTDOWN} \geq 2$ V and $V_{IN} \leq 26$ V, $V_{OUT} = 0$.

Note 11: When used in dual supply systems where the regulator load is returned to a negative supply, the output voltage must be diode clamped to ground.

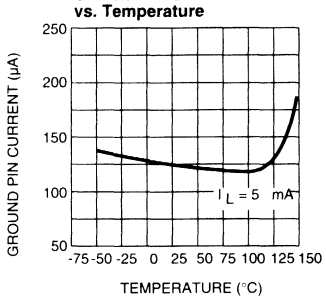
Note 12: Maximum positive supply voltage of 60 V must be of limited duration (< 100 ms) and duty cycle (≤ 1%). The maximum continuous supply voltage is 26V.

Typical Characteristics

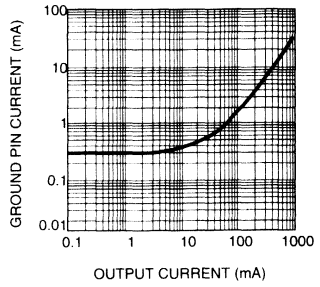
Ground Pin Current vs. Input Voltage



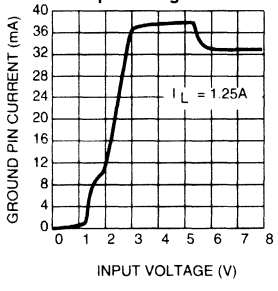
Ground Pin Current vs. Temperature



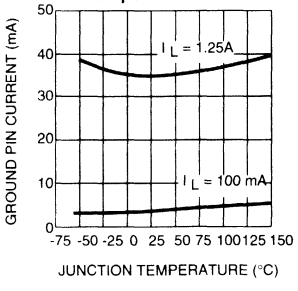
Ground Pin Current vs. Load



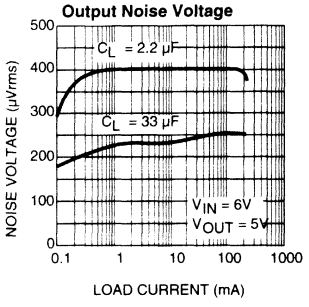
Ground Pin Current vs. Input Voltage



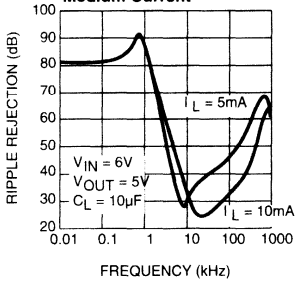
Ground Pin Current vs. Temperature



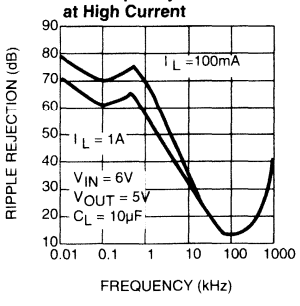
Output Noise Voltage



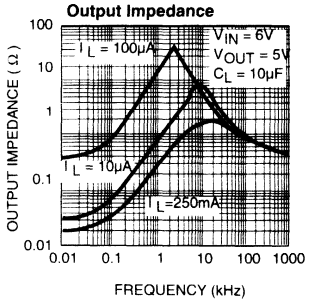
Ripple Rejection vs. Frequency at Medium Current



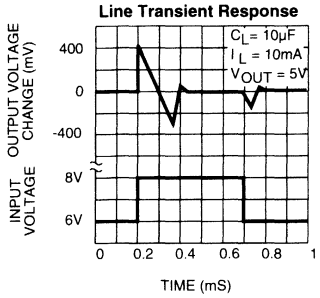
Ripple Rejection vs. Frequency at High Current



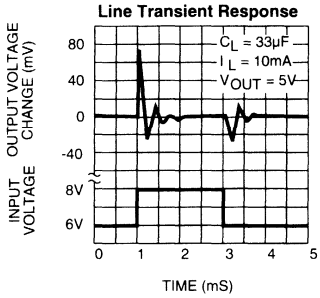
Output Impedance



Line Transient Response

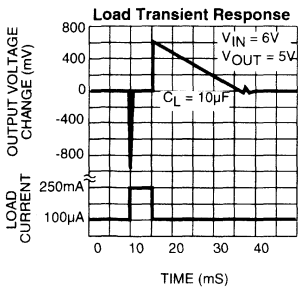


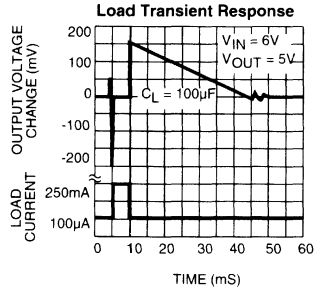
Line Transient Response

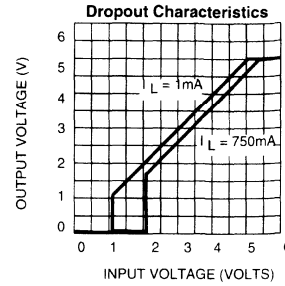


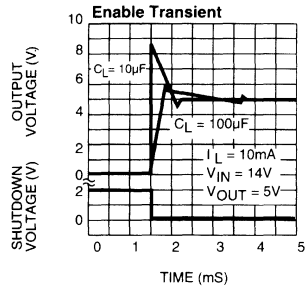
6

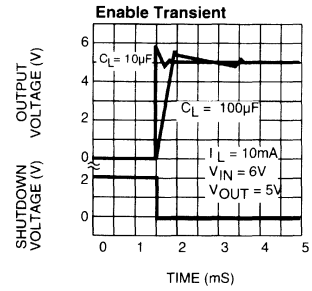
Typical Characteristics, Continued

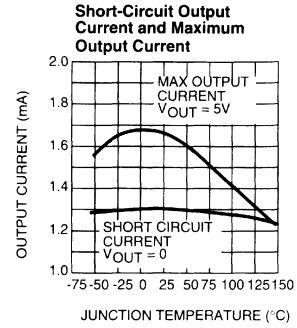


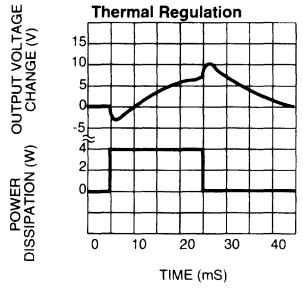


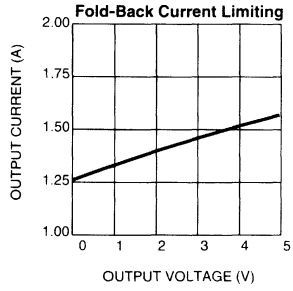


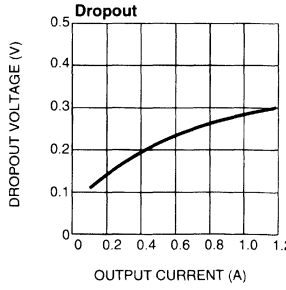












Applications Information

External Capacitors

A 10µF (or greater) capacitor is required between the MIC2940A output and ground to prevent oscillations due to instability. Most types of tantalum or aluminum electrolytics will be adequate; film types will work, but are costly and therefore not recommended. Many aluminum electrolytics have electrolytes that freeze at about –30°C, so solid tantalums are recommended for operation below –25°C. The important parameters of the capacitor are an effective series resistance of about 5Ω or less and a resonant frequency above 500kHz. The value of this capacitor may be increased without limit.

At lower values of output current, less output capacitance is required for output stability. The capacitor can be reduced to 3.3µF for current below 100mA or 2.2µF for currents below 10 mA. Adjusting the MIC2941A/29403 to voltages below 5V runs the error amplifier at lower gains so that more output capacitance is needed. For the worst-case situation of a 1.25A load at 1.23V output (Output shorted to Adjust) a 22µF (or greater) capacitor should be used.

The MIC2940A will remain stable and in regulation with no load in addition to the internal voltage divider, unlike many other voltage regulators. This is especially important in CMOS RAM keep-alive applications. When setting the output voltage of the MIC2941A version with external resistors, a minimum load of 1mA is recommended.

A 0.22µF capacitor should be placed from the MIC2940A input to ground if there is more than 10 inches of wire between the input and the AC filter capacitor or if a battery is used as the input.

Stray capacitance to the MIC2941A Adjust terminal can cause instability. This may especially be a problem when using high value external resistors to set the output voltage. Adding a 100pF capacitor between Output and Adjust and increasing the output capacitor to at least 22µF will remedy this.

Programming the Output Voltage (MIC2941A/ MIC29403)

The MIC2941A may be programmed for any output voltage between its 1.235V reference and its 26V maximum rating. An external pair of resistors is required, as shown in Figure 3.

The complete equation for the output voltage is

$$V_{OUT} = V_{REF} \times \{ 1 + R_1/R_2 \} + I_{FB} R_1$$

where V_{REF} is the nominal 1.235 reference voltage and I_{FB} is the Adjust pin bias current, nominally 20nA. The minimum recommended load current of 1 µA forces an upper limit of 1.2MΩ on the value of R_2, if the regulator must work with no load (a condition often found in CMOS in standby), I_{FB} will produce a 2% typical error in V_{OUT} which may be eliminated at room temperature by trimming R_1. For better accuracy, choosing R_2 = 100k reduces this error to 0.17% while increasing the resistor program current to 12 µA. Since the MIC2941A typically draws 100 µA at no load with SHUTDOWN open-circuited, this is a negligible addition.

Reducing Output Noise

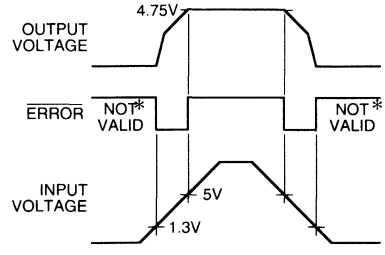
In reference applications it may be advantageous to reduce the AC noise present at the output. One method is to reduce the regulator bandwidth by increasing the size of the output capacitor. This is relatively inefficient, as increasing the capacitor from 1 µF to 220 µF only decreases the noise from 430µV to 160µV_{RMS} for a 100kHz bandwidth at 5V output. Noise can be reduced by a factor of four with the MIC2941A by adding a bypass capacitor across R_1, since it reduces the high frequency gain from 4 to unity. Pick

$$C_{BYPASS} \cong \frac{1}{2\pi R_1 \bullet 200\ Hz}$$

or about 0.01 µF. When doing this, the output capacitor must be increased to 22 µF to maintain stability. These changes reduce the output noise from 430 µV to 100 µV rms for a 100 kHz bandwidth at 5V output. With the bypass capacitor added, noise no longer scales with output voltage so that improvements are more dramatic at higher output voltages.

Automotive Applications

The MIC2940A is ideally suited for automotive applications for a variety of reasons. It will operate over a wide range of input voltages with very low dropout voltages (40mV at light loads), and very low quiescent currents (90µA typical). These features are necessary for use in battery powered systems, such as automobiles. It is a "bulletproof" device with the ability to survive both reverse battery (negative transients up to 20V below ground), and load dump (positive transients up to 60V) conditions. A wide operating temperature range with low temperature coefficients is yet another reason to use these versatile regulators in automotive designs.



* SEE APPLICATIONS INFORMATION

Figure 1. ERROR Output Timing

Typical Applications

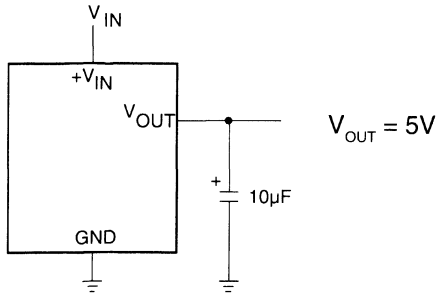


Figure 2. MIC2940A-5.0 Fixed +5V Regulator

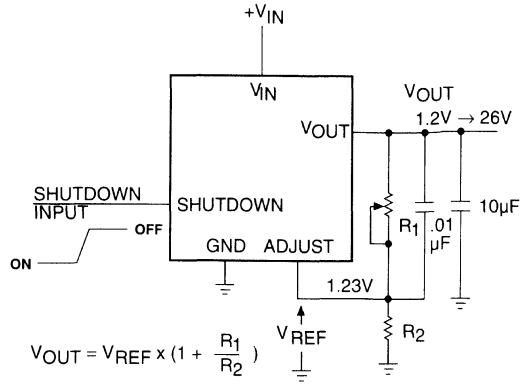
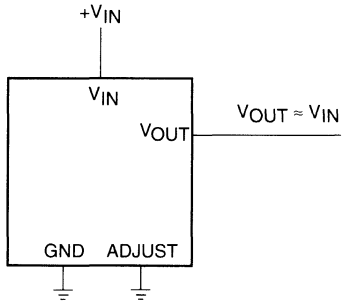
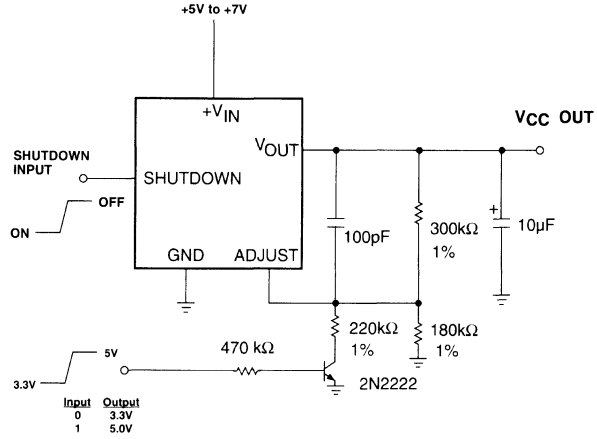


Figure 3. MIC2941A Adjustable Regulator



*MINIMUM INPUT-OUTPUT VOLTAGE RANGES FROM 40mV TO 400mV, DEPENDING ON LOAD CURRENT.

Figure 4. MIC2941A Wide Input Voltage Range Current Limiter



ADJUST PIN LOW= ENABLE OUTPUT. Q1 ON = 3.3V, Q1 OFF = 5.0V.

Figure 5. MIC2941A 5.0V or 3.3V Selectable Regulator with Shutdown.

MIC2950/MIC2951

150mA Low Drop Out Voltage Regulator

General Description

The MIC2950 and MIC2951 are "bulletproof" micropower voltage regulators with very low dropout voltage (typically 40mV at light loads and 250mV at 100mA), and very low quiescent current. Like their predecessors the LP2950 and LP2951, the quiescent current of the MIC2950/MIC2951 increases only slightly in dropout, thus prolonging battery life. The MIC2950/MIC2951 are pin for pin compatible with the LP2950/LP2951, but offer lower drop-out, lower quiescent current, reverse battery, and automotive load dump protection.

The key additional features and protection offered include higher output current (150mA), positive transient protection for up to 60V (load dump), and the ability to survive an unregulated input voltage transient of –20V below ground (reverse battery).

Available in a 3-Pin TO-92 package, the MIC2950 is pin-compatible with the older 5V regulators. Plastic or ceramic DIP packages and additional system functions such as programmable output voltage and logic controlled shutdown are available with the 8-lead MIC2951.

Features

- High accuracy 5V, guaranteed 150mA output
- Extremely low quiescent current
- Low dropout voltage
- Extremely tight load and line regulation
- Very low temperature coefficient
- Use as regulator or reference
- Needs only 1.5µF for stability
- Current and thermal limiting
- Unregulated DC input can withstand –20V reverse battery and +60V positive transients

MIC2951 Versions Only

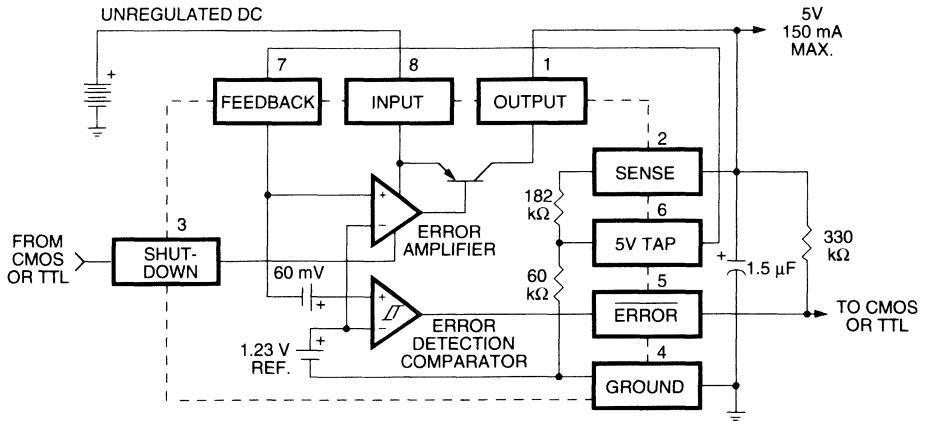
- Error flag warns of output dropout
- Logic-controlled electronic shutdown
- Output programmable from 1.24V to 29V

Applications

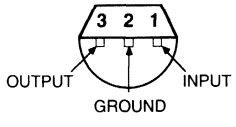
- Automotive Electronics
- Battery Powered Equipment
- Cellular Telephones
- SMPS Post-Regulator
- Voltage Reference
- Avionics
- High Efficiency Linear Power Supplies

6

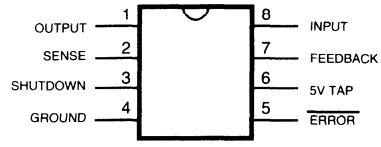
Block Diagram and Pin Configuration



MIC2950 and MIC2951 Block Diagram (Pin Numbers Refer to MIC2951)



TO-92 Plastic Package Bottom View (BZ)



DIP and SO Packages (AJ, BN, and BM)

Refer to the MIC2954 for a 250mA device in the same packages and pinouts.

These system functions also include an error flag output that warns of a low output voltage, which is often due to failing batteries on the input. This may also be used as a power-on reset. A logic-compatible shutdown input is also available which enables the regulator to be switched on and off. This part may also be pin-strapped for a 5 V output, or programmed from 1.24 V to 29 V with the use of two external resistors.

The MIC2950 is available as either an -05 or -06 version. The -05 and -06 versions are guaranteed for junction temperatures from –40°C to +125°C; the -05 version has a tighter output and reference voltage specification range over temperature. The MIC2951 is available as an -01, -02 , or -03 version. The -01 version is guaranteed for junction temperatures from –55°C to +150°C, and has slightly different specifications limits over the full operating temperature range.

The MIC2950 and MIC2951 have a tight initial tolerance (0.5% typical), a very low output voltage temperature coefficient which allows use as a low-power voltage reference, and extremely good load and line regulation (0.04% typical). This greatly reduces the error in the overall circuit, and is the result of careful design techniques and process control.

Ordering Information

Part Number	Temperature Range*	Package	Accuracy
MIC2950-05BZ	–40°C to +125°C	3-Pin TO-92 plastic	0.5%
MIC2950-06BZ	–40°C to +125°C	3-Pin TO-92 plastic	1.0%
MIC2951-02BM	–40°C to +125°C	8-Pin SO-8	0.5%
MIC2951-03BM	–40°C to +125°C	8-Pin SO-8	1.0%
MIC2951-01AJ	–55°C to +150°C	8-Pin CERDIP	0.5%
MIC2951-01AJB	–55°C to +150°C	8-Pin CERDIP†	0.5%
MIC2951-02BJ	–40°C to +125°C	8-Pin CERDIP	0.5%
MIC2951-03BJ	–40°C to +125°C	8-Pin CERDIP	1.0%
MIC2951-02BN	–40°C to +125°C	8-Pin Plastic DIP	0.5%
MIC2951-03BN	–40°C to +125°C	8-Pin Plastic DIP	1.0%

* Junction temperatures

† AJB Screened according to MIL-STD 5004, including burn-in

An 8-Pin Metal Header package is available. Contact Micrel for details.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact your local Micrel representative/distributor for availability and specifications.

Power Dissipation (Note 8)	Internally Limited
Lead Temperature (Soldering, 5 seconds)	260°C
Storage Temperature Range	–65°C to +150°C
Operating Junction Temperature Range (Note 8)	
MIC2951-01	–55°C to +150°C
MIC2950-05/MIC2950-06, MIC2951-02/MIC2951-03	–40°C to +125°C
Input Supply Voltage (Note 9)	–20V to +60V
Feedback Input Voltage (Notes 10 and 11)	–1.5V to +26V
Shutdown Input Voltage (Note 10)	–0.3V to +30V
Error Comparator Output Voltage (Note 10)	–0.3V to +30V
ESD Rating	To be determined.

Electrical Characteristics (Note 1)

Parameter	Conditions (Note 2)	MIC2951-01		MIC2950-05 MIC2951-02			MIC2950-06 MIC2951-03			Units
		Typ.	Tested Limit (Note 3)	Typ.	Tested Limit (Note 3)	Design Limit (Note 4)	Typ.	Tested Limit (Note 3)	Design Limit (Note 4)	
Output Voltage	$T_J = 25°C$	5.000	5.025 4.975	5.000	5.025 4.975		5.000	5.050 4.950		V max V min
	$-25°C \le T_J \le 85°C$					5.050 4.950			5.075 4.925	V max V min
	Full Operating Temperature Range		**5.060** **4.940**			**5.060** **4.940**			**5.100** **4.900**	V max V min
Output Voltage	$100\mu A \le I_L \le 150mA$ $T_J \le T_{J_{MAX}}$		**5.075** **4.925**			**5.070** **4.930**			**5.120** **4.880**	V max V min
Output Voltage Temperature Coefficient	(Note 13)	**20**	**120**	**20**		**100**	**50**		**150**	ppm/°C
Line Regulation	$6V \le V_{IN} \le 26V$ (Note 15, Note 16)	0.03	0.10 **0.50**	0.03	0.10	**0.20**	0.04	0.20	**0.40**	% max % max
Load Regulation	$100\mu A \le I_L \le 150mA$ (Note 15)	0.04	0.10 **0.30**	0.04	0.10	**0.20**	0.10	0.20	**0.30**	% max % max
Dropout Voltage (Note 5)	$I_L = 100\mu A$	40	80 **140**	40	80	**140**	40	80	**140**	mV max mV max
	$I_L = 100mA$	250	300	250	300		250	300		mV max
	$I_L = 150mA$	300	450 **600**	300	450	**600**	300	450	**600**	mV max mV max
Ground Current	$I_L = 100\mu A$	120	180 **300**	120	180	**300**	120	180	**300**	µA max µA max
	$I_L = 100mA$	1.7	2.5 **3.5**	1.7	2.5	**3.5**	1.7	2.5	**3.5**	mA max mA max
	$I_L = 150mA$	4	6 **8**	4	6	**8**	4	6	**8**	mA max mA max
Dropout Ground Current	$V_{IN} = 4.5V$ $I_L = 100\mu A$	180	**400**	180		**400**	180		**310**	µA max µA max
Current Limit	$V_{OUT} = 0$	240	300 **350**	240	300	**350**	240	300	**350**	mA max mA max
Thermal Regulation	(Note 14)	0.05	0.20	0.05	0.20		0.05	0.20		%/W max
Output Noise, 10Hz to 100kHz	$C_L = 1.5\mu F$	430		430			430			µV rms
	$C_L = 200\mu F$	160		160			160			µV rms
	$C_L = 3.3\mu F$ (Bypass = 0.01µF Pins 7–1 (MIC2951))	100		100			100			µV rms

6

Electrical Characteristics (Note 1) (Continued)

Parameter	Conditions (Note 2)	MIC2951-01 Typ.	MIC2951-01 Tested Limit (Note 3)	MIC2951-02 Typ.	MIC2951-02 Tested Limit (Note 3)	MIC2951-02 Design Limit (Note 4)	MIC2951-03 Typ.	MIC2951-03 Tested Limit (Note 3)	MIC2951-03 Design Limit (Note 4)	Units
8 Pin Version Only										
Reference Voltage		1.235	1.250 **1.260** 1.220 **1.200**	1.235	1.250 1.220 	 **1.260** **1.200**	1.235	1.260 1.210 	 **1.270** **1.200**	V max V max V min V min
Reference Voltage	(Note 7)		**1.270** **1.190**			**1.270** **1.190**			**1.285** **1.185**	V max V min
Feedback Pin Bias Current		20	40 **60**	20	40	 **60**	20	40	 **60**	nA max nA max
Reference Voltage Temperature Coefficient	(Note 13)	20		20			50			ppm/°C
Feedback Pin Bias Current Temperature Coefficient		0.1		0.1			0.1			nA/°C
Error Comparator										
Output Leakage Current	V_{OH} = 30V	0.01	1.00 **2.00**	0.01	1.00	 **2.00**	0.01	1.00	 **2.00**	µA max µA max
Output Low Voltage	V_{IN} = 4.5V I_{OL} = 400µA	150	250 **400**	150	250	 **400**	150	250	 **400**	mV max mV max
Upper Threshold Voltage	(Note 6)	60	40 **25**	60	40	 **25**	60	40	 **25**	mV min mV min
Lower Threshold Voltage	(Note 6)	75	95 **140**	75	95	 **140**	75	95	 **140**	mV max mV max
Hysteresis	(Note 6)	15		15			15			mV
Shutdown Input										
Input Logic Voltage	 Low (ON) High (OFF)	1.3	 **0.6** **2.0**	1.3		 **0.7** **2.0**	1.3		 **0.7** **2.0**	V V max V min
Shutdown Pin Input Current	$V_{SHUTDOWN}$ = 2.4V	30	50 **100**	30	50	 **100**	30	50	 **100**	µA max µA max
	$V_{SHUTDOWN}$ = 30V	450	600 **750**	450	600	 **750**	450	600	 **750**	µA max µA max
Regulator Output Current in Shutdown	(Note 12)	3	10 **20**	3	10	 **20**	3	10	 **20**	µA max µA max

Note 1: Boldface limits apply at temperature extremes.

Note 2: Unless otherwise specified all limits guaranteed for $T_J = 25°C$, $V_{IN} = 6V$, $I_L = 100\mu A$ and $C_L = 1\mu F$. Additional conditions for the 8-pin versions are Feedback tied to 5V Tap and Output tied to Output Sense ($V_{OUT} = 5V$) and $V_{SHUTDOWN} \leq 0.8V$.

Note 3: Guaranteed and 100% production tested.

Note 4: Guaranteed but not 100% production tested. These limits are not used to calculate outgoing AQL levels.

Note 5: Dropout Voltage is defined as the input to output differential at which the output voltage drops 100mV below its nominal value measured at 1V differential. At very low values of programmed output voltage, the minimum input supply voltage of 2V (2.3V over temperature) must be taken into account.

Note 6: Comparator thresholds are expressed in terms of a voltage differential at the Feedback terminal below the nominal reference voltage measured at 6V input. To express these thresholds in terms of output voltage change, multiply by the error amplifier gain = $V_{OUT}/V_{REF} = (R1 + R2)/R2$. For example, at a programmed output voltage of 5V, the Error output is guaranteed to go low when the output drops by 95 mV x 5V/1.235 V = 384 mV. Thresholds remain constant as a percent of VOUT as VOUT is varied, with the dropout warning occurring at typically 5% below nominal, 7.5% guaranteed.

Note 7: $V_{REF} \leq V_{OUT} \leq (V_{IN} - 1\ V)$, $2.3V \leq V_{IN} \leq 30V$, $100\mu A < I_L \leq 150mA$, $T_J \leq T_{J\ MAX}$.

Note 8: The junction-to-ambient thermal resistance of the TO-92 package is 180°C/W with 0.4" leads and 160°C/W with 0.25" leads to a PC board. The thermal resistances of the 8-Pin DIP packages are 105°C/W for the molded plastic (N) and 130°C/W for the CERDIP (J) junction to ambient when soldered directly to a PC board. Junction to ambient thermal resistance for the S.O. (M) package is 160°C/W.

Note 9: Maximum positive supply voltage of 60V must be of limited duration (< 100ms) and duty cycle (1%). The maximum continuous supply voltage is 30 V.

Note 10: May exceed input supply voltage.

Note 11: When used in dual-supply systems where the output terminal sees loads returned to a negative supply, the output voltage should be diode-clamped to ground.

Note 12: $V_{SHUTDOWN} \geq 2\ V$, $V_{IN} \leq 30\ V$, $V_{OUT} = 0$, with Feedback pin tied to 5V Tap.

Note 13: Output or reference voltage temperature coefficient is defined as the worst case voltage change divided by the total temperature range.

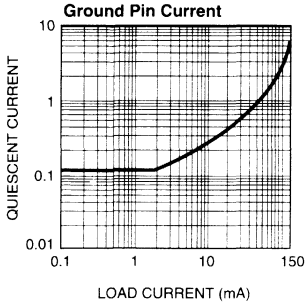
Note 14: Thermal regulation is defined as the change in output voltage at a time T after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for a 50mA load pulse at $V_{IN} = 30\ V$ (1.25W pulse) for T = 10ms.

Note 15: Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered in the specification for thermal regulation.

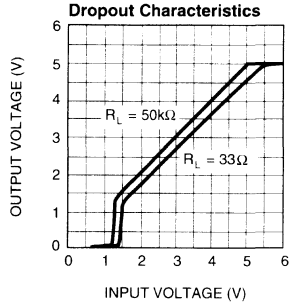
Note 16: Line regulation for the MIC2951 is tested at 150°C for $I_L = 1mA$. For $I_L = 100\mu A$ and $T_J = 125°C$, line regulation is guaranteed by design to 0.2%. See Typical Performance Characteristics for line regulation versus temperature and load current.

Typical Performance Characteristics

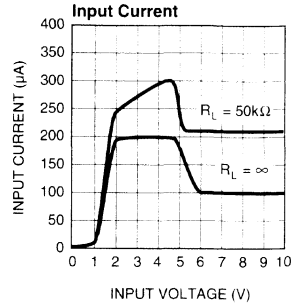
Ground Pin Current



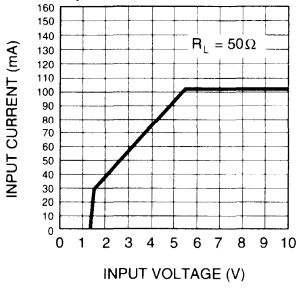
Dropout Characteristics



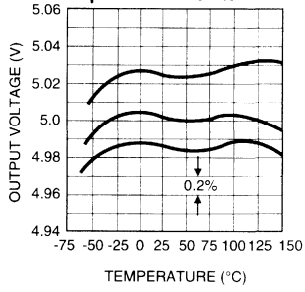
Input Current



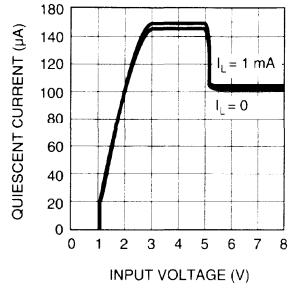
Input Current



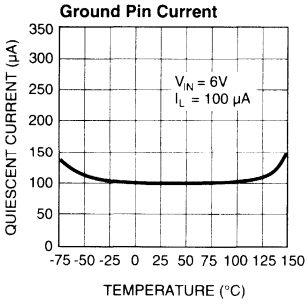
Output Voltage vs. Temperature of 3 Representative Units



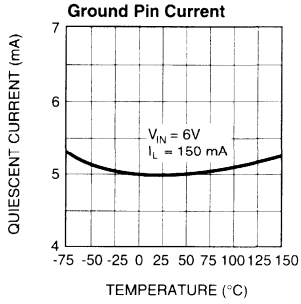
Ground Pin Current



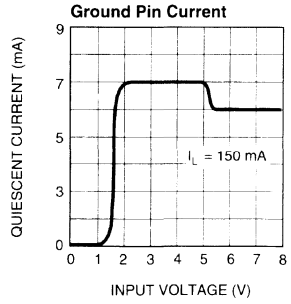
Ground Pin Current



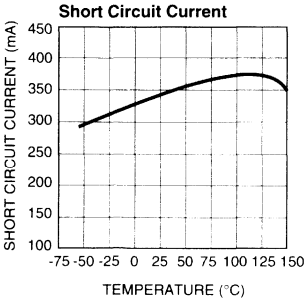
Ground Pin Current



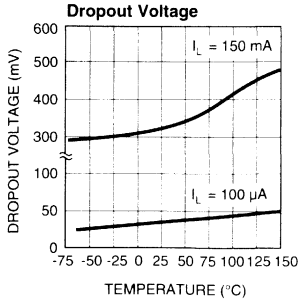
Ground Pin Current



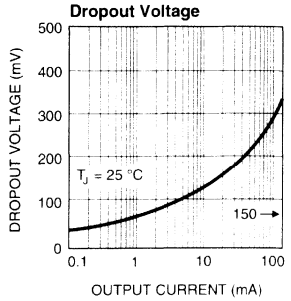
Short Circuit Current



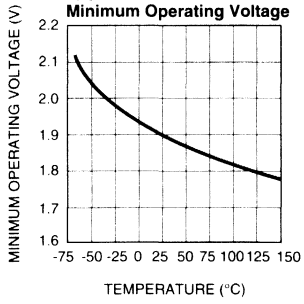
Dropout Voltage



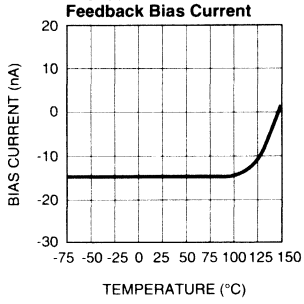
Dropout Voltage



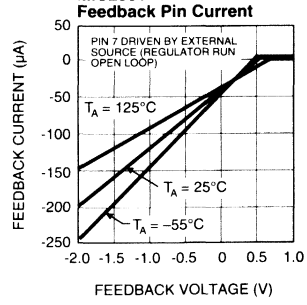
MIC2951 Minimum Operating Voltage



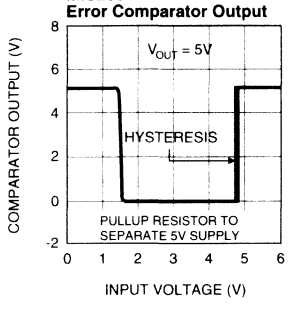
MIC2951 Feedback Bias Current



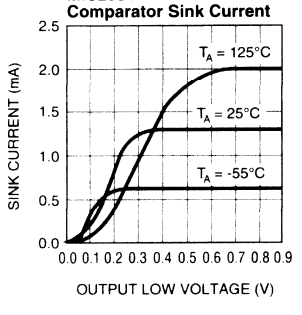
MIC2951 Feedback Pin Current



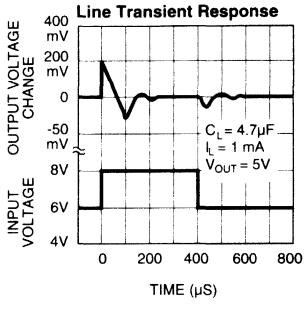
MIC2951 Error Comparator Output



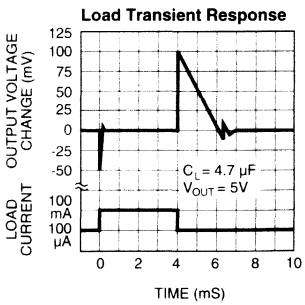
MIC2951 Comparator Sink Current



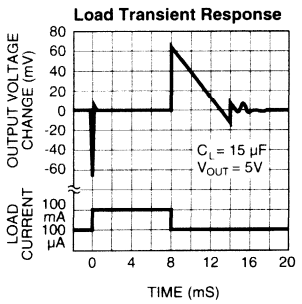
Line Transient Response



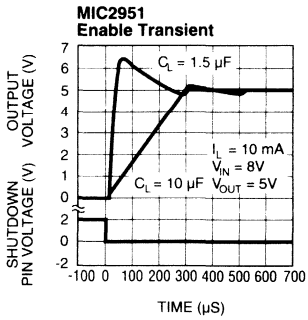
Load Transient Response



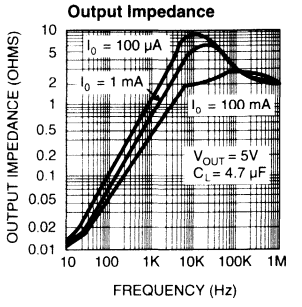
Load Transient Response



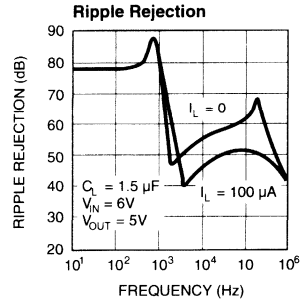
MIC2951 Enable Transient



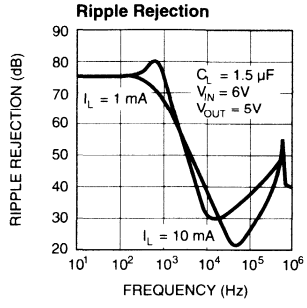
Output Impedance



Ripple Rejection

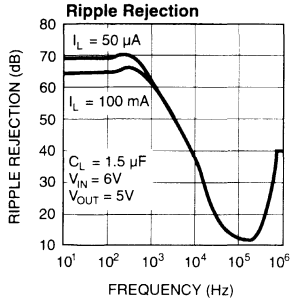


Ripple Rejection

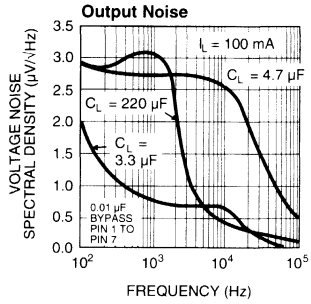


6

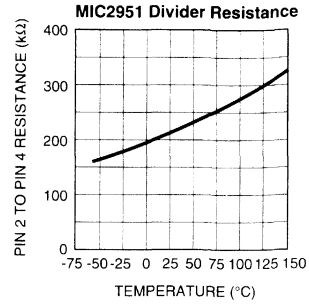
Ripple Rejection



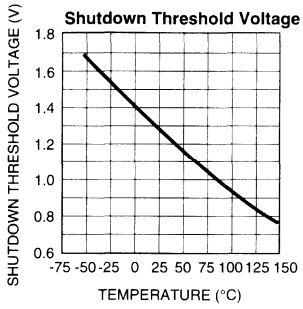
Output Noise



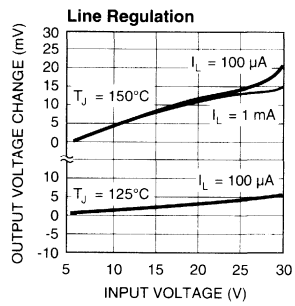
MIC2951 Divider Resistance



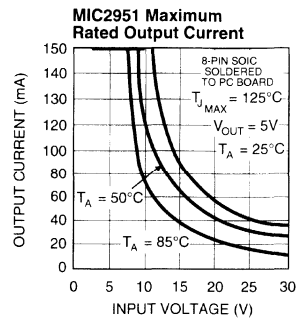
Shutdown Threshold Voltage



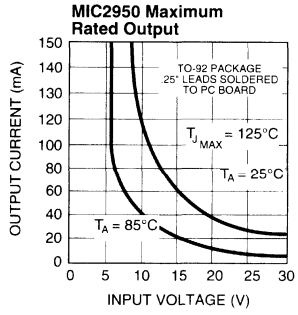
Line Regulation



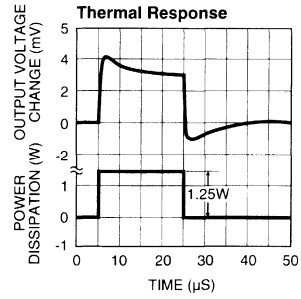
MIC2951 Maximum Rated Output Current



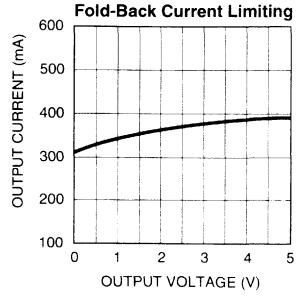
MIC2950 Maximum Rated Output



Thermal Response



Fold-Back Current Limiting



Applications Information

Automotive Applications

The MIC2950/2951 are ideally suited for automotive applications for a variety of reasons. They will operate over a wide range of input voltages, have very low dropout voltages (40mV at light loads), and very low quiescent currents (75μA typical). These features are necessary for use in battery powered systems, such as automobiles. They are also "bulletproof" devices; with the ability to survive both reverse battery (negative transients up to 20V below ground), and load dump (positive transients up to 60V) conditions. A wide operating temperature range with low temperature coefficients is yet another reason to use these versatile regulators in automotive designs.

External Capacitors

A 1.5 μF (or greater) capacitor is required between the MIC2950/MIC2951 output and ground to prevent oscillations due to instability. Most types of tantalum or aluminum electrolytics will be adequate; film types will work, but are costly and therefore not recommended. Many aluminum electrolytics have electrolytes that freeze at about –30°C, so solid tantalums are recommended for operation below –25°C. The important parameters of the capacitor are an effective series resistance of about 5Ω or less and a resonant frequency above 500kHz. The value of this capacitor may be increased without limit.

At lower values of output current, less output capacitance is required for output stability. The capacitor can be reduced to 0.5μF for current below 10mA or 0.15μF for currents below 1 mA. Using the 8-Pin versions at voltages below 5V runs the error amplifier at lower gains so that more output capacitance is needed. For the worst-case situation of a 150mA load at 1.23V output (Output shorted to Feedback) a 5μF (or greater) capacitor should be used.

The MIC2950 will remain stable and in regulation with no load in addition to the internal voltage divider, unlike many other voltage regulators. This is especially important in CMOS RAM keep-alive applications. When setting the output voltage of the MIC2951 version with external resistors, a minimum load of 1μA is recommended.

A 0.1μF capacitor should be placed from the MIC2950/ MIC2951 input to ground if there is more than 10 inches of wire between the input and the AC filter capacitor or if a battery is used as the input.

Stray capacitance to the MIC2951 Feedback terminal (pin 7) can cause instability. This may especially be a problem when using high value external resistors to set the output voltage. Adding a 100pF capacitor between Output and Feedback and increasing the output capacitor to at least 3.3μF will remedy this.

Error Detection Comparator Output

A logic low output will be produced by the comparator whenever the MIC2951 output falls out of regulation by more than approximately 5%. This figure is the comparator's built-in offset of about 60mV divided by the 1.235V reference voltage. (Refer to the block diagram on Page 1). This trip level remains "5% below normal" regardless of the programmed output voltage of the MIC2951. For example, the error flag trip level is typically 4.75V for a 5V output or 11.4V for a 12V output. The out of regulation condition may be due either to low input voltage, current limiting, thermal limiting, or overvoltage on input (over ≅ 40V).

Figure 1 is a timing diagram depicting the $\overline{\text{ERROR}}$ signal and the regulated output voltage as the MIC2951 input is ramped up and down. The $\overline{\text{ERROR}}$ signal becomes valid (low) at about 1.3V input. It goes high at about 5V input (the input voltage at which V_{OUT} = 4.75). Since the MIC2951's dropout voltage is load-dependent (see curve in Typical Performance Characteristics), the input voltage trip point (about 5V) will vary with the load current. The output voltage trip point (approximately 4.75V) does not vary with load.

The error comparator has an open-collector output which requires an external pull-up resistor. Depending on system requirements, this resistor may be returned to the 5V output or some other supply voltage. In determining a value for this resistor, note that while the output is rated to sink 400μA, this sink current adds to battery drain in a low battery condition. Suggested values range from 100k to 1MΩ. The resistor is not required if this output is unused.

In shutdown mode, $\overline{\text{ERROR}}$ will go high if it has been pulled up to an external 5V supply. To avoid this invalid response, $\overline{\text{ERROR}}$ should be pulled up to V_{OUT} (See figure 2).

Programming the Output Voltage (MIC2951)

The MIC2951 may be pin-strapped for 5V using its internal voltage divider by tying Pin 1 (output) to Pin 2 (sense) and Pin 7 (feedback) to Pin 6 (5V Tap). Alternatively, it may be programmed for any output voltage between its 1.235V reference and its 30V maximum rating. An external pair of resistors is required, as shown in Figure 2.

The complete equation for the output voltage is

$$V_{OUT} = V_{REF} \times \{ 1 + R_1/R_2 \} + I_{FB} R_1$$

where V_{REF} is the nominal 1.235 reference voltage and I_{FB} is the feedback pin bias current, nominally -20nA. The minimum recommended load current of 1 μA forces an upper limit of 1.2MΩ on the value of R_2, if the regulator must work with no load (a condition often found in CMOS in standby), I_{FB} will produce a 2% typical error in V_{OUT} which may be eliminated at room temperature by trimming R_1. For better accuracy, choosing R_2 = 100k reduces this error to 0.17% while increasing the resistor program current to 12 μA. Since the MIC2951 typically draws 60 μA at no load with Pin 2 open-circuited, this is a small price to pay.

Reducing Output Noise

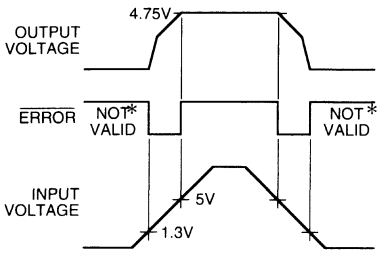
In reference applications it may be advantageous to reduce

the AC noise present at the output. One method is to reduce the regulator bandwidth by increasing the size of the output capacitor. This is the only method by which noise can be reduced on the 3 lead LP2950 and is relatively inefficient, as increasing the capacitor from 1μF to 220μF only decreases the noise from 430μV to 160μV rms for a 100kHz bandwidth at 5V output.

Noise can be reduced fourfold by a bypass capacitor across R_1, since it reduces the high frequency gain from 4 to unity. Pick

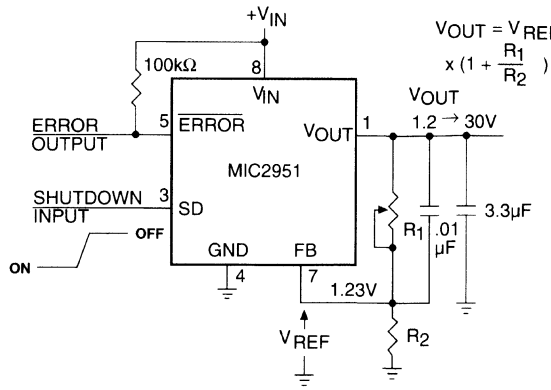
$$C_{BYPASS} \cong \frac{1}{2\pi R_1 \bullet 200\ Hz}$$

or about 0.01 μF. When doing this, the output capacitor must be increased to 3.3 μF to maintain stability. These changes reduce the output noise from 430 μV to 100 μV rms for a 100 kHz bandwidth at 5V output. With the bypass capacitor added, noise no longer scales with output voltage so that improvements are more dramatic at higher output voltages.



* SEE APPLICATIONS INFORMATION

Figure 1. ERROR Output Timing

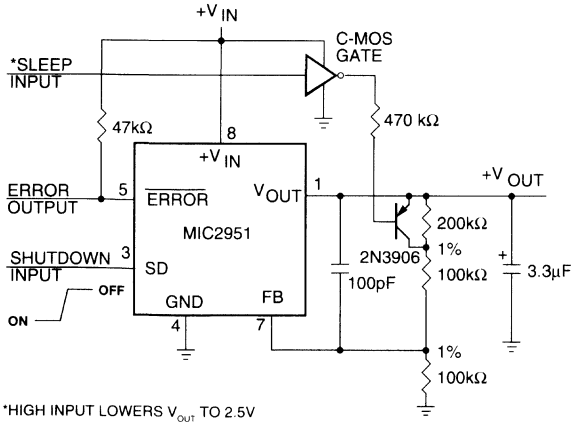


NOTE: PINS 2 AND 6 ARE LEFT OPEN

*SEE APPLICATIONS INFORMATION

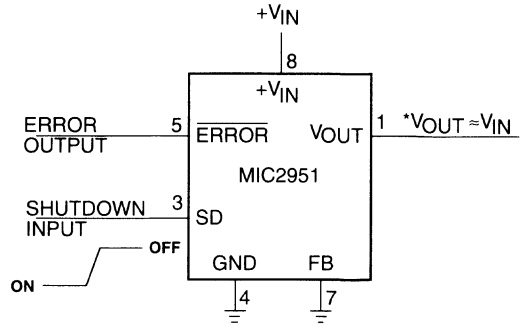
Figure 2. Adjustable Regulator

Typical Applications



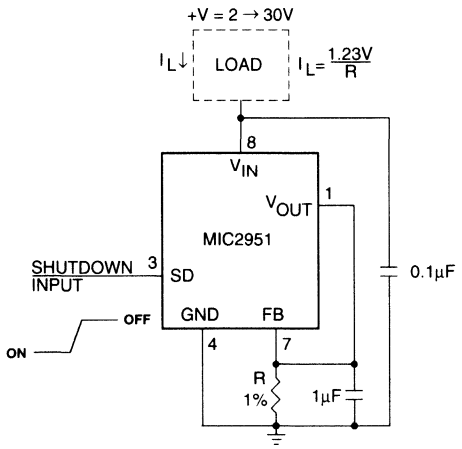
*HIGH INPUT LOWERS V_{OUT} TO 2.5V

5 V Regulator with 2.5 V Sleep Function

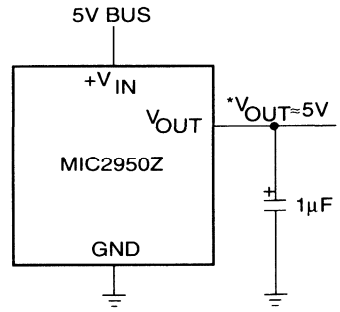


*MINIMUM INPUT-OUTPUT VOLTAGE RANGES FROM 40mV TO 400mV, DEPENDING ON LOAD CURRENT.

Wide Input Voltage Range Current Limiter

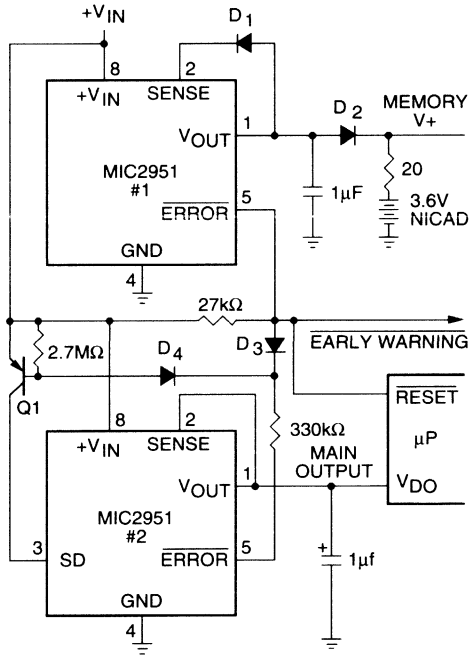


Low Drift Current Source



5 Volt Current Limiter

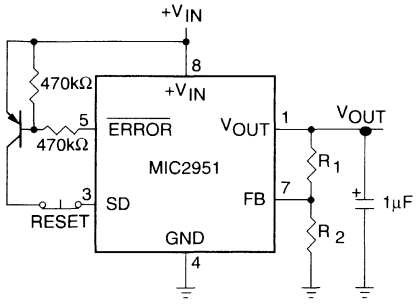
* MINIMUM INPUT-OUTPUT VOLTAGE RANGES FROM 40mV TO 400mV, DEPENDING ON LOAD CURRENT.



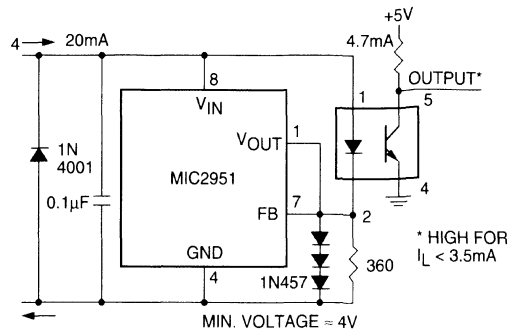
Regulator with Early Warning and Auxiliary Output

- EARLY WARNING FLAG ON LOW INPUT VOLTAGE
- MAIN OUTPUT LATCHES OFF AT LOWER INPUT VOLTAGES
- BATTERY BACKUP ON AUXILIARY OUTPUT

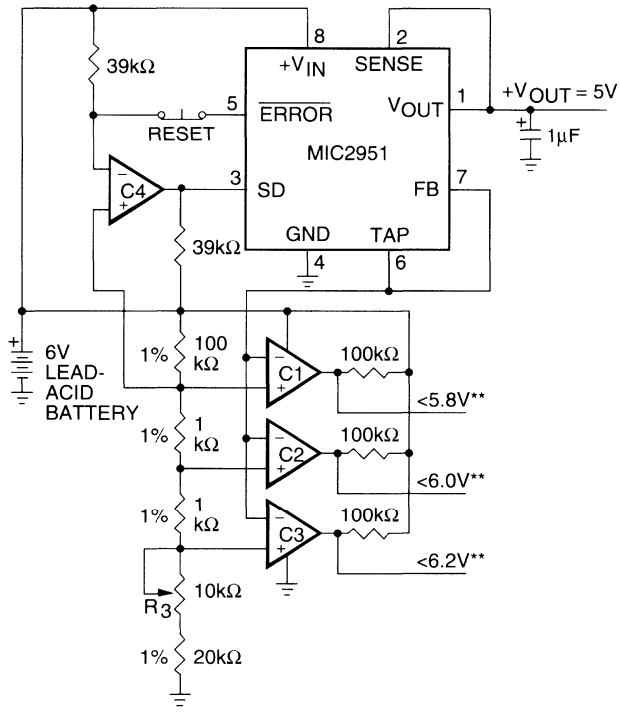
OPERATION: REG. #1'S V_{OUT} IS PROGRAMMED ONE DIODE DROP ABOVE 5 V. ITS ERROR FLAG BECOMES ACTIVE WHEN $V_{IN} \leq 5.7$ V. WHEN V_{IN} DROPS BELOW 5.3 V, THE ERROR FLAG OF REG. #2 BECOMES ACTIVE AND VIA Q1 LATCHES THE MAIN OUTPUT OFF. WHEN V_{IN} AGAIN EXCEEDS 5.7 V REG. #1 IS BACK IN REGULATION AND THE EARLY WARNING SIGNAL RISES, UNLATCHING REG. #2 VIA D3.



Latch Off When Error Flag Occurs

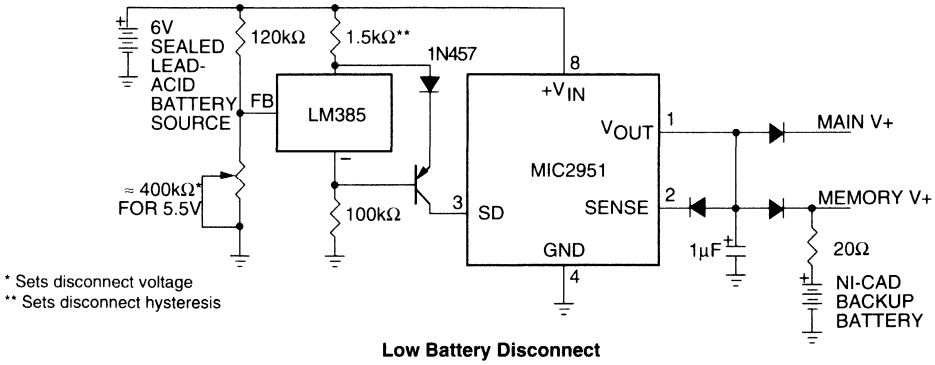


Open Circuit Detector for 4mA to 20mA Current Loop



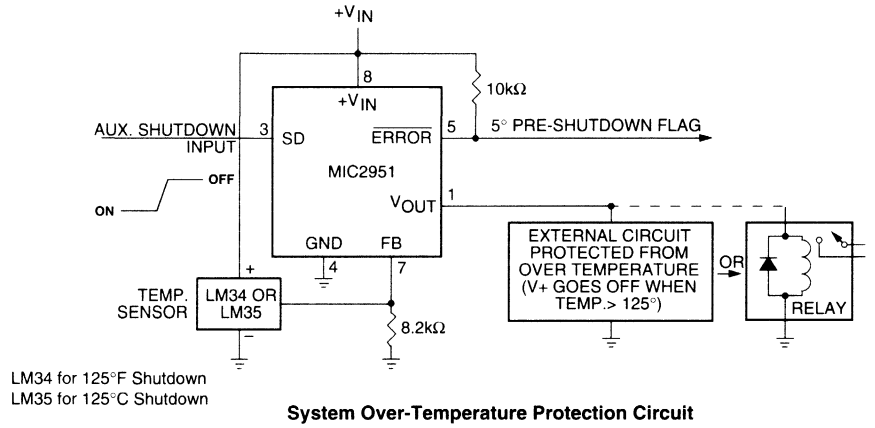
C1 TO C4 ARE COMPARATORS (LP339 OR EQUIVALENT)
*OPTIONAL LATCH OFF WHEN DROP OUT OCCURS. ADJUST R3 FOR C2 SWITCHING WHEN V_{IN} IS 6.0V
**OUTPUTS GO LOW WHEN V_{IN} DROPS BELOW DESIGNATED THRESHOLDS.

Regulator with State-of-Charge Indicator



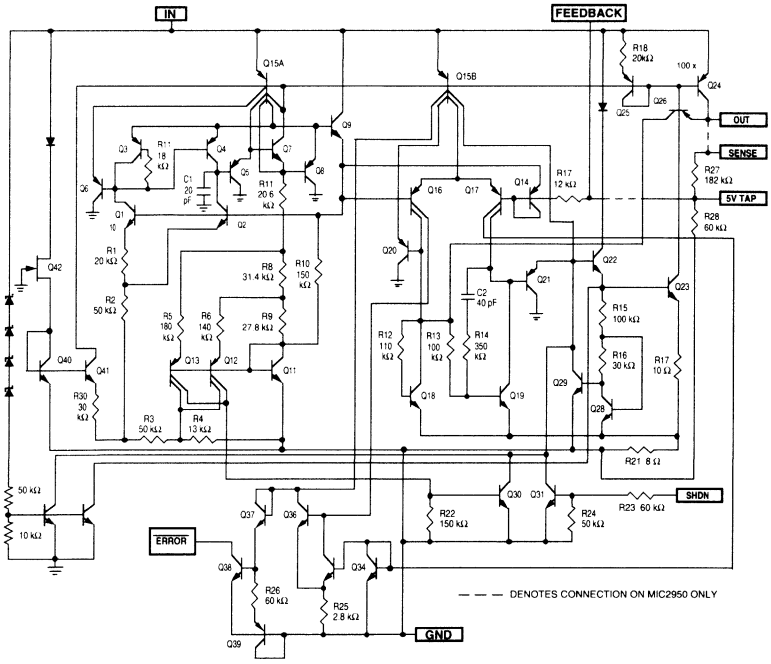
Low Battery Disconnect

For values shown, Regulator shuts down when V_{IN} < 5.5 V and turns on again at 6.0 V. Current drain in disconnected mode is 150μA.



System Over-Temperature Protection Circuit

Schematic Diagram



MIC2954

250mA Low Drop Out Voltage Regulator

General Description

The MIC2954 is a "bulletproof" efficient voltage regulator with very low dropout voltage (typically 40mV at light loads and 375mV at 250mA), and very low quiescent current (75μA typical). The quiescent current of the MIC2954 increases only slightly in dropout, thus prolonging battery life. Key MIC2954 features include protection against reversed battery, fold-back current limiting, and automotive load dump protection (60V positive transient).

The MIC2954-07/08BM is an adjustable version that includes an error flag output that warns of a low output voltage, which is often due to failing batteries on the input. This may also be used as a power-on reset. A logic-compatible shutdown input is provided which enables the regulator to be switched on and off. This part may be pin-strapped for 5V output, or programmed from 1.24 V to 29 V with the use of two external resistors.

The MIC2954 is available in two voltage tolerances, ±0.5% maximum and ±1% maximum. Both are guaranteed for junction temperatures from –40°C to +125°C.

The MIC2954 has a very low output voltage temperature coefficient and extremely good load and line regulation (0.04% typical).

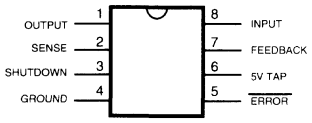
Features

- High accuracy 5V, guaranteed 250mA output
- Low quiescent current
- Low dropout voltage
- Extremely tight load and line regulation
- Very low temperature coefficient
- Current and thermal limiting
- Input can withstand –20V reverse battery and +60V positive transients
- Error flag warns of output dropout
- Logic-controlled electronic shutdown
- Output programmable from 1.24V to 29V(MIC2954-07/08BM)
- Available in TO-220, TO-92, and Surface Mount SOT-223 and SO-8 packages.

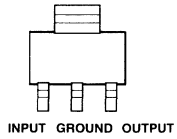
Applications

- Battery Powered Equipment
- Cellular Telephones
- Laptop, Notebook, and Palmtop Computers
- PCMCIA V_{CC} and V_{PP} Regulation/Switching
- Bar Code Scanners
- Automotive Electronics
- SMPS Post-Regulator/ DC to DC Modules
- Voltage Reference
- High Efficiency Linear Power Supplies

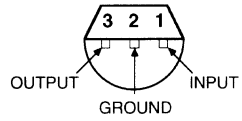
Pin Configuration



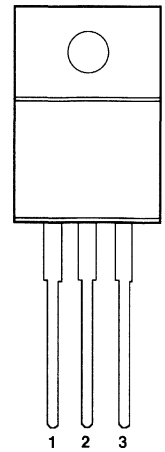
SO Package
(MIC2954-07BM, -08BM)



SOT-223 Package
(MIC2954-02BS, -03BS)



TO-92 Package
(MIC2954-02BZ, -03BZ)



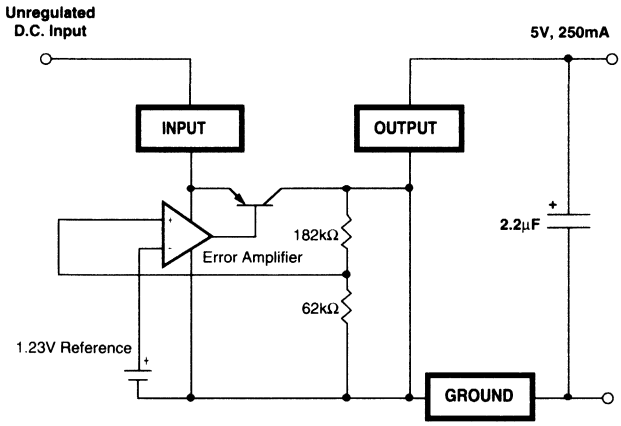
TO-220 Package Front View
(MIC2954-02BT, -03BT)

Ordering Information

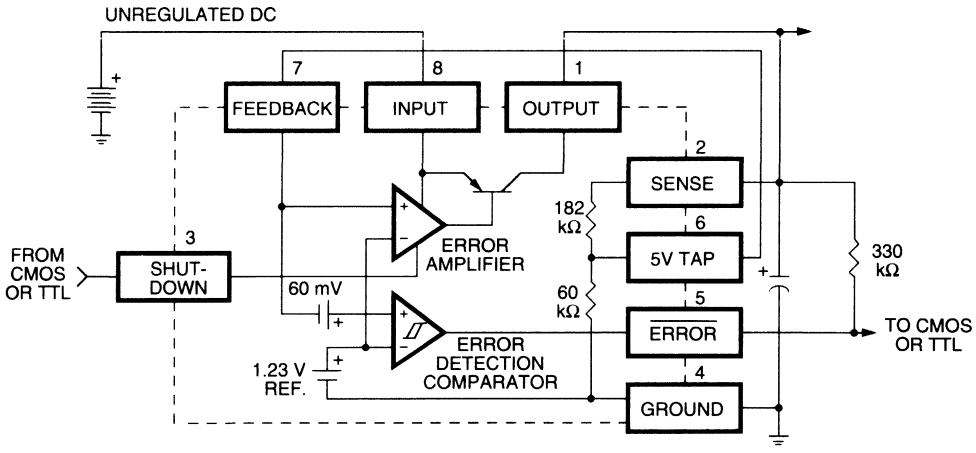
Part Number	Temperature Range*	Package	Accuracy
MIC2954-02BT	–40°C to +125°C	TO-220	0.5%
MIC2954-03BT	–40°C to +125°C	TO-220	1.0%
MIC2954-02BS	–40°C to +125°C	SOT-223	0.5%
MIC2954-03BS	–40°C to +125°C	SOT-223	1.0%
MIC2954-02BZ	–40°C to +125°C	TO-92	0.5%
MIC2954-03BZ	–40°C to +125°C	TO-92	1.0%
MIC2954-07BM	–40°C to +125°C	8-Pin SO-8	0.5%
MIC2954-08BM	–40°C to +125°C	8-Pin SO-8	1.0%

* Junction temperatures

MIC2954-02BT/BZ & 2954-03BT/BZ Block Diagram



MIC2954-07BM & 2954-08BM Block Diagram



6

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact your local Micrel representative/distributor for availability and specifications.

Power Dissipation (Note 1)	Internally Limited	Input Supply Voltage	–20V to +60V
Lead Temperature (Soldering, 5 seconds)	260°C	Feedback Input Voltage (Notes 10 and 11)	–1.5V to +26V
Storage Temperature Range	–65°C to +150°C	Shutdown Input Voltage	–0.3V to +30V
Operating Junction Temperature Range	–40°C to +125°C	Error Comparator Output Voltage	–0.3V to +30V
		ESD Rating	>±2000V

Electrical Characteristics

Limits in standard typeface are for T_J = 25°C and limits in **boldface** apply over the full operating temperature range. Unless otherwise specified, V_{IN} = 6V, I_L = 1mA, C_L = 2.2µF. The MIC2954-07BM,-08BM Feedback pin is tied to the 5V Tap and Output is tied to Output Sense (V_{OUT} = 5V) and $V_{SHUTDOWN} \leq 0.6V$.

Symbol	Parameter	Conditions	Typical	MIC2954-02/-07 Min	MIC2954-02/-07 Max	MIC2954-03/-08 Min	MIC2954-03/-08 Max	Units
V_O	Output Voltage		5.0	4.975	5.025	4.950	5.050	V
				4.940	**5.060**	**4.900**	**5.100**	
		1mA ≤ I_L ≤250mA	5.0	**4.930**	**5.070**	**4.880**	**5.120**	
$\frac{\Delta V_O}{\Delta T}$	Output Voltage Temperature Coef.	(Note 2)	**20**		**100**		**150**	ppm/°C
$\frac{\Delta V_O}{V_O}$	Line Regulation	V_{IN} = 6V to 26V	0.03		0.10		0.20	%
			(Note 3)		**0.20**		**0.40**	
$\frac{\Delta V_O}{V_O}$	Load Regulation	I_L = 1 to 250mA	0.04		0.16		0.20	%
		I_L = 0.1 to 1mA (Note 4)			**0.20**		**0.30**	
$V_{IN} - V_O$	Dropout Voltage (Note 5)	I_L = 1mA	60		100		100	mV
					150		**150**	
		I_L = 50mA	220		250		250	
					420		**420**	
		I_L = 100mA	250		300		300	
					450		**450**	
		I_L = 250mA	375		450		450	
					600		**600**	
I_{GND}	Ground Pin Current (Note 6)	I_L = 1mA	90		150		150	µA
					180		**180**	
		I_L = 50mA	0.5		1		1	mA
					2		**2**	
		I_L = 100mA	1.7		2.5		2.5	
					3.5		**3.5**	
		I_L = 250mA	10		14		14	
					16		**16**	
I_{GNDDO}	Ground Pin Current at Dropout (Note 6)	V_{IN} = 4.5V	180		**300**		**300**	µA
I_{LIMIT}	Current Limit	V_{OUT} = 0V (Note 7)			750		750	mA
					800		**800**	
$\frac{\Delta V_O}{\Delta P_D}$	Thermal Regulation	(Note 8)	0.05		0.2		0.2	%/W
e_n	Output Noise Voltage (10Hz to 100kHz) I_L = 100mA	C_L = 2.2µF	400					µV RMS
		C_L = 33µF	260					

Electrical Characteristics, MIC2954-07BM/-08BM,(Continued)

Parameter	Conditions	MIC2954-07BM			MIC2954-08BM			Units
		Typ.	Min	Max	Typ.	Min	Max	
Reference Voltage		1.235	1.220 **1.200**	1.250 **1.260**	1.235	1.210 **1.200**	1.260 **1.270**	V V max
Reference Voltage	(Note 9)		**1.190**	**1.270**		**1.185**	**1.285**	V
Feedback Pin Bias Current		20		40 **60**	20		40 **60**	nA
Reference Voltage Temperature Coefficient	(Note 8)	20			50			ppm/°C
Feedback Pin Bias Current Temperature Coefficient		0.1			0.1			nA/°C
Error Comparator								
Output Leakage Current	V_{OH} = 30V	0.01		1.00 **2.00**	0.01		1.00 **2.00**	µA
Output Low Voltage	V_{IN} = 4.5V I_{OL} = 400µA	150		250 **400**	150		250 **400**	mV
Upper Threshold Voltage	(Note 10)	60	40 **25**		60	40 **25**		mV
Lower Threshold Voltage	(Note 10)	75		95 **140**	75		95 **140**	mV
Hysteresis	(Note 10)	15			15			mV
Shutdown Input								
Input Logic Voltage	Low (ON) High (OFF)	1.3	 **2.0**	**0.7**	1.3	 **2.0**	**0.7**	V
Shutdown Pin Input Current	$V_{SHUTDOWN}$ = 2.4V	30		50 **100**	30		50 **100**	µA
	$V_{SHUTDOWN}$ = 30V	450		600 **750**	450		600 **750**	µA
Regulator Output Current in Shutdown	(Note 11)	3		10 **20**	3		10 **20**	µA

6

Note 1: Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device outside of its rated operating conditions. The maximum allowable power dissipation is a function of the maximum junction temperature, $T_{J(MAX)}$, the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using: $P_{(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$ Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the regulator will go into thermal shutdown. The junction to ambient thermal resistance of the MIC2954BM is 160°C/W mounted on a PC board. (See MIC2954BM Thermal Characteristics section for further information.

Note 2: Output voltage temperature coefficient is defined as the worst case voltage change divided by the total temperature range.

Note 3: Line regulation for the MIC2954 is tested at 150°C for I_L = 1 mA. For I_L = 100 µA and T_J = 125°C, line regulation is guaranteed by design to 0.2%. See Typical Performance Characteristics for line regulation versus temperature and load current.

Note 4: Regulation is measured at constant junction temperature using low duty cycle pulse testing Parts are tested separately for load regulation in the load ranges 0.1mA to 1mA and 1mA to 250mA. Changes in output voltage due to heating effects are covered by the thermal regulation specification.

Note 5: Dropout Voltage is defined as the input to output differential at which the output voltage drops 100 mV below its nominal value measured at 1V differential. At very low values of programmed output voltage, the minimum input supply voltage of 2 V (2.3 V over temperature) must be taken into account.

Note 6: Ground pin current is the regulator quiescent current. The total current drawn from the source is the sum of the load current plus the ground pin current.

Note 7: The MIC2954 features fold-back current limiting. The short circuit (V_{OUT} = 0V) current limit is less than the maximum current with normal output voltage.

Note 8: Thermal regulation is defined as the change in output voltage at a time T after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for a 200mA load pulse at V_{IN} = 20V (a 4W pulse) for T = 10ms.

Note 9: $V_{REF} \leq V_{OUT} \leq (V_{IN} - 1\ V)$, $2.3V \leq V_{IN} \leq 30V$, $100\ \mu A < I_L \leq 250\ mA$, $T_J \leq T_{J\ MAX}$.

Note 10: Comparator thresholds are expressed in terms of a voltage differential at the Feedback terminal below the nominal reference voltage measured at 6V input. To express these thresholds in terms of output voltage change, multiply by the error amplifier gain = V_{OUT} /V_{REF} = (R1 + R2)/R2. For example, at a programmed output voltage of 5V, the Error output is guaranteed to go low when the output drops by 95 mV x 5V/1.235 V = 384 mV. Thresholds remain constant as a percent of VOUT as VOUT is varied, with the dropout warning occurring at typically 5% below nominal, 7.5% guaranteed.

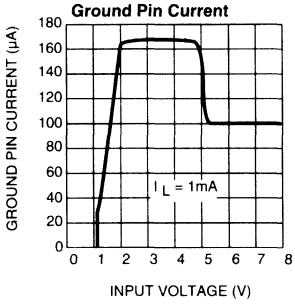
Note 11: $V_{SHUTDOWN} \geq 2\ V$, $V_{IN} \leq 30\ V$, $V_{OUT} = 0$, with Feedback pin tied to 5V Tap.

Note 12: When used in dual supply systems where the regulator load is returned to a negative supply, the output voltage must be diode clamped to ground.

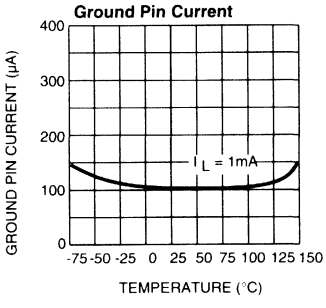
Note 13: Maximum positive supply voltage of 60 V must be of limited duration (< 100 ms) and duty cycle (≤ 1%). The maximum continuous supply voltage is 30 V.

Typical Characteristics

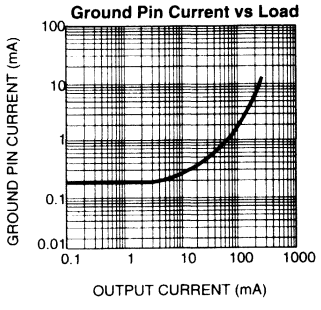
Ground Pin Current



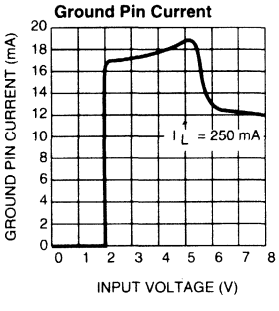
Ground Pin Current



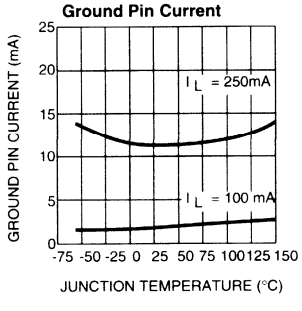
Ground Pin Current vs Load



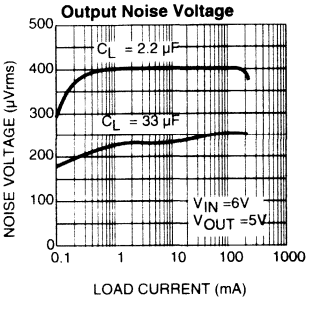
Ground Pin Current



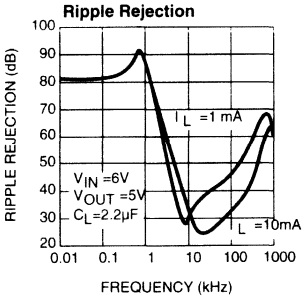
Ground Pin Current



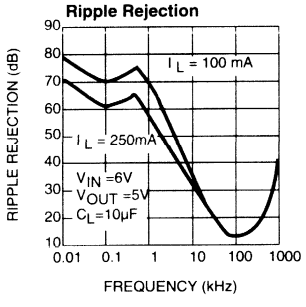
Output Noise Voltage



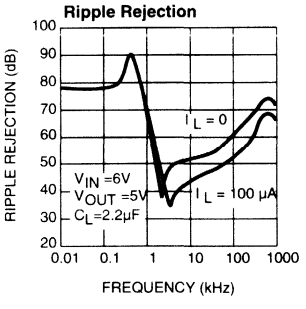
Ripple Rejection



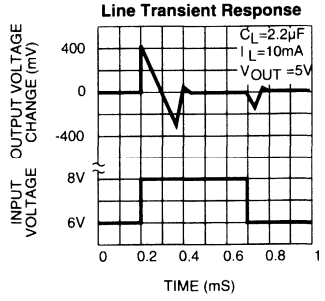
Ripple Rejection



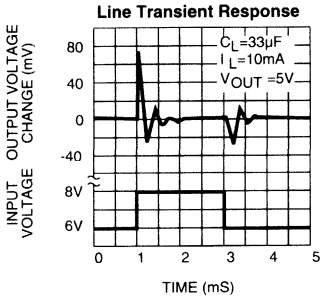
Ripple Rejection



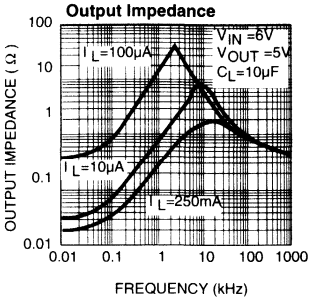
Line Transient Response



Line Transient Response

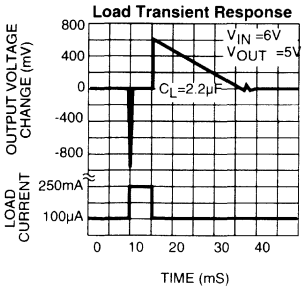


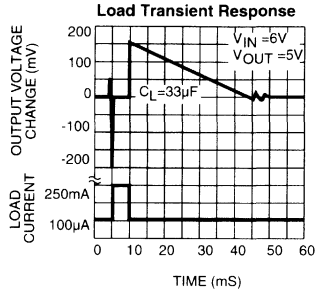
Output Impedance

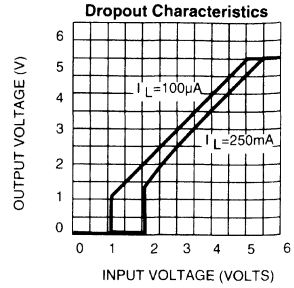


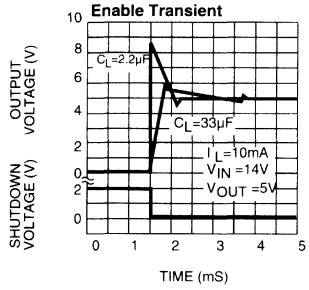
6

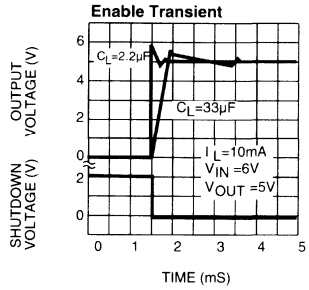
Typical Characteristics, Continued

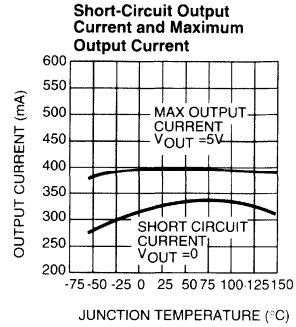


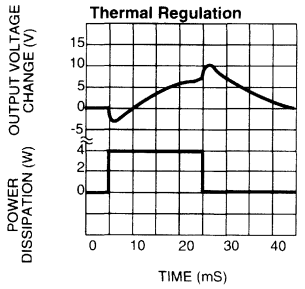


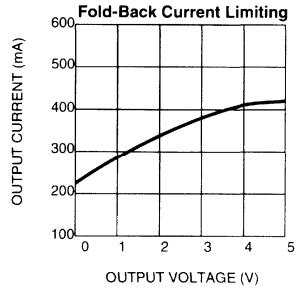












Applications Information

External Capacitors

A 2.2µF (or greater) capacitor is required between the MIC2954 output and ground to prevent oscillations due to instability. Most types of tantalum or aluminum electrolytics will be adequate; film types will work, but are costly and therefore not recommended. Many aluminum electrolytics have electrolytes that freeze at about –30°C, so solid tantalums are recommended for operation below –25°C. The important parameters of the capacitor are an effective series resistance of about 5Ω or less and a resonant frequency above 500kHz. The value of this capacitor may be increased without limit.

At lower values of output current, less output capacitance is required for output stability. The capacitor can be reduced to 0.5µF for current below 10mA or 0.15µF for currents below 1 mA. Adjusting the MIC2954-07BM/-08BM to voltages below 5V runs the error amplifier at lower gains so that more output capacitance is needed. For the worst-case situation of a 250mA load at 1.23V output (Output shorted to Feedback) a 5µF (or greater) capacitor should be used.

The MIC2954 will remain stable and in regulation with no load in addition to the internal voltage divider, unlike many other voltage regulators. This is especially important in CMOS RAM keep-alive applications. When setting the output voltage of the MIC2954-07BM/-08BM version with external resistors, a minimum load of 1µA is recommended.

A 0.1µF capacitor should be placed from the MIC2954 input to ground if there is more than 10 inches of wire between the input and the AC filter capacitor or if a battery is used as the input.

Stray capacitance to the MIC2954-07BM/-08BM Feedback terminal (pin 7) can cause instability. This may especially be a problem when using high value external resistors to set the output voltage. Adding a 100pF capacitor between Output and Feedback and increasing the output capacitor to at least 3.3µF will remedy this.

Error Detection Comparator Output (MIC2954-07BM/-08BM)

A logic low output will be produced by the comparator whenever the MIC2954BM output falls out of regulation by more than approximately 5%. This figure is the comparator's built-in offset of about 60mV divided by the 1.235V reference voltage. (Refer to the block diagram on Page 1). This trip level remains "5% below normal" regardless of the programmed output voltage of the MIC2954-07BM/-08BM. For example, the error flag trip level is typically 4.75V for a 5V output or 11.4V for a 12V output. The out of regulation condition may be due either to low input voltage, current limiting, or thermal limiting.

Figure 1 is a timing diagram depicting the $\overline{\text{ERROR}}$ signal and the regulated output voltage as the MIC2954-07BM/-08BM input is ramped up and down. The $\overline{\text{ERROR}}$ signal becomes valid (low) at about 1.3V input. It goes high at about 5V input (the input voltage at which V_{OUT} = 4.75). Since the MIC2954-07BM/-08BM's dropout voltage is load-dependent (see curve in Typical Performance Characteristics), the input voltage trip point (about 5V) will vary with the load current. The output voltage trip point (approximately 4.75V) does not vary with load.

The error comparator has an open-collector output which requires an external pull-up resistor. Depending on system requirements, this resistor may be returned to the 5V output or some other supply voltage. In determining a value for this resistor, note that while the output is rated to sink 400µA, this sink current adds to battery drain in a low battery condition. Suggested values range from 100k to 1MΩ. The resistor is not required if this output is unused.

In shutdown mode, $\overline{\text{ERROR}}$ will go high if it has been pulled up to an external 5V supply. To avoid this invalid response, $\overline{\text{ERROR}}$ should be pulled up to V_{OUT}.

Programming the Output Voltage (MIC2954-07BM/-08BM)

The MIC2954-07BM/-08BM may be pin-strapped for 5V using its internal voltage divider by tying Pin 1 (output) to Pin 2 (sense) and Pin 7 (feedback) to Pin 6 (5V Tap). Alternatively, it may be programmed for any output voltage between its 1.235V reference and its 30V maximum rating. An external pair of resistors is required, as shown in Figure 2.

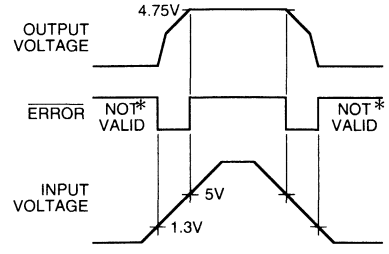
The complete equation for the output voltage is

$$V_{OUT} = V_{REF} \times \{ 1 + R_1/R_2 \} + I_{FB} R_1$$

where V_{REF} is the nominal 1.235 reference voltage and I_{FB} is the feedback pin bias current, nominally -20nA. The minimum recommended load current of 1 µA forces an upper limit of 1.2MΩ on the value of R_2, if the regulator must work with no load (a condition often found in CMOS in standby), I_{FB} will produce a 2% typical error in V_{OUT} which may be eliminated at room temperature by trimming R_1. For better accuracy, choosing R_2 = 100k reduces this error to 0.17% while increasing the resistor program current to 12 µA. Since the MIC2954-07BM/-08BM typically draws 60 µA at no load with Pin 2 open-circuited, this is a negligible addition.

Reducing Output Noise

In reference applications it may be advantageous to reduce the AC noise present at the output. One method is to reduce the regulator bandwidth by increasing the size of the output capacitor. This is relatively inefficient, as increasing the



* SEE APPLICATIONS INFORMATION

Figure 1. $\overline{\text{ERROR}}$ Output Timing

capacitor from 1 μF to 220 μF only decreases the noise from 430μV to 160μV_{RMS} for a 100kHz bandwidth at 5V output. Noise can be reduced fourfold by a bypass capacitor across R_1, since it reduces the high frequency gain from 4 to unity. Pick

$$C_{BYPASS} \cong \frac{1}{2\pi R_1 \bullet 200\ Hz}$$

or about 0.01 μF. When doing this, the output capacitor must be increased to 3.3 μF to maintain stability. These changes reduce the output noise from 430 μV to 100 μV rms for a 100 kHz bandwidth at 5V output. With the bypass capacitor added, noise no longer scales with output voltage so that improvements are more dramatic at higher output voltages.

Automotive Applications

The MIC2954 is ideally suited for automotive applications for a variety of reasons. It will operate over a wide range of input voltages with very low dropout voltages (40mV at light loads), and very low quiescent currents (75μA typical). These features are necessary for use in battery powered systems, such as automobiles. It is a "bulletproof" device with the ability to survive both reverse battery (negative transients up to 20V below ground), and load dump (positive transients up to 60V) conditions. A wide operating temperature range with low temperature coefficients is yet another reason to use these versatile regulators in automotive designs.

Typical Applications

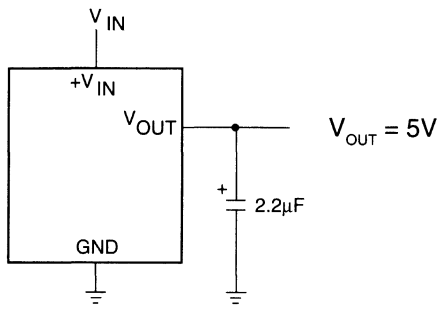


Figure 2. MIC2954 Fixed +5V Regulator

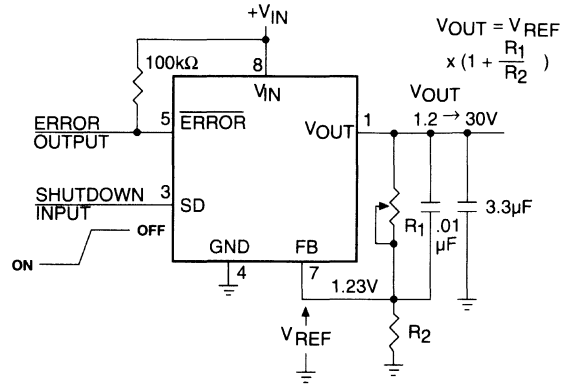
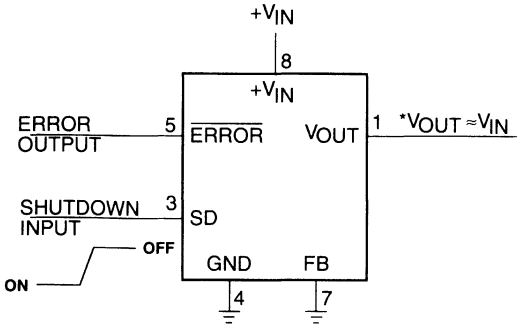
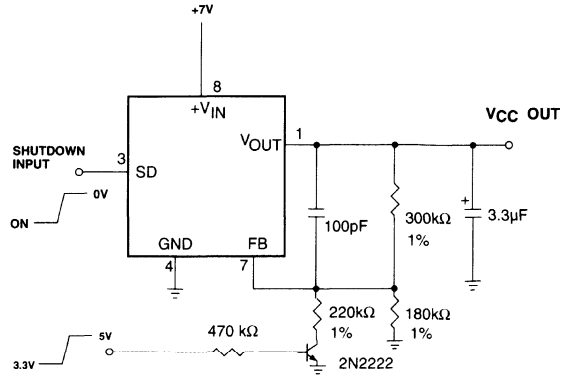


Figure 3. MIC2954-07BM/-08BM Adjustable Regulator



*MINIMUM INPUT-OUTPUT VOLTAGE RANGES FROM 40mV TO 400mV, DEPENDING ON LOAD CURRENT.

Figure 4. MIC2954-07BM/-08BM Wide Input Voltage Range Current Limiter



PIN 3 LOW= ENABLE OUTPUT. Q1 ON = 3.3V, Q1 OFF = 5.0V.

Figure 5. MIC2954-07BM/-08BM 5.0V or 3.3V Selectable Regulator with Shutdown.

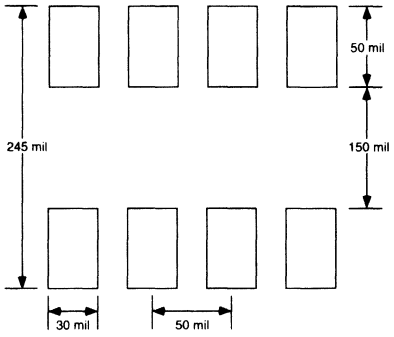
MIC2954-07BM/-08BM Thermal Calculations

Layout Considerations

The MIC2954-07BM/-08BM (8-Pin Surface Mount Package) has the following thermal characteristics when mounted on a single layer copper-clad printed circuit board.

PC Board Dielectric Material	θ_{JA}
FR4	160°C/W
Ceramic	120°C/W

Pad Layout (minimum recommended geometry)



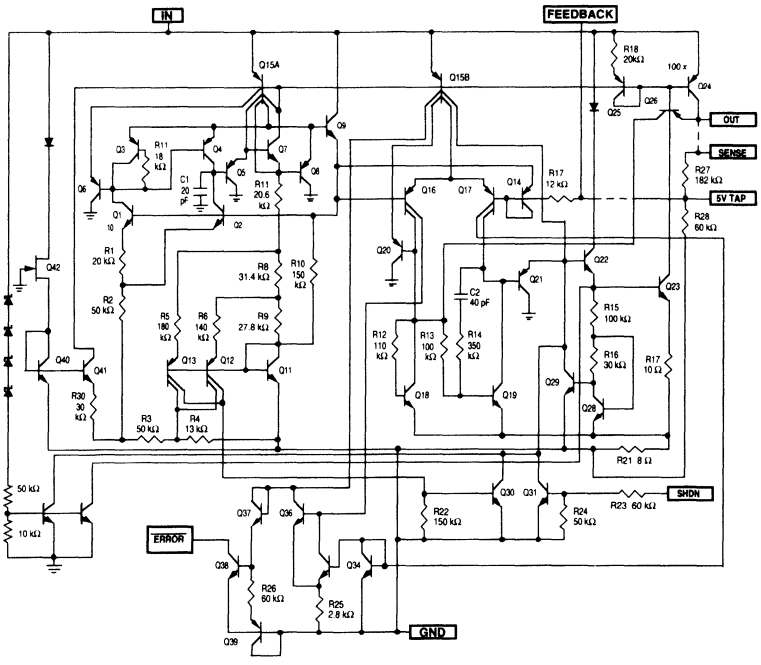
Multi-layer boards having a ground plane, wide traces near the pads, and large supply bus lines provide better thermal conductivity.

Our calculations will use the "worst case" value of 160°C/W, which assumes no ground plane, minimum trace widths, and a FR4 material board.

Nominal Power Dissipation and Die Temperature

The MIC2954-07BM/-08BM at a 55°C ambient temperature will operate reliably at up to 440mW power dissipation when mounted in the "worst case" manner described above. This power level is equivalent to a die temperature of 125°C, the recommended maximum temperature for non-military grade silicon integrated circuits.

Schematic Diagram



MIC5156/5157/5158

Super LDO Regulator Controller

Preliminary

General Description

The MIC5156, MIC5157, and MIC5158 Super Low-Dropout (LDO) Regulator Controllers are single IC solutions for controlling virtually limitless output currents with minimal V_{IN} to V_{OUT} differential voltages. With the exception of a pass transistor and optional current sense resistor, these controllers contain all the functions normally found in an LDO regulator. Designed to control an external N-channel power MOSFET as the linear pass element, the dropout voltage can be as low as the product of the output current times the $R_{DS(ON)}$ of the power MOSFET.

Operating from 3V to 36V, the MIC5156/7/8 use a voltage greater than V_{OUT} for controlling the gate to source voltage of the external N-channel MOSFET. The MIC5156 requires the user to supply this voltage, while the MIC5157 and MIC5158 include an internal charge pump tripler capable of driving a logic FET to 3.3V output with a 3.5V supply (V_{DD}). Full implementation of the tripler is accomplished with the addition of only two small-value capacitors. The tripled voltage, V_{CP}, is clamped to V_{DD} + 16V.

All versions feature a TTL compatible enable pin. A high signal applied to this pin activates the regulator. When low the MIC5156/7/8 typically draws <1μA while forcing the output voltage to ground. Additionally, all versions monitor the output voltage providing an active low open-collector flag when the output voltage falls 6% or more below its nominal value.

For circuits requiring constant current limiting, the MIC5156/7/8 and an external resistor provide a low threshold (35mV nominal) trip point which, when exceeded, removes drive from the external transistor, limiting the maximum output current.

The MIC5156-3.3 and MIC5156-5.0 controllers have internally fixed output voltages. The output voltage of the MIC5156 [adjustable] is configured using two external resistors. The MIC5157 is a fixed output controller which is externally configured to select either 3.3V, 5.0V, or 12V. The MIC5158 can be used as a fixed 5V controller or programmed to any voltage from 1.3V to 36V using only two external resistors.

The MIC5156 is available in an 8-pin plastic DIP, ceramic DIP, or SOIC package. The MIC5157 and MIC5158 are available in a 14-pin plastic DIP, ceramic DIP, or SOIC. The plastic DIP and SOIC versions operate from –40°C to +85°C. The ceramic DIP versions cover the –55°C to +125°C military temperature range.

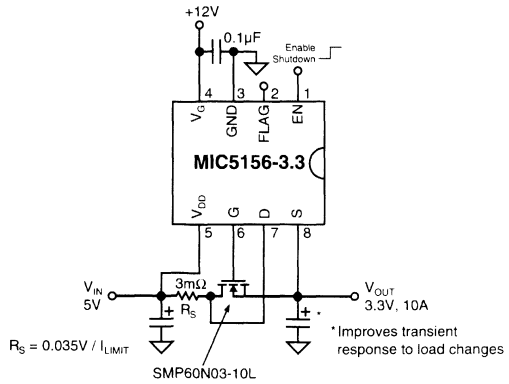
Features

- 6mA typical operating current
- <1μA typical standby current
- Low external parts count
- Optional current limit (35mV typical threshold)
- 1% initial output voltage tolerance
- 2% output voltage tolerance over temperature
- Fixed output voltages of 3.3V, 5.0V (MIC5156)
- Fixed output voltages of 3.3V, 5.0V, 12V (MIC5157)
- Programmable (1.3 to 36V) with 2 resistors (MIC5156/8)
- Internal charge pump voltage tripler (MIC5157/8)
- Enable pin to activate or shutdown the regulator
- Internal gate-to-source protective clamp
- All versions available in DIP and SOIC

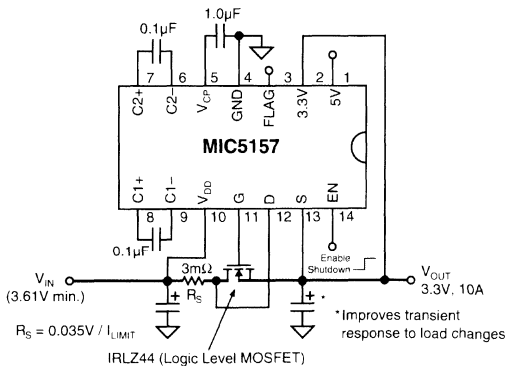
Applications

- Ultra-high current ultra-low dropout voltage regulation
- Low parts count 5.0V to 3.3V computer supply
- Low noise/low-dropout SMPS post regulator

Typical Applications



10A 5V to 3.3V Desktop Computer Regulator



10A Low-Dropout Voltage Regulator

Ordering Information MIC5156

Part Number	Temperature Range	Voltage	Package
MIC5156-3.3BN	–40°C to +85°C	3.3V	8-pin P-DIP
MIC5156-5.0BN	–40°C to +85°C	5.0V	8-pin P-DIP
MIC5156BN	–40°C to +85°C	Adjustable	8-pin P-DIP
MIC5156-3.3BM	–40°C to +85°C	3.3V	8-pin SOIC
MIC5156-5.0BM	–40°C to +85°C	5.0V	8-pin SOIC
MIC5156BM	–40°C to +85°C	Adjustable	8-pin SOIC
MIC5156-3.3AJ	–55°C to +125°C	3.3V	8-pin CerDIP
MIC5156-5.0AJ	–55°C to +125°C	5.0V	8-pin CerDIP
MIC5156AJ	–55°C to +125°C	Adjustable	8-pin CerDIP

Ordering Information MIC5157

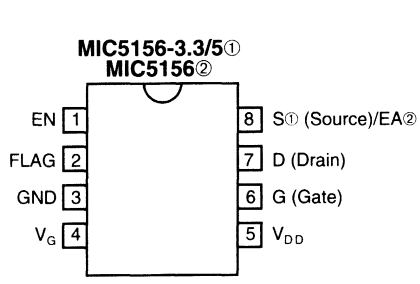
Part Number	Temperature Range	Voltage	Package
MIC5157BN	–40°C to +85°C	Selectable	14-pin P-DIP
MIC5157BM	–40°C to +85°C	Selectable	14-pin SOIC
MIC5157AJ	–55°C to +125°C	Selectable	14-pin CerDIP

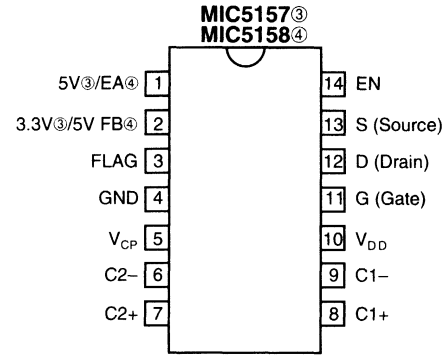
Ordering Information MIC5158

Part Number	Temperature Range	Voltage	Package
MIC5158BN	–40°C to +85°C	5.0V/Adj.	14-pin P-DIP
MIC5158BM	–40°C to +85°C	5.0V/Adj.	14-pin SOIC
MIC5158AJ	–55°C to +125°C	5.0V/Adj.	14-pin CerDIP

6

Pin Configuration





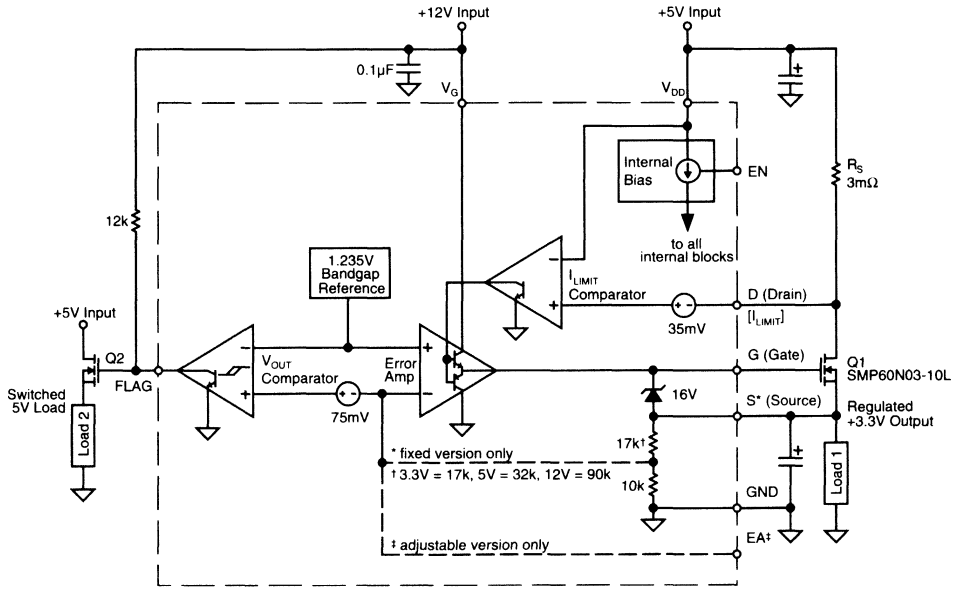
Pin Description MIC5156 (8-pin)

Pin Number	Pin Name	Pin Function
1	EN	Enable (Input): TTL high enables regulator; TTL low shuts down regulator.
2	FLAG	Output Flag (Output): Open collector output is active (low) when V_{OUT} is more than 6% below nominal output. Circuit has 3% hysteresis.
3	GND	Circuit ground.
4	V_G	N-channel Gate Drive Supply Voltage: User supplied voltage for driving the gate of the external MOSFET.
5	V_{DD}	Supply Voltage (Input): Supply voltage connection. Connect sense resistor (R_S) to V_{DD} if current limiting used. Connect supply bypass capacitor to ground near device.
6	G	Gate (Output): Drives the gate of the external MOSFET.
7	D	Drain and Current Limit (Input): Connect to external MOSFET drain and external sense resistor (current limit), or connect to V_{DD} and external MOSFET drain (no current limit).
8 (3.3V, 5V)	S	Source (Input): Top of internal resistive divider chain. Connect directly to the load for best load regulation.
8 (adjustable)	EA	Error Amplifier (Input): Connect to external resistive divider.

Pin Description MIC5157, MIC5158 (14-pin)

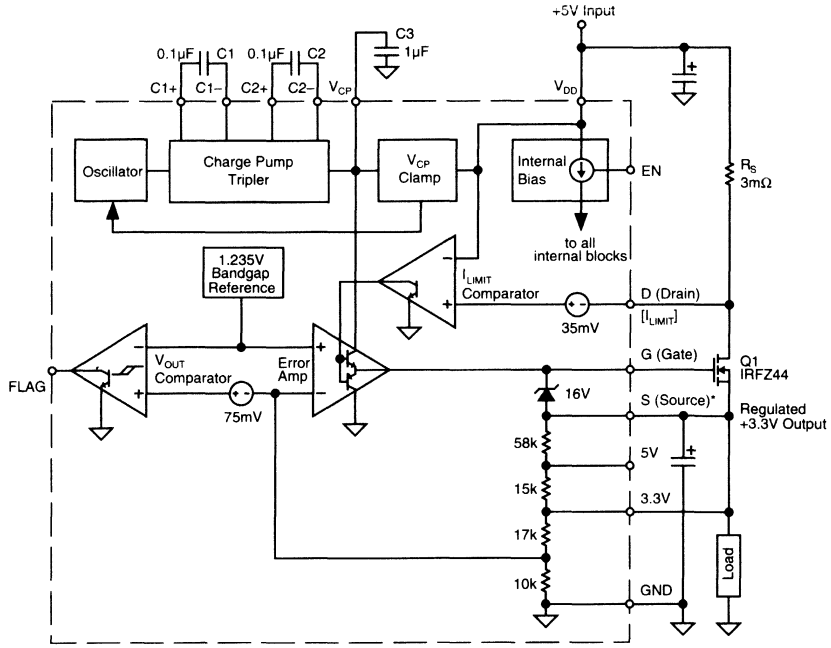
Pin Number	Pin Name	Pin Function
1 (MIC5157)	5V	5V Configuration (Input): Connect to S (source) pin for 5V output.
1 (MIC5158)	EA	Error Amplifier (Input): Connect to external resistive divider to obtain adjustable output.
2 (MIC5157)	3.3V	3.3V Configuration (Input): Connect to S (source) pin for 3.3V output.
2 (MIC5158)	5V FB	5V Feedback (Input): Connect to EA for fixed 5V output.
3	FLAG	Output Voltage Flag (Output): Open collector is active (low) when V_{OUT} is 6% or more below its nominal value.
4	GND	Circuit ground.
5	V_{CP}	Voltage Tripler Output [Filter Capacitor]. Connect a 1µF capacitor to ground.
6	C2–	Charge Pump Capacitor 2: Second stage of internal voltage tripler. Connect a 0.1µF capacitor from C2+ to C2–.
7	C2+	Charge Pump Capacitor 2: See C2– pin.
8	C1+	Charge Pump Capacitor 1: First stage of internal voltage tripler. Connect a 0.1µF capacitor from C1+ to C1–.
9	C1–	Charge Pump Capacitor 1: See C1+ pin.
10	V_{DD}	Supply Voltage (Input): Supply voltage connection. Connect sense resistor (R_S) to V_{DD} if current limiting used. Connect supply bypass capacitor to ground near device.
11	G	Gate (Output): Connect to External MOSFET gate.
12	D	Drain and Current Limit (Input): Connect to external MOSFET drain and external sense resistor (current limit), or connect to V_{DD} and external MOSFET drain (no current limit).
13 (MIC5157)	S	Source and 3.3V/5V Configuration: Top of internal resistor chain. Connect to source of external MOSFET near load for best regulation. Also, for 3.3V connect to 3.3V pin; for 5V connect to 5V pin; for 12V no other connection necessary.
13 (MIC5158)	S	Source (Input): Top of internal resistor chain. Connect to top of external resistive divider and source of external MOSFET near load for best regulation.
14	EN	Enable (Input): TTL high enables regulator; TTL low shuts down regulator.

Block Diagram MIC5156



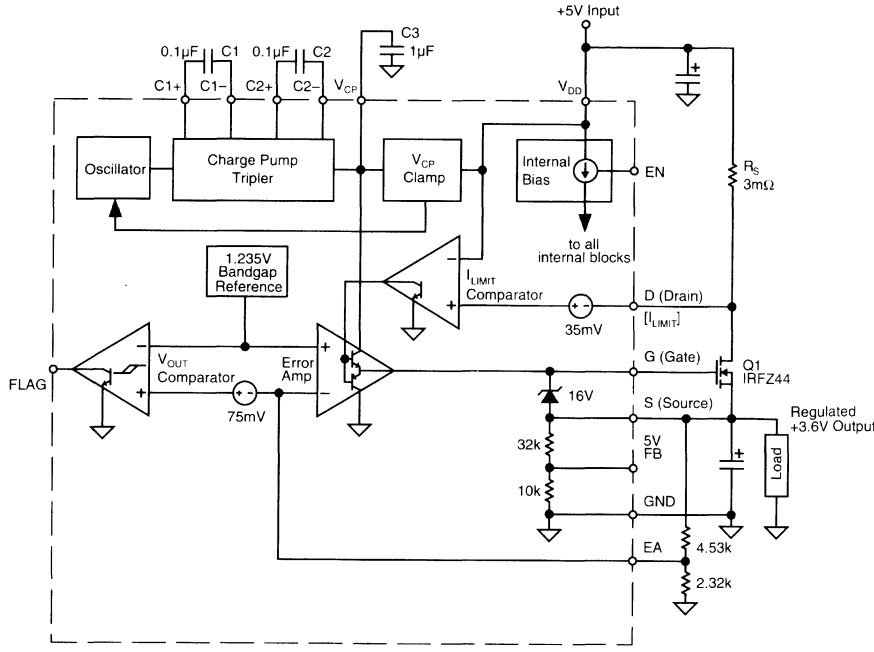
Block Diagram with External Components
Fixed 3.3V Power Supply with 5.0V Load Switch

Block Diagram MIC5157



Block Diagram with External Components
Fixed 3.3V 10A Power Supply

Block Diagram MIC5158



Block Diagram with External Components
Adjustable Power Supply, 3.6V Configuration

Absolute Maximum Ratings

V_{DD} 36V
EN ..... –0.3V to 36V
V_G (MIC5156) 55V
V_{CP} (MIC5157/8) 55V
V_{SOURCE} ..... 1.3 to 36V
FLAG ..... –0.3 to 40V

Ambient Temperature Range
T_A (MIC515xBM/BN) ..... –40°C to +85°C
T_A (MIC515xAJ) ..... –55°C to +125°C
Operating Junction Temperature
T_J ..... 150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature
(soldering 10s) ..... 300°C

Electrical Characteristics T_A = 25°C, V_{DD} = 5V, V_{EN} = 5V

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{DD}	Supply Voltage		3		36	V
$I_{DD(ON)}$ $I_{DD(OFF)}$	Supply Current	Operating, V_{EN} = 5V Shutdown, V_{EN} = 0V		6 0.5		mA µA
V_{IH} V_{IL}	Enable Input Threshold	High Low	2.4	1.2 1.2	 0.8	V V
EN I_B	Enable Input Bias Current	V_{EN} = 2.4V		20		µA
EA V_{OH}	Maximum Gate Voltage (MIC5157/8)	V_{SOURCE} = 0V V_{DD} = 3.5V V_{DD} = 5V V_{DD} = 12V		 7.0 11.3 27		 V V V
EA V_{OL}	Minimum Gate Voltage	V_{SOURCE} > $V_{OUT(NOM)}$		1.0		V
I_{LIM}	Current Limit Threshold	V_{DD} – V_D @ I_{LIM}		35		mV
V_S	Source Voltage	Short gate to source MIC5156-3.3, MIC5157 MIC5156-5. MIC5157. MIC5158 MIC5157, V_{DD} = 7V	 3.267 4.95 11.8	 3.3 5.0 12	 3.333 5.05 12.2	 V V V
V_{BG}	Bandgap Reference Voltage		1.223	1.235	1.247	V
$V_{GS\ MAX}$	Gate to Source Clamp			16		V
V_{FT}	Flag Comparator Threshold	% of nominal V_{SOURCE}		94		%
V_{FH}	Flag Comparator Hysteresis	% of nominal V_{SOURCE}		3		%
V_{SAT}	Flag Comparator Sat. Voltage	I_{FLAG} = 1mA		0.16		V

MIC5200

100mA Low Drop-out Voltage Regulator

Preliminary Information

General Description

The MIC5200 is an efficient linear voltage regulator with very low drop out voltage (typically 17mV at light loads and 200mV at 100mA), and very low ground current (1mA at 100mA output), offering better than 1% initial accuracy with a logic compatible ON/OFF switching input. Designed especially for hand-held battery powered devices, the MIC5200 is switched by a CMOS or TTL compatible logic signal. The ENABLE control may be tied directly to V_{IN} if unneeded. When disabled, power consumption drops nearly to zero. The ground current of the MIC5200 increases only slightly in dropout, further prolonging battery life. Key MIC5200 features include protection against reversed battery, current limiting, and over-temperature shutdown.

The MIC5200 is available in several fixed voltages and accuracy configurations. Other options are available; contact Micrel for details.

Features

- High output voltage accuracy
- Variety of output voltages
- Guaranteed 100mA output
- Low quiescent current
- Low dropout voltage
- Extremely tight load and line regulation
- Very low temperature coefficient
- Current and thermal limiting
- Zero OFF mode current
- Logic-controlled electronic shutdown
- Available in SO-8 and SOT-223 packages

Applications

- Cellular Telephones
- Laptop, Notebook, and Palmtop Computers
- Battery Powered Equipment
- PCMCIA V_{CC} and V_{PP} Regulation/Switching
- Bar Code Scanners
- SMPS Post-Regulator/ DC to DC Modules
- High Efficiency Linear Power Supplies

Ordering Information

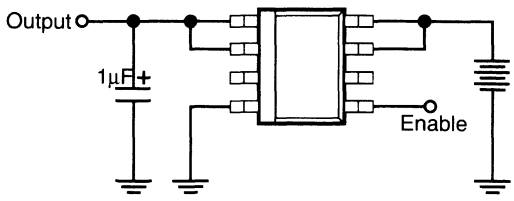
Part Number	Volts	Accuracy	Temperature Range*	Package
MIC5200-3.0BM	3.0	1%	–40°C to +125°C	SO-8
MIC5200-3.3BM	3.3	1%	–40°C to +125°C	SO-8
MIC5200-4.8BM	4.85	1%	–40°C to +125°C	SO-8
MIC5200-5.0BM	5.0	1%	–40°C to +125°C	SO-8
MIC5200-3.0BS	3.0	1%	–40°C to +125°C	SOT-223
MIC5200-3.3BS	3.3	1%	–40°C to +125°C	SOT-223
MIC5200-4.8BS	4.85	1%	–40°C to +125°C	SOT-223
MIC5200-5.0BS	5.0	1%	–40°C to +125°C	SOT-223

* *Junction Temperature*

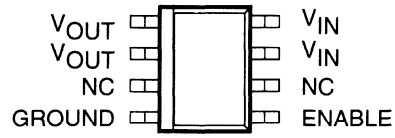
Other voltages are available; contact Micrel for details.

Typical Application

MIC5200-3.3

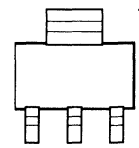


Pin Configuration



MIC5200-xxBM

Both V_{IN} and both V_{OUT} pins must be tied together. ENABLE must be pulled high for operation.



V_{IN} GND V_{OUT}

MIC5200-xxBS

ENABLE may be tied directly to V_{IN}

Absolute Maximum Ratings

Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Electrical specifications do not apply when operating the device beyond its specified **Operating Ratings.**

Power Dissipation	Internally Limited
Lead Temperature (Soldering, 5 seconds)	260°C
Operating Junction Temperature Range	–40°C to +125°C
Input Supply Voltage	–20V to +60V
ENABLE Input Voltage	–20V to +60V
ESD Rating	> 2000V

Recommended Operating Conditions

Input Voltage	2.5V to 26V
Operating Junction Temperature Range	–40°C to +125°C
ENABLE Input Voltage	–20V to V_{IN}

Electrical Characteristics

Limits in standard typeface are for T_J = 25°C and limits in **boldface** apply over the junction temperature range of –40°C to +125°C. Unless otherwise specified, $V_{IN} = V_{OUT} + 1V$, I_L = 1mA, C_L = 3.3µF, and $V_{ENABLE} \geq 2.0V$

Symbol	Parameter	Conditions	Min	Typical	Max	Units
V_O	Output Voltage Accuracy	Variation from specified V_{OUT}	–1 **–2**		1 **2**	%
$\frac{\Delta V_O}{\Delta T}$	Output Voltage Temperature Coef.	(Note 2)		**20**	**100**	ppm/°C
$\frac{\Delta V_O}{V_{IN}}$	Line Regulation	$V_{IN} = V_{OUT}$ + 1 V to 26V		0.004	0.10 **0.40**	%
$\frac{\Delta V_O}{I_L}$	Load Regulation	I_L = 0.1mA to 100mA (Note 3)		0.04	0.16 **0.30**	%
$V_{IN} - V_O$	Dropout Voltage (Note 4)	I_L = 100µA I_L = 20mA I_L = 30mA I_L = 50mA I_L = 100mA		17 **75** 130 **160** 150 **200** 190 **240** 230 **350**		mV
I_{GND}	Quiescent Current	$V_{ENABLE} \leq 0.7V$ (Shutdown)		0.01		µA
I_{GND}	Ground Pin Current	$V_{ENABLE} \geq 2.0V$, I_L = 100µA I_L = 20mA I_L = 30mA I_L = 50mA I_L = 100mA		130 240 300 450 900		µA
PSRR	Ripple Rejection			70		dB
I_{GNDDO}	Ground Pin Current at Dropout	V_{IN} = 0.5V less than specified V_{OUT} I_L = 100µA (Note 5)		270	**330**	µA
I_{LIMIT}	Current Limit	V_{OUT} = 0V		**350**		mA
$\frac{\Delta V_O}{\Delta P_D}$	Thermal Regulation	(Note 6)		0.05		%/W
e_n	Output Noise			30		µV

ENABLE Input

V_{IL}	Input Voltage Level Logic Low Logic High	 OFF ON	 **2.0**		**0.7**	V
I_{IL} I_{IH}	ENABLE Input Current	$V_{IL} \leq 0.7V$ $V_{IH} \geq 2.0V$		0.01 15	 **50**	µA

Note 1: Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device outside of its rated operating conditions. The maximum allowable power dissipation is a function of the maximum junction temperature, $T_{J\,(MAX)}$, the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using: $P_{(MAX)} = (T_{J(MAX)} - T_A)\,\theta_{JA}$. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the regulator will go into thermal shutdown. The θ_{JC} of the MIC5200-xxBS is 15°C/W and θ_{JA} for the MIC5200BM is 160°C/W mounted on a PC board (see "Thermal Considerations" section for further details).

Note 2: Output voltage temperature coefficient is defined as the worst case voltage change divided by the total temperature range.

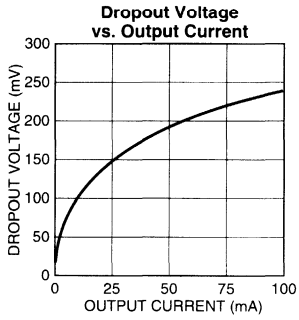
Note 3: Regulation is measured at constant junction temperature using low duty cycle pulse testing. Parts are tested for load regulation in the load range from 0.1mA to 100mA. Changes in output voltage due to heating effects are covered by the thermal regulation specification.

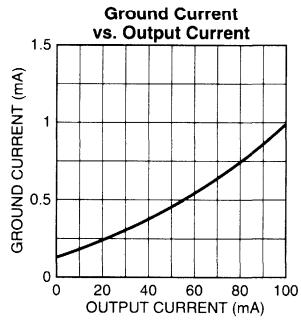
Note 4: Dropout Voltage is defined as the input to output differential at which the output voltage drops 2% below its nominal value measured at 1V differential.

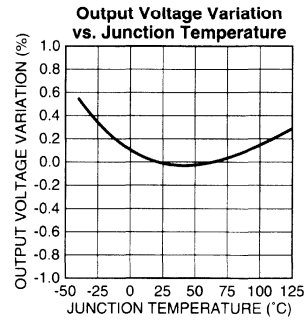
Note 5: Ground pin current is the regulator quiescent current plus pass transistor base current. The total current drawn from the supply is the sum of the load current plus the ground pin current.

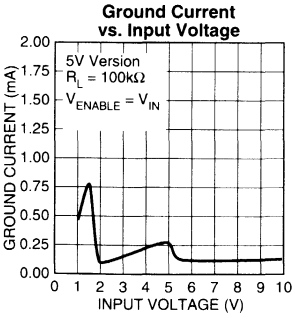
Note 6: Thermal regulation is defined as the change in output voltage at a time T after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for a 100mA load pulse at V_{IN} = 26V for T = 10ms.

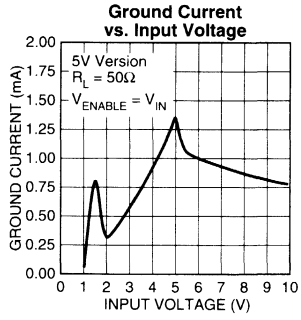
Typical Characteristics











Applications Information

External Capacitors

A 1µF capacitor is recommended between the MIC5200 output and ground to prevent oscillations due to instability. Larger values serve to improve the regulator's transient response. Most types of tantalum or aluminum electrolytics will be adequate; film types will work, but are costly and therefore not recommended. Many aluminum electrolytics have electrolytes that freeze at about –30°C, so solid tantalums are recommended for operation below –25°C. The important parameters of the capacitor are an effective series resistance of about 5Ω or less and a resonant frequency above 500kHz. The value of this capacitor may be increased without limit.

At lower values of output current, less output capacitance is required for output stability. The capacitor can be reduced to 0.47µF for current below 10mA or 0.33µF for currents below 1 mA. A 1µF capacitor should be placed from the MIC5200 input to ground if there is more than 10 inches of wire between the input and the AC filter capacitor or if a battery is used as the input.

The MIC5200 will remain stable and in regulation with no load in addition to the internal voltage divider, unlike many other voltage regulators. This is especially important in CMOS RAM keep-alive applications.

When used in dual supply systems where the regulator load is returned to a negative supply, the output voltage must be diode clamped to ground.

Thermal Considerations

Part I. Layout

The MIC5200-xxBM (8-pin surface mount package) has the following thermal characteristics when mounted on a single layer copper-clad printed circuit board.

PC Board Dielectric	θ_{JA}
FR4	160°C/W
Ceramic	120°C/W

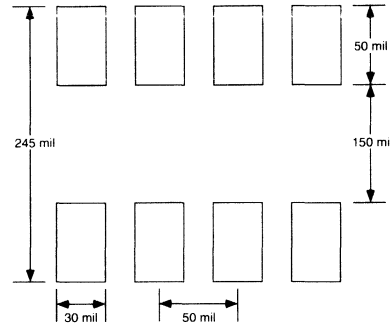
Multi-layer boards having a ground plane, wide traces near the pads, and large supply bus lines provide better thermal conductivity.

The "worst case" value of 160°C/W assumes no ground plane, minimum trace widths, and a FR4 material board.

Part II. Nominal Power Dissipation and Die Temperature

The MIC5200-xxBM at a 25°C ambient temperature will operate reliably at up to 625mW power dissipation when mounted in the "worst case" manner described above. At an ambient temperature of 55°C, the device may safely dissipate 440mW. These power levels are equivalent to a die temperature of 125°C, the recommended maximum temperature for non-military grade silicon integrated circuits.

For MIC5200-xxBS (SOT-223 package) heat sink characteristics, please refer to Micrel Application Hint 17, "P.C. Board Heat Sinking".



Minimum recommended board pad size, SO-8.

MIC5201

200mA Low Drop-out Voltage Regulator

Preliminary Information

General Description

The MIC5201 is an efficient linear voltage regulator with very low drop out voltage (typically 17mV at light loads and 200mV at 100mA), and very low ground current (1mA at 100mA output), offering better than 1% initial accuracy with a logic compatible ON/OFF switching input. Designed especially for hand-held battery powered devices, the MIC5201 is switched by a CMOS or TTL compatible logic signal. This ENABLE control may be tied directly to V_{IN} if unneeded. When disabled, power consumption drops nearly to zero. The ground current of the MIC5201 increases only slightly in dropout, further prolonging battery life. Key MIC5201 features include protection against reversed battery, current limiting, and over-temperature shutdown.

The MIC5201 is available in several fixed voltages and accuracy configurations. It features the same pinout as the LT1121 with better performance. Other options are available; contact Micrel for details.

Features

- High output voltage accuracy
- Variety of output voltages
- Guaranteed 200mA output
- Low quiescent current
- Low dropout voltage
- Extremely tight load and line regulation
- Very low temperature coefficient
- Current and thermal limiting
- Reverse-battery protection
- Zero OFF mode current
- Logic-controlled electronic enable
- Available in SO-8 and SOT-223 packages

Applications

- Cellular Telephones
- Laptop, Notebook, and Palmtop Computers
- Battery Powered Equipment
- PCMCIA V_{CC} and V_{PP} Regulation/Switching
- Bar Code Scanners
- SMPS Post-Regulator/ DC to DC Modules
- High Efficiency Linear Power Supplies

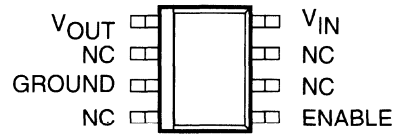
Ordering Information

Part Number	Volts	Accuracy	Temperature Range*	Package
MIC5201-3.0BM	3.0	1%	–40°C to +125°C	SO-8
MIC5201-3.3BM	3.3	1%	–40°C to +125°C	SO-8
MIC5201-4.8BM	4.85	1%	–40°C to +125°C	SO-8
MIC5201-5.0BM	5.0	1%	–40°C to +125°C	SO-8
MIC5201-3.0BS	3.0	1%	–40°C to +125°C	SOT-223
MIC5201-3.3BS	3.3	1%	–40°C to +125°C	SOT-223
MIC5201-4.8BS	4.85	1%	–40°C to +125°C	SOT-223
MIC5201-5.0BS	5.0	1%	–40°C to +125°C	SOT-223

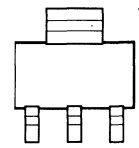
* *Junction Temperature*

Other voltages are available; contact Micrel for details.

Pin Configuration



MIC5201-xxBM

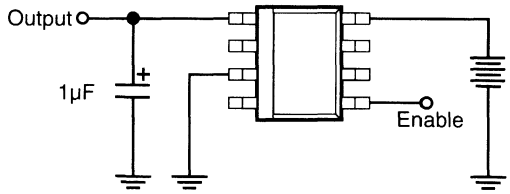


V_{IN} GND V_{OUT}

MIC5201-xxBS

Typical Application

MIC5201-3.3



ENABLE may be tied directly to V_{IN}

Absolute Maximum Ratings

Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Electrical specifications do not apply when operating the device beyond its specified **Operating Ratings.**

Power Dissipation	Internally Limited
Lead Temperature (Soldering, 5 seconds)	260°C
Operating Junction Temperature Range	–40°C to +125°C
Input Supply Voltage	–20V to +60V
ENABLE Input Voltage	–20V to +60V
ESD Rating	> 2000V

Recommended Operating Conditions

Input Voltage	2.5V to 26V
Operating Junction Temperature Range	–40°C to +125°C
ENABLE Input Voltage	0V to V_{IN}

Electrical Characteristics

Limits in standard typeface are for T_J = 25°C and limits in **boldface** apply over the junction temperature range of –40°C to +125°C. Unless otherwise specified, $V_{IN} = V_{OUT} + 1V$, I_L = 1mA, C_L = 3.3µF, and $V_{ENABLE} \geq 2.0V$

Symbol	Parameter	Conditions	Min	Typical	Max	Units
V_O	Output Voltage Accuracy	Variation from specified V_{OUT}	–1 **–2**		1 **2**	%
$\frac{\Delta V_O}{\Delta T}$	Output Voltage Temperature Coef.	(Note 2)		**20**	**100**	ppm/°C
$\frac{\Delta V_O}{V_{IN}}$	Line Regulation	$V_{IN} = V_{OUT}$ + 1 V to 26V		0.004	0.10 **0.40**	%
$\frac{\Delta V_O}{I_L}$	Load Regulation	I_L = 0.1mA to 200mA (Note 3)		0.04	0.16 **0.30**	%
$V_{IN} - V_O$	Dropout Voltage (Note 4)	I_L = 100µA I_L = 20mA I_L = 50mA I_L = 100mA I_L = 200mA		17 **75** 130 **160** 190 **240** 210 **350** 270 **400**		mV
I_{GND}	Quiescent Current	$V_{ENABLE} \leq 0.7V$ (Shutdown)		0.01		µA
I_{GND}	Ground Pin Current	$V_{ENABLE} \geq 2.0V$, I_L = 100µA I_L = 20mA I_L = 50mA I_L = 100mA I_L = 200mA		130 240 450 900 3.0		µA mA
PSRR	Ripple Rejection			70		dB
I_{GNDDO}	Ground Pin Current at Dropout	V_{IN} = 0.5V less than specified V_{OUT} I_L = 100µA (Note 5)		270	**330**	µA
I_{LIMIT}	Current Limit	V_{OUT} = 0V		**350**		mA
$\frac{\Delta V_O}{\Delta P_D}$	Thermal Regulation	(Note 6)		0.05		%/W
e_n	Output Noise			30		µV

ENABLE Input

V_{IL}	Input Voltage Level Logic Low Logic High	 OFF ON	 **2.0**		**0.7**	V
I_{IL} I_{IH}	ENABLE Input Current	$V_{IL} \leq 0.7V$ $V_{IH} \geq 2.0V$		0.01 15	 **50**	µA

Note 1: Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device outside of its rated operating conditions. The maximum allowable power dissipation is a function of the maximum junction temperature, $T_{J(MAX)}$, the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using: $P_{(MAX)} = (T_{J(MAX)} - T_A)\ \theta_{JA}$. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the regulator will go into thermal shutdown. The θ_{JC} of the MIC5201-xxBS is 15°C/W and θ_{JA} for the MIC5201BM is 160°C/W mounted on a PC board (see "Thermal Considerations" section for further details).

Note 2: Output voltage temperature coefficient is defined as the worst case voltage change divided by the total temperature range.

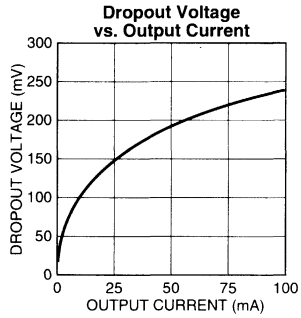
Note 3: Regulation is measured at constant junction temperature using low duty cycle pulse testing. Parts are tested for load regulation in the load range from 0.1mA to 200mA. Changes in output voltage due to heating effects are covered by the thermal regulation specification.

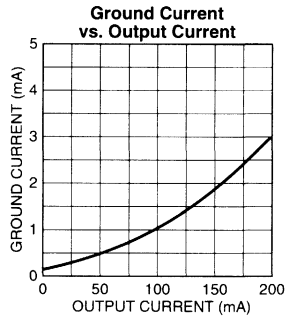
Note 4: Dropout Voltage is defined as the input to output differential at which the output voltage drops 2% below its nominal value measured at 1V differential.

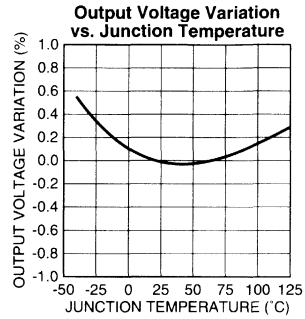
Note 5: Ground pin current is the regulator quiescent current plus pass transistor base current. The total current drawn from the supply is the sum of the load current plus the ground pin current.

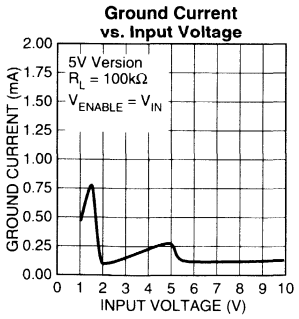
Note 6: Thermal regulation is defined as the change in output voltage at a time T after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for a 200mA load pulse at V_{IN} = 26V for T = 10ms.

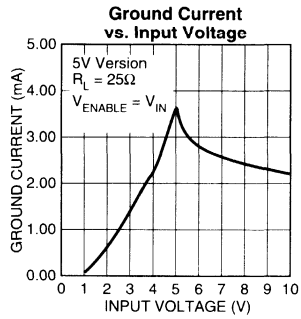
Typical Characteristics











Applications Information

External Capacitors

A 1μF capacitor is recommended between the MIC5201 output and ground to prevent oscillations due to instability. Larger values serve to improve the regulator's transient response. Most types of tantalum or aluminum electrolytics will be adequate; film types will work, but are costly and therefore not recommended. Many aluminum electrolytics have electrolytes that freeze at about –30°C, so solid tantalums are recommended for operation below –25°C. The important parameters of the capacitor are an effective series resistance of about 5Ω or less and a resonant frequency above 500kHz. The value of this capacitor may be increased without limit.

At lower values of output current, less output capacitance is required for output stability. The capacitor can be reduced to 0.47μF for current below 10mA or 0.33μF for currents below 1 mA. A 1μF capacitor should be placed from the MIC5201 input to ground if there is more than 10 inches of wire between the input and the AC filter capacitor or if a battery is used as the input.

The MIC5201 will remain stable and in regulation with no load in addition to the internal voltage divider, unlike many other voltage regulators. This is especially important in CMOS RAM keep-alive applications.

When used in dual supply systems where the regulator load is returned to a negative supply, the output voltage must be diode clamped to ground.

Thermal Considerations

Part I. Layout

The MIC5201-xxBM (8-pin surface mount package) has the following thermal characteristics when mounted on a single layer copper-clad printed circuit board.

PC Board Dielectric	θ_{JA}
FR4	160°C/W
Ceramic	120°C/W

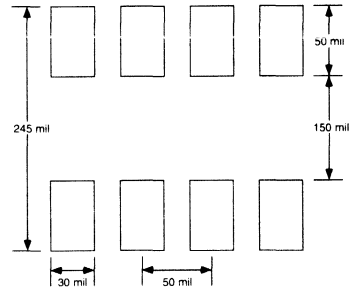
Multi-layer boards having a ground plane, wide traces near the pads, and large supply bus lines provide better thermal conductivity.

The "worst case" value of 160°C/W assumes no ground plane, minimum trace widths, and a FR4 material board.

Part II. Nominal Power Dissipation and Die Temperature

The MIC5201-xxBM at a 25°C ambient temperature will operate reliably at up to 625mW power dissipation when mounted in the "worst case" manner described above. At an ambient temperature of 55°C, the device may safely dissipate 440mW. These power levels are equivalent to a die temperature of 125°C, the recommended maximum temperature for non-military grade silicon integrated circuits.

For MIC5201-xxBS (SOT-223 package) heat sink characteristics, please refer to Micrel Application Hint 17, "P.C. Board Heat Sinking".



Minimum recommended board pad size, SO-8.

6

MIC5202

Dual Low Drop-out Voltage Regulator

Preliminary Information

General Description

The MIC5202 is a family of dual linear voltage regulators with very low drop out voltage (typically 17mV at light loads and 210mV at 100mA), and very low ground current (1mA at 100mA output–each section), offering better than 1% initial accuracy with a logic compatible ON/OFF switching input. Designed especially for hand-held battery powered devices, the MIC5202 is switched by a CMOS or TTL compatible logic signal. This ENABLE control may be tied directly to V_{IN} if unneeded. When disabled, power consumption drops nearly to zero. The ground current of the MIC5202 increases only slightly in dropout, further prolonging battery life. Key MIC5202 features include protection against reversed battery, current limiting, and over-temperature shutdown.

The MIC5202 is available in several fixed voltages. Other options, including different voltages in the same package (3.3V and 5.0V in one package, for example) and accuracy configurations are available; contact Micrel for details.

Features

- High output voltage accuracy
- Variety of output voltages
- Guaranteed 100mA output
- Low quiescent current
- Low dropout voltage
- Extremely tight load and line regulation
- Very low temperature coefficient
- Current and thermal limiting
- Reverse-battery protection
- Zero OFF mode current
- Logic-controlled electronic shutdown
- Available in SO-8 package

Applications

- Cellular Telephones
- Laptop, Notebook, and Palmtop Computers
- Battery Powered Equipment
- PCMCIA V_{CC} and V_{PP} Regulation/Switching
- Bar Code Scanners
- SMPS Post-Regulator/ DC to DC Modules
- High Efficiency Linear Power Supplies

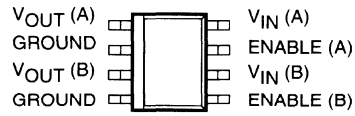
Ordering Information

Part Number	Volts	Accuracy	Temperature Range*	Package
MIC5202-3.0BM	3.0	1%	–40°C to +125°C	SO-8
MIC5202-3.3BM	3.3	1%	–40°C to +125°C	SO-8
MIC5202-4.5BM	4.5	1%	–40°C to +125°C	SO-8
MIC5202-4.7BM	4.75	1%	–40°C to +125°C	SO-8
MIC5202-5.0BM	5.0	1%	–40°C to +125°C	SO-8

* Junction Temperature

Other voltages are available; contact Micrel for details.

Pin Configuration

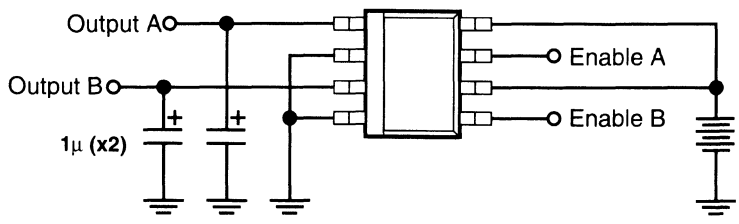


MIC5202-xxBM

Both GROUND pins must be tied to the same potential. V_{IN} (A) and V_{IN} (B) may run from separate supplies.

Typical Application

MIC5202-3.3



ENABLE pins may be tied directly to V_{IN}

Absolute Maximum Ratings

Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Electrical specifications do not apply when operating the device beyond its specified **Operating Ratings.**

Power Dissipation	Internally Limited
Lead Temperature (Soldering, 5 seconds)	260°C
Operating Junction Temperature Range	–40°C to +125°C
Input Supply Voltage	–20V to +60V
ENABLE Input Voltage	–20V to +60V
ESD Rating	> 2000V

Recommended Operating Conditions

Input Voltage	2.5V to 26V
Operating Junction Temperature Range	–40°C to +125°C
ENABLE Input Voltage	0V to V_{IN}

Electrical Characteristics

Limits in standard typeface are for T_J = 25°C and limits in **boldface** apply over the junction temperature range of –40°C to +125°C. Specifications are for each half of the (dual) MIC5202. Unless otherwise specified, $V_{IN} = V_{OUT} + 1V$, I_L = 1mA, C_L = 10µF, and $V_{CONTROL} \geq 2.0V$.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_O	Output Voltage	Variation from specified V_{OUT} Accuracy	–1 **–2**		1 **2**	%
$\frac{\Delta V_O}{\Delta T}$	Output Voltage Temperature Coef.	(Note 2)		**20**	**100**	ppm/°C
$\frac{\Delta V_O}{V_{IN}}$	Line Regulation	$V_{IN} = V_{OUT}$ + 1 V to 26V		0.004	0.10 **0.40**	%
$\frac{\Delta V_O}{I_L}$	Load Regulation	I_L = 0.1mA to 100mA (Note 3)		0.04	0.16 **0.30**	%
$V_{IN} - V_O$	Dropout Voltage (Note 4)	I_L = 100µA I_L = 20mA I_L = 30mA I_L = 50mA I_L = 100mA		17 **75** 130 **160** 150 **200** 190 **240** 210 **350**		mV
I_{GND}	Quiescent Current	$V_{CONTROL} \leq 0.7V$ (Shutdown)		0.01		µA
I_{GND}	Ground Pin Current	$V_{CONTROL} \geq 2.0V$, I_L = 100µA I_L = 20mA I_L = 30mA I_L = 50mA I_L = 100mA		130 240 300 450 900		µA
PSRR	Ripple Rejection			70		dB
I_{GNDDO}	Ground Pin Current at Dropout	V_{IN} = 0.5V less specified V_{OUT}, I_L = 100µA (Note 5)		270	**330**	µA
I_{LIMIT}	Current Limit	V_{OUT} = 0V		**350**		mA
$\frac{\Delta V_O}{\Delta P_D}$	Thermal Regulation	(Note 6)		0.05		%/W
e_n	Output Noise			30		µV

Control Input

V_{IL}	Input Voltage Level Logic Low Logic High	 OFF ON	 **2.0**		 **0.7**	V
I_{IL} I_{IH}	Control Input Current	$V_{IL} \leq 0.7V$ $V_{IH} \geq 2.0V$		0.01 15	 **50**	µA

Note 1: Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device outside of its rated operating conditions. The maximum allowable power dissipation is a function of the maximum junction temperature, $T_{J(MAX)}$ the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using: $P_{(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the regulator will go into thermal shutdown. The junction to ambient thermal resistance of the MIC5202BM is 160°C/W mounted on a PC board.

Note 2: Output voltage temperature coefficient is defined as the worst case voltage change divided by the total temperature range.

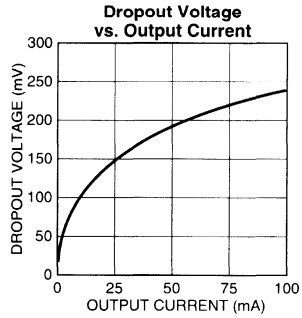
Note 3: Regulation is measured at constant junction temperature using low duty cycle pulse testing. Parts are tested for load regulation in the load range from 0.1mA to 100mA. Changes in output voltage due to heating effects are covered by the thermal regulation specification.

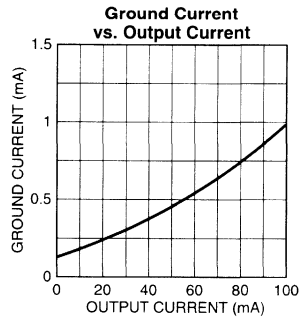
Note 4: Dropout Voltage is defined as the input to output differential at which the output voltage drops 2% below its nominal value measured at 1V differential.

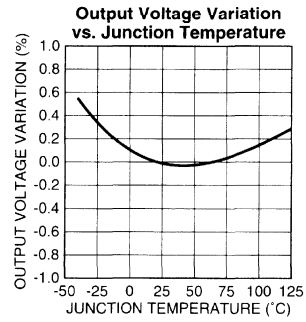
Note 5: Ground pin current is the regulator quiescent current plus pass transistor base current. The total current drawn from the supply is the sum of the load current plus the ground pin current.

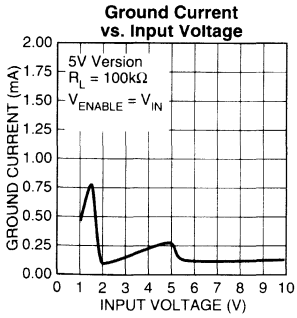
Note 6: Thermal regulation is defined as the change in output voltage at a time T after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for a 100mA load pulse at V_{IN} = 26V for T = 10ms, and is measured separately for each section.

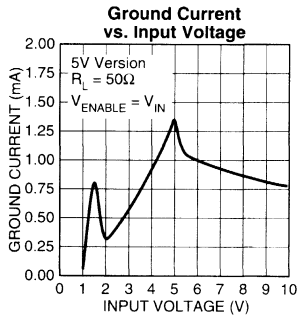
Typical Characteristics (Each half of the Dual MIC5202)











Applications Information

External Capacitors

A 1μF capacitor is recommended between the MIC5202 output and ground to prevent oscillations due to instability. Larger values serve to improve the regulator's transient response. Most types of tantalum or aluminum electrolytics will be adequate; film types will work, but are costly and therefore not recommended. Many aluminum electrolytics have electrolytes that freeze at about –30°C, so solid tantalums are recommended for operation below –25°C. The important parameters of the capacitor are an effective series resistance of about 5Ω or less and a resonant frequency above 500kHz. The value of this capacitor may be increased without limit.

At lower values of output current, less output capacitance is required for output stability. The capacitor can be reduced to 0.47μF for current below 10mA or 0.33μF for currents below 1 mA. A 1μF capacitor should be placed from the MIC5202 input to ground if there is more than 10 inches of wire between the input and the AC filter capacitor or if a battery is used as the supply.

General Notes

The MIC5202 will remain stable and in regulation with no load in addition to the internal voltage divider, unlike many other voltage regulators. This is especially important in CMOS RAM keep-alive applications. Thermal shutdown is independant on both halfs of the dual MIC5202, however an over-temperature condition on one half might affect the other. When used in dual supply systems where the regulator load is returned to a negative supply, the output voltage must be diode clamped to ground.

Both MIC5202 GROUND pins must be tied to the same ground potential. Isolation between the two halfs allows connecting the two V_{IN} pins to different supplies.

Thermal Considerations

Part I. Layout

The MIC5202-xxBM (8-pin surface mount package) has the following thermal characteristics when mounted on a single layer copper-clad printed circuit board.

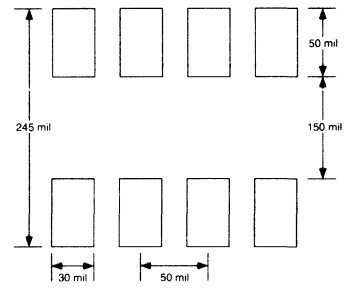
PC Board Dielectric	θ_{JA}
FR4	160°C/W
Ceramic	120°C/W

Multi-layer boards having a ground plane, wide traces near the pads, and large supply bus lines provide better thermal conductivity.

The "worst case" value of 160°C/W assumes no ground plane, minimum trace widths, and a FR4 material board.

Part II. Nominal Power Dissipation and Die Temperature

The MIC5202-xxBM at a 25°C ambient temperature will operate reliably at up to 625mW power dissipation when mounted in the "worst case" manner described above. At an ambient temperature of 55°C, the device may safely dissipate 440mW. These power levels are equivalent to a die temperature of 125°C, the recommended maximum temperature for non-military grade silicon integrated circuits.



Minimum recommended board pad size, SO-8.

Application Note 9

Design Considerations for 5V to 3.3V Pass Regulators

By Bob Wolbert

General Description

The rise of 3.3V logic and memory components in personal computer systems has created demand for 3.3V power supplies. Several options exist for the computer system designer. One of these options is to provide both 3.3V and 5.0V from the main system power supply and use a switch matrix for voltage selection (see Application Hint 15 for representative circuitry). Two drawbacks to this technique exist: (1) the extra 3.3V output costs money; and (2), at current levels above about 1A, the MOSFETs used in the 3.3V portion of the matrix require exceptionally low ON resistance to maintain output tolerance and are quite expensive. Another option uses the existing high current 5V supply and employs a low drop-out (LDO) linear regulator to provide 3.3V. This is a low cost option, requiring only short design work and little motherboard space. Linear regulators provide clean, accurate output and do not radiate RFI, so government certification is not jeopardized. They are fast starting, and may provide ON/OFF control and an error flag that indicates power system trouble. At low current levels, thermal considerations are not difficult; however, at currents of 3.5 to 5 amperes, the resulting heat may be troublesome. This note discusses the LDO option, including choosing between simple three terminal regulators and full-featured five terminal regulators, and provides formulas, calculations, and a selection of commercial heat sinks for powering 3.3V logic circuitry requiring up to 5 amps from a standard +5V supply. Additionally, a "trick" for reducing heat sink requirements by distributing power dissipation with a series resistor is discussed.

Why Choose Five Terminal Regulators?

What do the extra pins of the five pin linear regulators provide? After all, three terminal regulators give Input, Output, and Ground; what else is necessary? Five terminal devices allow the system designer to monitor power quality to the load and digitally switch the supply ON and OFF. Power quality is monitored by a flag output. When the output voltage is within a few percent of its desired value, the flag is high, indicating "Good". If the output drops, because of either low input voltage to the regulator or an over-current condition, the flag drops to signal a fault condition. A controller can monitor this output and make decisions regarding the system's readiness. For example, at initial power-up, the flag will instantaneously read high (if pulled up to an external supply), but as soon as the input supply to the regulator reaches about 2V, the flag pulls low. It stays low until the regulator output nears its desired value. With the MIC29150 family of low drop-out linear regulators, the flag rises when the output voltage reaches about 97% of the desired value. In a 3.3V system, the flag indicates "power good" with V_{OUT} = 3.2V.

Digital power control allows "sleep" mode operation and results in better energy efficiency. The ENABLE input of the MIC29150 family is TTL and 5V or 3.3V CMOS compatible. When this input is pulled above approximately 1.4V, the regulator is activated. A special feature of this regulator family is *zero power consumption* when inactive. Whenever the digital control input is low, all internal circuitry is biased OFF. (A tiny leakage current, measured in nanoamperes, may flow).

Three terminal regulators are used whenever ON/OFF control is not necessary and processing power is not available to use the flag output information. Three terminal regulators need only a single output filter capacitor so design effort is minimal.

Five terminal regulators provide all the functionality of three pin devices PLUS allow power supply quality monitoring and ON/OFF switching for "sleep" mode applications.

Thermal Design Considerations

Micrel low drop-out (LDO) regulators are very easy to use. Only one external filter capacitor is necessary for operation so electrical design effort is minimal. In many cases, thermal design is also quite simple, due to the low drop-out characteristic of Micrel's LDOs. Unlike other linear regulators, Micrel's LDOs operate with drop-out voltages of 300mV–often less. The resulting Voltage x Current power loss can be quite small with low to moderate output current. At higher currents, however, selecting the correct heat sink is an important chore. Power dissipation in a linear regulator is:

$$P_D = (V_{IN} - V_{OUT}) \bullet I_{OUT} + V_{IN} \bullet I_{GND}$$

Where: P_D = Power dissipation

V_{IN} = Input voltage applied to the regulator

V_{OUT} = Regulator output voltage

I_{OUT} = Regulator output current

I_{GND} = Regulator biasing currents

Proper design dictates use of worst case values for all parameters. Worst case V_{IN} is high supply; in this case, 5V + 5%, or 5.25V. Worst case V_{OUT} for thermal considerations is minimum, or 3.3V – 2% = 3.234V.[1] I_{OUT} is taken at its highest steady-state value. The ground current value comes from the device's datasheet, from the graph of I_{GND} vs. I_{OUT}. Armed with this information, we calculate the thermal resistance (θ_{SA}) required of the heat sink using the following formula:

$$\theta_{SA} = \frac{T_J - T_A}{P_D} - (\theta_{JC} + \theta_{CS})$$

Assuming a Micrel LDO with a maximum die temperature of 125°C in a TO-220 package with a θ_{JA} of 2°C/W and a mounting resistance (θ_{CS}) of 1°C/W[2], operating at an ambient temperature of 50°C, we get

$$\theta_{SA} = \frac{125 - 50°C}{10.5W} - (2 + 1°C/W) = \mathbf{4.1\ °C/W}$$

Performing similar calculations for 1.25A, 1.5A, 2.0A, 2.5A, 3.0A, 4.0A, and 5.0A gives the results shown in Table 1.

Regulator	I_{OUT}	P_D (W)	θ_{SA}(°C/W)
MIC29150	1.25A	2.6	25
MIC29150	1.5A	3.2	21
MIC29300	2.0A	4.2	15
MIC29300	2.5A	5.2	11
MIC29300	3.0A	6.3	8.8
MIC29500	4.0A	8.4	5.9
MIC29500	5.0A	10.5	4.1

Table 1. Micrel LDO power dissipation and heat sink requirements for various 3.3V current levels.

Table 2 shows the effect maximum ambient temperature has on heat sink thermal properties. Lower thermal resistances require physically larger heat sinks. The table clearly shows cooler running systems need smaller heat sinks, as common sense suggests.

Heat Sink Selection

With this information we may specify a heat sink. The worst case is still air (natural convection). The heat sink should be mounted so that at least 0.25 inches (about 6mm) of separation exists between the sides and top of the sink and other components or the system case. Thermal properties are maximized when the heat sink is mounted so that natural vertical motion of warm air is directed along the long axis of the sink fins.

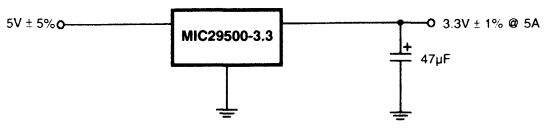


Figure 2. Using a Micrel LDO is very simple. Only an output filter capacitor is necessary. Here, 3.3V at 5A is produced from a nominal 5V input.

If we are fortunate enough to have some forced airflow, reductions in heat sink cost and space are possible by characterizing air speed–even a slow airstream significantly assists cooling. As with natural convection, a small gap allowing the airstream to pass is necessary. Fins should be located to maximize airflow along them. Orientation with respect to vertical is not important, as the airflow dominates.

Output	Ambient Temperature		
	40°C	50°C	60°C
1.5A	24°C/W	21°C/W	17°C/W
5A	5.1°C/W	4.1°C/W	3.2°C/W

Table 2. Ambient temperature affects heat sink requirements

As an example, we will select heat sinks for 1.5A and 5A outputs. We consider four airflow cases: natural convection, 200 feet/minute (1m/sec), 300 feet/minute (1.5m/sec), and 400 feet/minute (2m/sec). Table 3 shows heat sinks for these air velocities; note the rapid reduction in size and weight (fin thickness) when forced air is available. Consulting manufacturer's charts,[3,4] we see a variety of sinks are made that are suitable for our application. At 5A (10.5W worst case package dissipation) and natural convection, sinks are sizable, but at 1.5A (3.2W worst case package dissipation) and 400 feet/minute airflow, modest heat sinks are adequate.

The heat sink required for 5A applications in still air is massive and expensive. There is a better way to manage heat problems: we take advantage of the very low drop out voltage characteristic of Micrel's Super ßeta PNP™ regulators and dissipate some power externally in a series resistance.[5] By distributing the voltage drop between this low cost resistor and the regulator, we distribute the heating, and reduce the size of the regulator heat sink. Knowing the worst case voltages in the system and the peak current requirements, we select a resistor that drops a portion of the excess voltage without sacrificing performance. The maximum value of the resistor is calculated from:

$$R_{MAX} = \frac{V_{IN\ MIN} - (V_{OUT\ MAX} + V_{DO})}{I_{OUT\ PEAK} + I_{GND}}$$

Where: $V_{IN\ MIN}$ is low supply (5V – 5% = 4.75V)

$V_{OUT\ MAX}$ is the maximum output voltage across the full temperature range (3.3V + 2% = 3.366V)

V_{DO} is the worst case dropout voltage across the full temperature range (600mV)

$I_{OUT\ PEAK}$ is the maximum 3.3V load current

I_{GND} is the regulator ground current.

For our 5A output example:

$$R_{MAX} = \frac{4.75 - (3.366 + 0.6)\ V}{5 + 0.08\ A} = \frac{0.784V}{5.08A} = 0.154\Omega$$

The power drop across this resistor is

$$P_{D\ RES} = (I_{OUT\ PEAK} + I_{GND})^2 \bullet R$$

or 4.0W. This subtracts directly from the 10.5W of regulator power dissipation that occurs without the resistor, reducing regulator heat generation to 6.5W.

$$P_{D(Regulator)} = P_{D(R\ =\ 0\Omega)} - P_{D\ RES}$$

Considering 5% resistor tolerances and standard values leads us to a 0.15Ω ± 5% resistor. This produces a nominal power savings of 3.9W. With worst-case tolerances, the regulator power dissipation drops to 6.8W maximum. This heat drop reduces our heat sinking requirements for the MIC29500 significantly. We can use a smaller heat sink with a larger thermal resistance. Now, a heat sink with 8.3°C/W thermal characteristics is suitable–nearly a factor of 2 better than without the resistor. Table 4 lists representative heat sinks meeting these conditions.

For the 1.5A output application using the MIC29150, we calculate a maximum R of 0.512Ω. Using R = 0.51Ω, savings of at least 1.1W are achieved, dropping power dissipation to only 2.0W–a heat sink probably is not required. This circuit is shown in Figure 4.

Another option exists for designers of lower current systems. The MIC29150 and MIC29300 regulators are available in the surface mount derivative of the TO-220 package, the TO-263, which is soldered directly to the PC board. No separate heat sink is necessary, as copper area on the board acts as the heat exchanger. For further information, refer to Micrel's Application Hint 17, "P.C. Board Heat Sinking".

Output Current		
Airflow	**1.5A**	**5A**
400 ft./min. (2m/sec)	Thermalloy 6049PB	Thermalloy 6232 Thermalloy 6034 Thermalloy 6391B
300 ft./min. (1.5m/sec)		AAVID 504222B AAVID 563202B AAVID 593202B AAVID 534302B Thermalloy 7021B Thermalloy 6032 Thermalloy 6234B
200 ft./min. (1m/sec)	AAVID 577002 Thermalloy 6043PB Thermalloy 6045B	AAVID 508122 AAVID 552022 AAVID 533302 Thermalloy 7025B Thermalloy 7024B Thermalloy 7022B Thermalloy 6101B
Natural Convection (no forced airflow)	AAVID 576000 AAVID 574802 592502 579302 Thermalloy 6238B Thermalloy 6038 Thermalloy 7038	AAVID 533602B (vertical) AAVID 519922B (horizontal) AAVID 532802B (vertical) Thermalloy 6299B (vertical) Thermalloy 7023 (horizontal)

Table 3. Commercial heat sinks for 1.5A and 5.0A applications

Airflow	Heat Sink Model
400 ft./min. (2m/sec)	AAVID 530700 AAVID 574802 Thermalloy 6110 Thermalloy 7137, 7140 Thermalloy 7128
300 ft./min. (1.5m/sec)	AAVID 57302 AAVID 530600 AAVID 577202 AAVID 576802 Thermalloy 6025 Thermalloy 6109 Thermalloy 6022
200 ft./min. (1m/sec)	AAVID 575102 AAVID 574902 AAVID 523002 AAVID 504102 Thermalloy 6225 Thermalloy 6070 Thermalloy 6030 Thermalloy 6230 Thermalloy 6021, 6221 Thermalloy 7136, 7138
Natural Convection (no forced airflow)	AAVID 563202 AAVID 593202 AAVID 534302 Thermalloy 6232 Thermalloy 6032 Thermalloy 6034 Thermalloy 6234

Table 4. Representative commercial heat sinks for the 5.0A output example using a series dropping resistor. Assumptions: T_A = 50°C, R = 0.15Ω ±5%, $I_{OUT\ MAX}$ = 5.0A, θ_{JC} = 2°C/W, θ_{CS} = 1°C/W, resulting in a required θ_{SA} = 8.0°C/W.

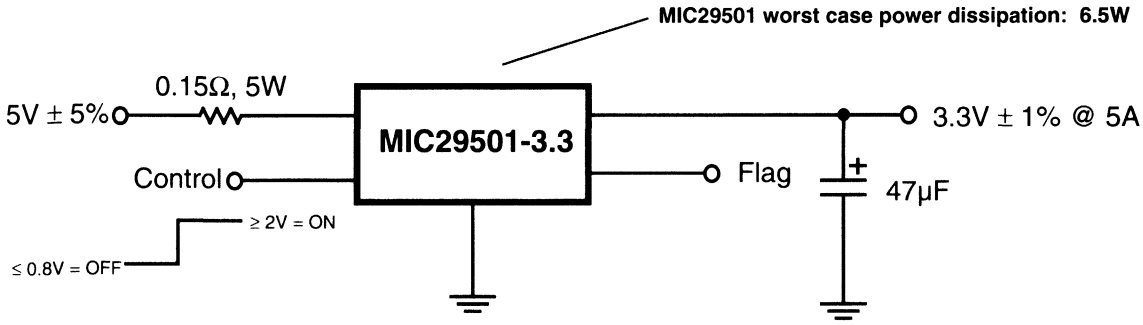


Figure 3. Producing 3.3V at 5A with minimal heat sink requirements. A 0.15Ω resistor dissipates excess power, reducing regulator heat generation. The resistor needs no heat sink.

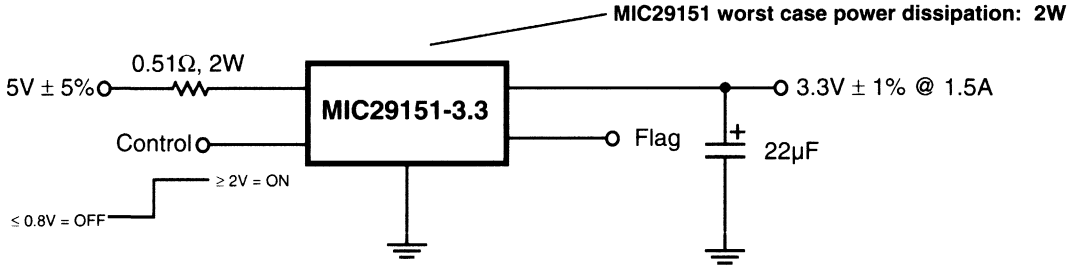


Figure 4. The MIC29151-3.3 produces 1.5A at 3.3V. No heat sink is necessary in most situations when the external power sharing resistor is employed.

6

Notes

NOTE 1: The MIC29150, MIC29300, MIC29500, and MIC29750 LDO regulator family feature trimmed outputs guaranteed to ±1% under standard conditions. Across the full temperature range, with load and input voltage variations, the device output voltage varies less than 2% worst case.

NOTE 2: The mounting tab of the MIC29150 family regulators is grounded. The estimated value of θ_{CS} assumes no electrical insulation between mounting tab and heat sink.

NOTE 3: AAVID Engineering, Inc., One Kool Path, Laconia, NH 03247. (603) 528-3400.

NOTE 4: Thermalloy Inc., P.O. Box 810839, Dallas, TX 75381. (214) 243-4321.

NOTE 5: Super ßeta PNP™ is a registered trademark of Micrel, Inc.

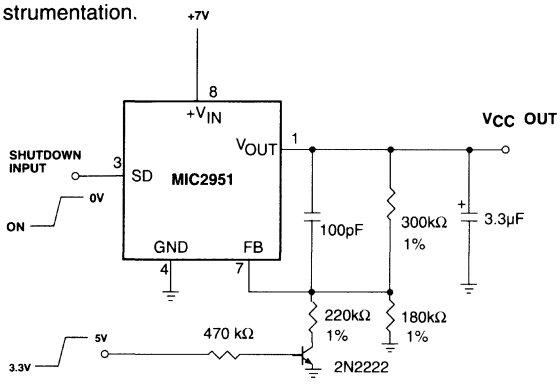
Application Hint 7

Using Low Current LDO Regulators

by Bob Wolbert

General Description

The MIC2951 brings the benefits of linear regulation to surface mountable packaging. High accuracy, high efficiency, very low ripple, and excellent protective features are combined into a useful device for laptop/notebook computers, communications equipment, and battery operated instrumentation.



MIC2951 Configured as a selectable 3.3V or 5.0V output regulator.

Features

- High accuracy +5V or adjustable output voltage
- Extremely small size; up to 150mA output current
- Low dropout voltage and quiescent curent
- Thermal and over-current protection
- Error flag warns of output dropout
- Logic-controlled electronic shutdown

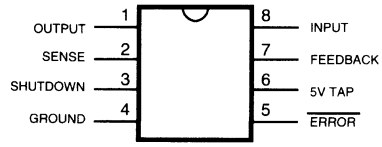
MIC Versus LP Benefits

- Lower dropout voltage
- 150mA output current vs. 100mA
- One-sixth the ground current
- Reverse battery protection for load
- Survives automotive "Load Dump" transient (60V)

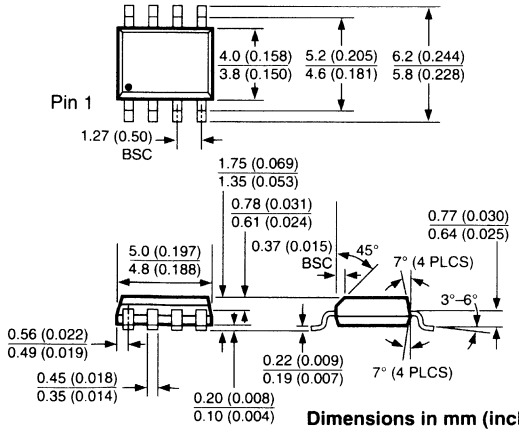
Ordering Information

Part Number	Temperature Range	Package	Accuracy
LP2951-02BM	–40°C to + 85°C	8-Pin SOIC	0.5%
LP2951-03BM	–40°C to + 85°C	8-Pin SOIC	1.0%
MIC2951-02BM	–40°C to + 85°C	8-Pin SOIC	0.5%
MIC2951-03BM	–40°C to + 85°C	8-Pin SOIC	1.0%

Pin Configuration



Package Dimensions



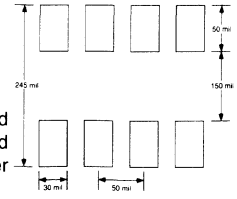
Dimensions in mm (inch)

Thermal Considerations

Part I. Layout

The MIC2951-02/03BM (8-pin surface mount package) has the following thermal characteristics when mounted on a single layer copper-clad printed circuit board.

PC Board Dielectric	θ_{JA}
FR4	160°C/W
Ceramic	120°C/W



Minimum recommended board pad size

Multi-layer boards having a ground plane, wide traces near the pads, and large supply bus lines provide better thermal conductivity.

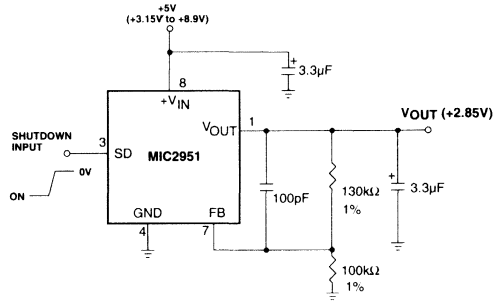
The "worst case" value of 160°C/W assumes no ground plane, minimum trace widths, and a FR4 material board.

Part II. Nominal Power Dissipation and Die Temperature

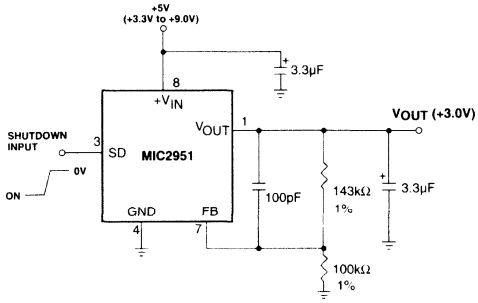
The MIC2951-02/-03BM at a 25°C ambient temperature will operate reliably at up to 625mW power dissipation when mounted in the "worst case" manner described above. At an ambient temperature of 55°C, the device may safely dissipate 440mW. These power levels are equivalent to a die temperature of 125°C, the recommended maximum temperature for non-military grade silicon integrated circuits.

Typical Applications

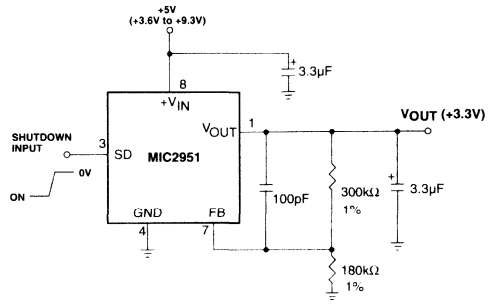
MIC2951-02/-03BM common voltage applications. Calculations assume 100mA of output current, 25°C ambient temperature, 100% duty cycle, and 160°C/W mounting. The Shutdown Input may be left floating if it is not used.



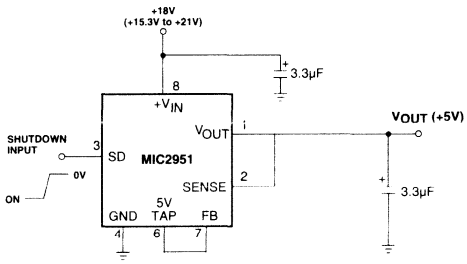
MIC2951 +2.85V Regulator



MIC2951 +3.0V Regulator

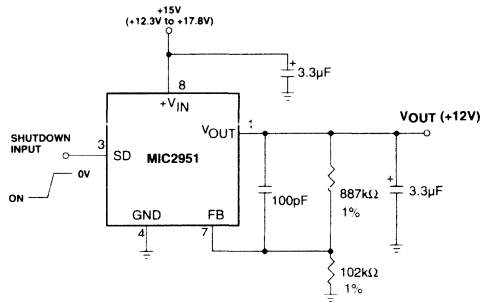


MIC2951 +3.3V Regulator

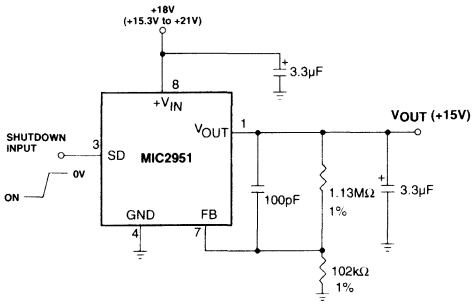


(Note: no external resistors are necessary)

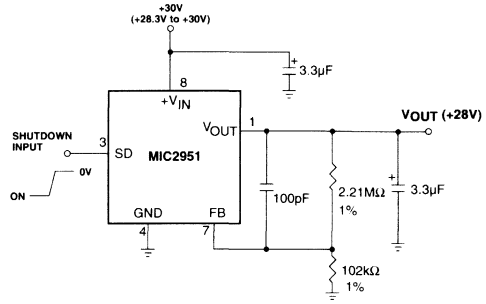
MIC2951 +5.0V Regulator



MIC2951 +12.0V Regulator



MIC2951 +15.0V



MIC2951 +28.0V Regulator

6

Application Hint 17

Calculating P.C. Board Heat Sink Area For Surface Mount Packages

By Bob Wolbert

General Description

System designers increasingly face the restriction of using all surface-mounted components in their new designs; even including the power components. Through-hole components can dissipate excess heat with clip-on or bolt-on heat sinks keeping things cool. Surface mounted components do not have this flexibility and rely on the conductive traces or pads on the printed circuit board for heat transfer. This hint addresses the question "How much PC board pad area does my design require?"

We will determine if a Micrel surface mount low dropout linear regulator may operate using only a PC board pad as its heat sink. We start with the circuit requirements.

System Requirements:

V_{OUT} = 5.0V
$V_{IN\ (MAX)}$ = 9.0V
$V_{IN\ (MIN)}$ = 5.6V
I_{OUT} = 700mA
Duty cycle = 100%
T_A = 50°C

This leads us to choose the 750mA MIC2937A-5.0BU voltage regulator, which has these characteristics:

V_{OUT} = 5V ± 2% (worst case over temperature)
$T_{J\ MAX}$ = 125°C
θ_{JC} of the TO-263 = 3°C/W
θ_{CS} ≈ 0°C/W (soldered directly to board)

Preliminary Calculations

$V_{OUT\ (MIN)}$ = 5V – 2% = 4.9V

$P_D = (V_{IN\ (MAX)} - V_{OUT\ (MIN)}) \times I_{OUT} + (V_{IN\ (MAX)} \times I_{GND})$
$= [9V - 4.9V] \times 700mA + (9V \times 15mA) = 3W$

Maximum temperature rise, $\Delta T = T_{J(MAX)} - T_A$
$= 125°C - 50°C = 75°C$

Thermal resistance requirement, θ_{JA} (worst case):

$$\frac{\Delta T}{P_D} = \frac{75°C}{3.0W} = 25°C/W$$

Heat sink thermal resistance, $\theta_{SA} = \theta_{JA} - (\theta_{JC} + \theta_{CS})$
$\theta_{SA} = 25 - (3 + 0) =$ **22°C/W (max)**

Heat sink physical size determination

Figure 1 shows the total area of a round or square pad, centered on the device. The solid trace represents the area of a square, single sided, horizontal, solder masked, copper PC board trace heat sink, measured in square millimeters. No airflow is assumed. The dashed line shows a heat sink covered in black oil-based paint and with 1.3m/sec (250 feet per minute) airflow. This approaches a "best case" pad heat sink.

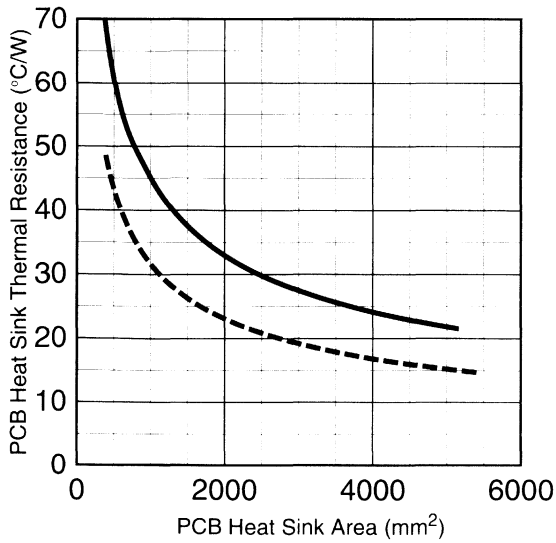


Figure 1. Graph to determine PC board area for a given thermal resistance. See text for discussion of the two curves.

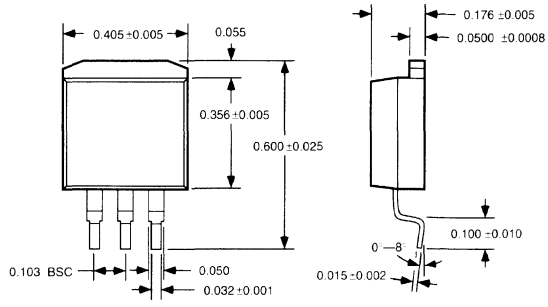


Figure 2. The TO-263 "U" Package. Derived from the popular TO-220 power package, the TO-263 has excellent thermal properties for a surface mount package.

Conservative design dictates using the solid trace data, which indicates a pad size of 5000 mm^2 is needed. This is a pad 71mm by 71mm (2.8 inches per side).

Example 2, SO-8 and SOT-223 package.

Given the following requirements, determine the safe heat sink pad area.

V_{OUT} = 5.0V
$V_{IN\ (MAX)}$ = 14V
$V_{IN\ (MIN)}$ = 5.6V
I_{OUT} = 150mA
Duty cycle = 100%
T_A = 50°C

Your board production facility prefers handling the dual-in-line SO-8 packages whenever possible. Is the SO-8 up to this task? Choosing the MIC2951-03BM, we get these characteristics:

$T_{J\ MAX}$ = 125°C
θ_{JC} of the SO-8 ≈ 100°C/W

SO-8 Calculations:

$P_D = [14V - 5V] \times 150mA + (14V \times 8mA) =$ **1.46W**

Temperature rise = 125°C – 50°C = **75°C**

Thermal resistance requirement, θ_{JA} (worst case):

$\frac{\Delta T}{P_D} = \frac{75°C}{1.46W} =$ **51.3°C/W**

Heat sink θ_{SA} = 51 – 100 = **–49 °C/W (max)**

Which obviously presents a problem: without refrigeration, the SO-8 is not suitable for this application. Consider the MIC5201-5.0BS in a SOT-223 package. This package is smaller than the SO-8, but its three terminals are designed for much better thermal flow. Choosing the MIC5201-3.3BS, we get these characteristics:

$T_{J\ MAX}$ = 125°C
θ_{JC} of the SOT-223 = 15°C/W
θ_{CS} = 0 °C/W (soldered directly to board)

SOT-223 Calculations:

$P_D = [14V - 4.9V] \times 150mA + (14V \times 1.5mA) =$ **1.4W**

Temperature rise = 125°C – 50°C = **75°C**

Thermal resistance requirement, θ_{JA} (worst case):

$\frac{\Delta T}{P_D} = \frac{75°C}{1.4W} =$ **54°C/W**

Heat sink θ_{SA} = 54 – 15 = **39°C/W (max)**

Board Area

Referring to Figure 1, a pad of 1400mm^2 (a square pad 1.5 inches per side) provides the required thermal characteristics.

Conclusion:

These formulae are provided as a general guide to thermal characteristics for surface mounted power components. Many estimations and generalizations were made; your system will vary. Please use this information as a rough approximation of board area required and fully evaluate the thermal properties of each board you design to confirm the validity of the equations.

6

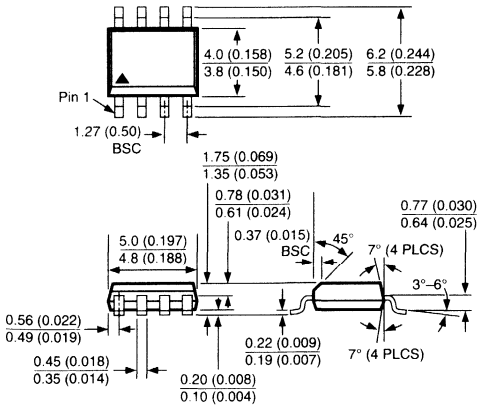


Figure 2. SO-8 Package. The SO-8 is small and very popular, but is far from ideal thermally.

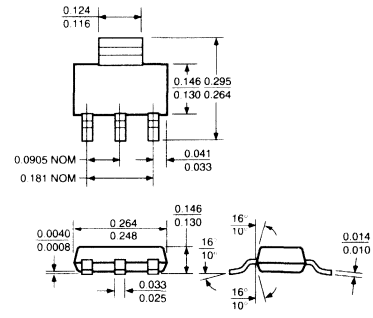


Figure 3. SOT-223 Package. Smaller than the popular SO-8, the SOT-223 has significantly better thermal characteristics.

Application Hint 18

Powering Intel™ P24 Microprocessors From +5V Supplies

By Bob Wolbert

General Description

The Intel™ P24c and P24c "OverDrive™" microprocessors are upgrades to the popular 486 microprocessor and share the same basic pinout.[1] A computer motherboard may be designed that accepts either processor, allowing the end user to initially use the lower cost 486 and later upgrade to the P24 by simply replacing ICs. There is a catch: the P24 operates from a 3.3V supply[2]. Pin S4 on the P24, VOLDET (voltage detect), is grounded to indicate the 3.3V processor is installed. This pin is not connected on 486 processors. Using this indicator, we can design a power control system that insures the proper voltage is applied to the processor.

This note describes a circuit that reads VOLDET from a P24-series processor and automatically determines whether to supply 5V or 3.3V. It operates from a single +5V ± 5% power supply and produces 3.3V output with a low drop-out linear regulator.

Circuit Discussion

Our goal is to provide the proper supply voltage to the microprocessor. We begin by determining what is the proper voltage. Intel has assigned P24 pin S4 to "VOLDET". This pin position, unassigned on the 486, is internally bonded to ground on the P24. A pull-up resistor connected from VOLDET to a system supply will allow differentiation between the grounded P24 and the open-circuited 486.

Our next consideration is to provide switched +5V from the main supply when a 486 is used. A low ON resistance switch will work. Micrel's MIC5014 high side MOSFET driver and a medium sized N-channel power MOSFET is ideal.

Now, we must produce a clean 3.3V source. The Intel P24c requires up to 1.25A at 3.3V. The Intel P24c OverDrive™ needs up to 3A. The Micrel MIC29150-3.3 is easily supplies the P24c, and the MIC29300 is perfect for suppling the P24c OverDrive™.

Finally, we put the blocks together and iron out interfacing. Figure 1 shows the power system block diagram.

Details

The schematic diagram for the power control block appears as Figure 2. With a 486 processor installed, the pull-up resistor, R1, pulls the MIC5014 input pin high, enabling the MOSFET driver. An internal charge pump voltage multiplier charges the power MOSFET (Q1) gate and supplies +5V V_{CC} to the processor. Voltage to the processor is V_{CC} minus a voltage drop determined by processor supply current times MOSFET ON resistance. The MOSFET size is determined by the maximum allowable voltage drop:

$$R_{MOSFET\ ON} = (V_{CC\ (S)\ MIN} - V_{CC\ (P)\ MIN}) / I_{CC}$$

Where: $V_{CC\ (S)\ MIN}$ is the minimum supply voltage from the power source

$V_{CC\ (P)\ MIN}$ is the minimum operating voltage for the processor

I_{CC} is the peak processor operating current

Assuming a 5V ±5% supply and a 486 rated for ±10% supply tolerance, the MOSFET ON resistance is:

$$R_{MOSFET} = (4.75 - 4.50) / I_{CC} = 0.25V / I_{CC}$$

Or 250 milliohms for a 1A load. A MOSFET with 0.25Ω or lower ON resistance will work.

Providing 3.3V from a nominal 5V supply is an easy matter using Micrel's low drop out linear regulators. These regulators need only one external component for operation, an output filter capacitor. Micrel's Super ßeta PNP™ LDOs are ideal for this application for other reasons as well. Unlike other regulators, Micrel's LDOs operate with drop-out voltages of 300mV–often less. This is important when we con-

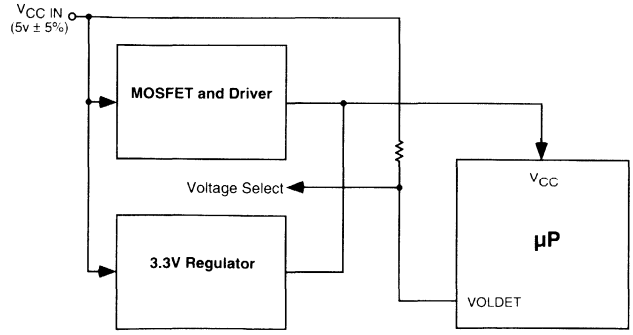


Figure 1. Block diagram for an auto-select voltage block for powering a computer motherboard that uses either 486 or P24c microprocessors. VOLDET signals the MOSFET and Driver block and the 3.3V Regulator block whether the 5V 486 or the 3.3V P24 is installed. The end user can upgrade his processor without worrying about supply voltage jumpers.

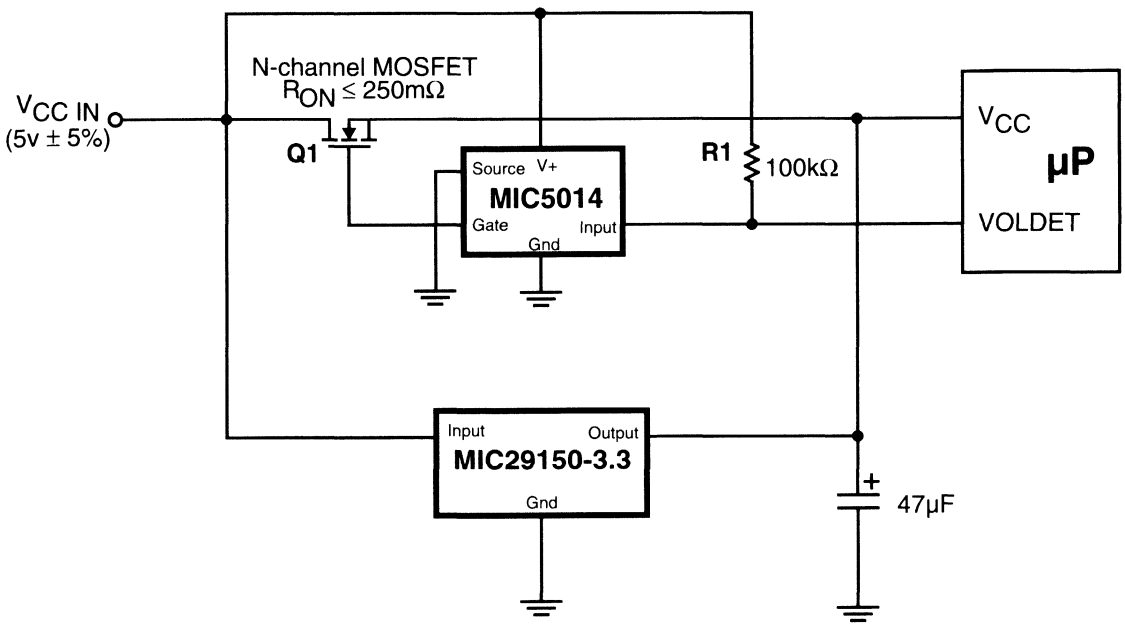


Figure 2. Complete schematic for the automatic voltage selection switch using the P24c VOLDET pin.

6

sider worst case tolerances: The "5V" supply can be as low as 4.75V and still be in-specification. The MIC29150-3.3 output may be as high as 3.366V under worst case conditions. This gives us a worst case available drop out voltage of only 1.384V (4.75V – 3.366V) . This is well within the 300mV typical performance of Micrel's LDOs as well as comfortably within the 600mV guaranteed maximum (over the full operating temperature range) specification. No NPN-pass element linear regulator can approach this performance. Additionally, Micrel LDOs feature "reverse battery" protection. This is like an ideal diode in series with the regulator that prevents reverse current flow caused either by a negative input voltage *or a higher voltage present on the regulator output.* This feature lets us connect the 3.3V LDO directly in parallel with the 5V switch to the processor V_{CC}. If the 5V supply is disabled, the LDO will source 3.3V. When the 5V supply is enabled, it will reverse bias the "diode" in the LDO output and effectively shut off the regulator. This means a simple three terminal LDO can be employed.

If other output voltages are required, Micrel's adjustable MIC29152 and MIC29302 are available and allow the designer to select any output voltage from 1.24V to the maximum rating of the device. Please refer to Application Hint 19 for further discussion of adjustable regulator applications.

At the 1.25A P24c level, thermal considerations are not difficult; however at the 3A level of the P24c OverDrive™, proper heat sinking is essential. For full details on heat sinking Micrel LDOs in this application, refer to Micrel Application Note 9, "Design Considerations for 5V to 3.3V Pass Regulators".

Notes

NOTE 1: Intel™ and OverDrive™ are trademarks of Intel Corp.

NOTE 2: The P24c accepts logic inputs as high as 5.3V when operating in a mixed-V_{CC} environment.

Application Hint 19

Powering IBM™ "Blue Lightning" Microprocessors From +5V Supplies

By Bob Wolbert

General Description

The IBM™ "Blue Lightning™" microprocessor is a 486-type processor built on a proprietary IBM process and uses a nominal 3.60V power supply.[1] Some versions operate at 3.3V, while higher performance devices require 3.6V, 3.8V, and even 4.1V. With its internal clock tripling circuitry, they dissipate up to a maximum of 3.6W, drawing about 1A. This power supply voltage creates a problem with PC motherboard manufacturers because a 3.3V to 4.1V variable supply is not available from standard computer power supplies. Micrel's MIC29152BU, in a surface mount TO-263 package, will power any version of the Blue Lightning from a standard 5V supply. This hint provides the circuit and thermal design for this application.

Circuit and Thermal Calculations

If the Blue Lightning version you use employs either a 3.3V or 3.6V power supply, Micrel offers a three terminal MIC29150 regulator that will simplify your design. Figure 1 shows the schematic diagram of the 3.3V or 3.6V power supply: only one external component is necessary for operation, an output filter capacitor. If the higher performance Blue Lightning processor is contemplated, or rapid production changes between versions using the same motherboard design is expected, the MIC29152 adjustable regulator is preferred. Figure 2 shows the schematic diagram of this flexible supply. Two resistors determine the output voltage. Since the layout remains the same, the production line can rapidly accommodate processor changes (and the required supply voltage changes) by simply changing one of the two resistors. Table 1 shows resistor values for the common processor supply voltages. For voltage requirements not listed, the formula for resistor ratio is:

$$\frac{V_O}{1.235} - 1 = \frac{R1}{R2}$$

The pinout of the three terminal MIC29150 and the center three pins of the MIC29152 is the same, with slightly different lead spacing. This means a single motherboard layout is possible that allows *both* the 3-pin fixed and 5-pin adjustable versions. Micrel's Super ßeta PNP™ LDOs are ideal for this application for other reasons as well.[2] Unlike other regulators, Micrel's LDOs operate with drop-out voltages of 300mV–often less. This is important when we consider worst case tolerances: The "5V" supply can be as low as 4.75V and still be in-specification. The MIC29150-3.3 output may be as high as 3.672V under worst case conditions. This gives us a worst case available drop out voltage of only 1.078V (4.75V – 3.672V) . This is well within the 300mV typical performance of Micrel's LDOs as well as comfortably within the 600mV guaranteed maximum (over the full operating temperature range) specification. No NPN-pass element linear regulator can approach this performance. Additionally, Micrel LDOs feature "reverse battery" protection.

Our thermal calculations are conservative and assume a worst case current of 1.0A at 3.67V (3.6V + 2%). Worst case drop out available is 1.08V (4.75V – 3.67V), which is well above the 0.60V guaranteed level of the MIC29150-3.6, so we have a fine match. Using the formula for power dissipation:

$$P_D = (V_{IN\,MAX} - V_{OUT\,MIN}) \times I_{OUT\,MAX} + V_{IN\,MAX} \times I_{GND}$$

the worst case power dissipation operating from a 5V ± 5% supply is:

$$P_D = (5.25V - 3.53V) \times 1.0A + (5.25V \times 10mA)$$

$$= \mathbf{1.77W}$$

What size of heat sink, if any, is necessary? The thermal resistance of a heat sink is:

$$\theta_{SA} = \frac{T_J - T_A}{P_D} - (\theta_{JC} + \theta_{CS})$$

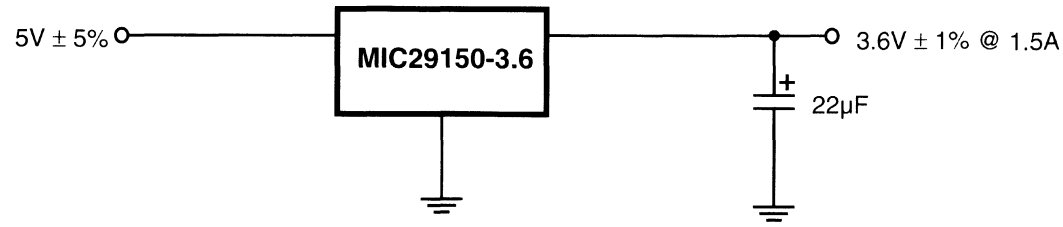
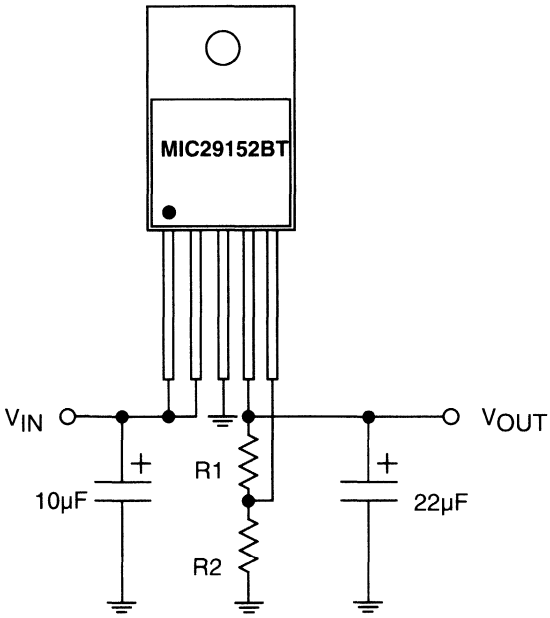


Figure 1. The MIC29150-3.6BU powers the IBM™ "Blue Lightning" from a nominal 5V supply without requiring any heat sinking other than the P.C. board mounting pad itself.



$$V_{OUT} = 1.235V \times [1 + (R1 / R2)]$$

Figure 2. MIC29152 Adjustable regulator circuit for use with Blue Lightning. Refer to Table 1 for resistor values.

Voltage Required	R1	R2
3.3V*	158k	95.3k
3.6V†	158k	82.5k
3.8V	158k	76.1k
4.1V	158k	68.1k

* The MIC29150-3.3 is a three terminal replacement if production-time voltage selection is not necessary.

† The MIC29150-3.6 is a three terminal replacement if production-time voltage selection is not necessary.

Table 1. Resistor values for Figure 1 calculated for common Blue Lightning operating voltages.

Assuming a θ_{JC} of 2°C/W, a θ_{CS} of 0.5°C/W, (the surface mount TO-263 is soldered directly to the PC board heat sink) and an ambient temperature, T_A, of 50°C, the maximum allowable heat sink thermal resistance is:

$$\theta_{SA} = \frac{125°C - 50°C}{1.8W} - (2°C/W + 0.5°C/W) = \mathbf{39°C/W}$$

Referring to Application Hint 17, we see that a square P.C. board pad of 40mm by 40mm (1.6 inches per side) is adequate. No external series dropping resistor is necessary for power sharing as this design is conservative. This pad is shown in Figure 3.

The through-hole MIC29150-3.6BT in a TO-220 package does not require a heat sink.

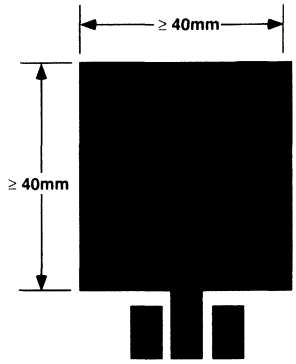


Figure 3. Suitable P.C. board heat sink for the MIC29150 powering "Blue Lightning".

Conclusion

The IBM "Blue Lightning" microprocessor operates from a nominal 3.6V supply[3], which can be obtained from a surface mount MIC29150-3.6BU without any heat sink other than the P.C. board itself. The entire schematic consists of only two components, the regulator and a filter capacitor, and is shown in Figure 1. At the 1A Blue Lightning current level, thermal considerations are not difficult and a P.C. board heat sink pad will serve. For full details on heat sinking Micrel LDOs in this application, refer to Micrel Application Hint 17, "P.C. Board Heat Sinking", or for more stringent requirements refer to Micrel Application Note 9, "Design Considerations for 5V to 3.3V Pass Regulators".

Notes

NOTE 1: IBM™ and "Blue Lightning"™ are trademarks of IBM Corp.

NOTE 2: Super ßeta PNP is a trademark of Micrel, Inc.

NOTE 3: At press time, the Blue Lightning supply currents and voltages have not been finalized. If other than 3.3V or 3.6V are needed, the Micrel MIC29152 adjustable 1.5A regulator is available which can provide any output voltage from about 1.2V to 25V, programmed using two external resistors. See the MIC29150 datasheet for full details.

SECTION 7: SWITCH-MODE VOLTAGE REGULATORS

Switching Regulator Selection Guide

Device	Input Voltage Range	Preferred Topology	Maximum Input Current	Control Mode	Maximum Frequency	Features				Package
						Front Edge Blanking	Shut-down	Over Current Shutdown / Current Limit	Thermal Protection	
MIC2172 adjustable	3V to 40V	Boost	1.25A	Current	100kHz			•	•	SOIC P-DIP CerDIP
MIC3172 adjustable	3V to 40V	Boost	1.25A	Current	100kHz		•	•	•	
LM2574 3.3V, 5.0V, 12V, 15V, adjustable	4V to 40V	Buck	0.5A	Voltage	52kHz		•	•	•	SOIC P-DIP
LM1575/ 2575 3.3V, 5.0V, 12V, 15V, adjustable	4V to 40V	Buck	1A	Voltage	52kHz		•	•	•	TO-3 TO-220 TO-263 P-DIP SOIC
LM1576/ 2576 3.3V, 5.0V, 12V, 15V, adjustable	4V to 40V	Buck	3A	Voltage	52kHz		•	•	•	TO-3 TO-220 TO-263
MIC18xC42/ 43/44/45 MIC38xC42/ 43/44/45	8V to 18V	Buck or Boost	—	Current	>500kHz			•		P-DIP CerDIP SOIC
MIC3830/ 31/32/33	8V to 21V	Current-Fed	—	Current or Voltage	500kHz	•	•	•		P-DIP CerDIP SOIC
MIC631/2/3 3.3V, 5.0V, 12V, 15V	2V to 16.5V	Boost	450mA	Hysteretic	50kHz				•	P-DIP CerDIP SOIC
MIC641/2/3 3.3V, 5.0V, 12V, 15V	2V to 16.5V	Boost	Determined by external MOSFET	Hysteretic	50kHz				•	P-DIP CerDIP SOIC

LM2574

52kHz Simple 0.5A Buck Voltage Regulator

General Description

The LM2574 family is a series of easy to use fixed and adjustable switching voltage regulators. The LM2574 contains all of the active circuitry necessary to construct a stepdown (buck) switching regulator and requires a minimum of external components.

The LM2574 is available in 3.3V, 5V, 12V, and 15V fixed output versions, or an adjustable version with an output voltage range of 1.23V to 37V. Output voltage is guaranteed to ±4% for specified input and load conditions.

The LM2574 can supply 0.5A while maintaining excellent line and load regulation. The output switch includes cycle-by-cycle current limiting, as well as thermal shutdown for full protection under fault conditions.

An external shutdown connection selects operating or standby modes. Standby current is less than 200µA.

Heat sinks are generally unnecessary due the regulator's high efficiency. Adequate heat transfer is usually provided by soldering all package pins to a printed circuit board.

The LM2574 includes internal frequency compensation and an internal 52kHz fixed frequency oscillator guaranteed to ±10% of the frequency.

Circuits constructed around the LM2574 use a standard series of inductors which are available from several different manufacturers.

Features

- 3.3V, 5V, 12V, 15V, and Adjustable Output Versions
- Adjustable Version Output 1.23V to 37V ±4% Max. over Line and Load Conditions.
- Guaranteed 0.5A Output Current
- Wide Input Voltage, up to 40V
- Thermal Shutdown and Current Limit Protection
- Requires only 4 external Components.
- Shutdown Capability (Standby Mode)
- Low Power Standby Mode < 200µA Typical
- High Efficiency
- 52kHz Fixed Frequency Internal Oscillator
- Uses Standard Inductors

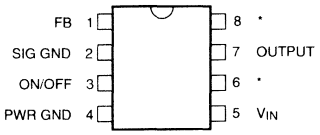
Applications

- Simple High-efficiency Step-down (Buck) Regulator
- Efficient Pre-Regulator for Linear Regulators
- On-card Switching Regulators
- Positive to Negative Converter (Buck-Boost)

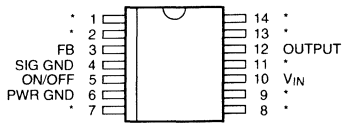
Ordering Information

Part Number	Temp. Range	Package
LM2574BN	–40°C to +85°C	8-pin Plastic DIP
LM2574BWM	–40°C to +85°C	14-pin Wide SOIC
LM2574-3.3BN	–40°C to +85°C	8-pin Plastic DIP
LM2574-3.3BWM	–40°C to +85°C	14-pin Wide SOIC
LM2574-5.0BN	–40°C to +85°C	8-pin Plastic DIP
LM2574-5.0BWM	–40°C to +85°C	14-pin Wide SOIC
LM2574-12BN	–40°C to +85°C	8-pin Plastic DIP
LM2574-12BWM	–40°C to +85°C	14-pin Wide SOIC
LM2574-15BN	–40°C to +85°C	8-pin Plastic DIP
LM2574-15BWM	–40°C to +85°C	14-pin Wide SOIC

Pin Configuration



8-pin DIP (N)



14-pin SOIC (WM)

* NC: solder to printed circuit for maximum heat transfer

Typical Application

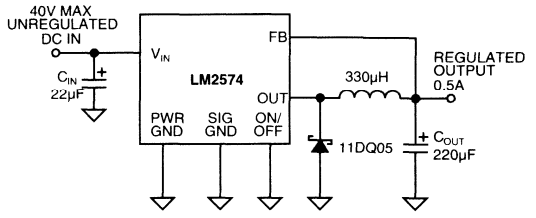


Figure 1. Fixed Output Regulator Circuit

7

Absolute Maximum Ratings

Maximum Supply Voltage
- LM2574 ..... 45V

OFF Pin Input Voltage ..... $-0.3V \le V \le V_{IN}$
Output Voltage to Ground (Steady State) ..... −1V
Power Dissipation ..... Internally Limited
Storage Temperature Range ..... −65°C to +150°C
Minimum ESD Rating
- C = 100pF, R = 1.5kΩ 2kV
- FB Pin 1kV

Lead Temperature (soldering, 10 sec.) ..... 260°C
Maximum Junction Temperature ..... 150°C

Operating Ratings

Temperature Range
- LM2574 ..... $40°C \le T_J \le +125°C$

Supply Voltage
- LM2574 ..... 40V

Electrical Characteristics

Specifications with standard typeface are for T_J = 25°C, and those with boldface type apply over full Operating Temperature Range. Unless otherwise specified, V_{in} = 12V, and I_{LOAD} = 100mA.

Symbol	Parameter	Condition	Min	Typ	Max	Units
SYSTEM PARAMETERS, ADJUSTABLE REGULATORS (Note 3) Test Circuit *Figure 2*						
V_{OUT}	Feedback Voltage	V_{IN} = 12V, I_{LOAD} = 0.1A, V_{OUT} = 5V	1.217	1.230	1.243	V
V_{OUT}	Feedback Voltage (LM2574)	$0.1A \le I_{LOAD} \le 0.5A$, $7V \le V_{IN} \le 40V$, V_{OUT} = 5V	1.193 **1.180**	1.230	1.267 **1.280**	V V
η	Efficiency	V_{IN} = 12V, I_{LOAD} = 0.1A, V_{OUT} = 5V		78		%
SYSTEM PARAMETERS, 3.3V REGULATORS (Note 3) Test Circuit *Figure 3*						
V_{OUT}	Output Voltage	V_{IN} = 12V, I_{LOAD} = 0.1A, V_{OUT} = 3.3V	3.234	3.3	3.366	V
V_{OUT}	Output Voltage (LM2574-3.3)	$0.1A \le I_{LOAD} \le 0.5A$, $4.75V \le V_{IN} \le 40V$, V_{OUT} = 3.3V	3.168 **3.135**	3.3	3.432 **3.465**	V V
η	Efficiency	V_{IN} = 12V, I_{LOAD} = 0.1A		73		%
SYSTEM PARAMETERS, 5V REGULATORS (Note 3) Test Circuit *Figure 3*						
V_{OUT}	Output Voltage	V_{IN} = 12V, I_{LOAD} = 0.1A, V_{OUT} = 5V	4.900	5.0	5.100	V
V_{OUT}	Output Voltage (LM2574-5.0)	$0.1A \le I_{LOAD} \le 0.5A$, $7V \le V_{IN} \le 40V$, V_{OUT} = 5V	4.800 **4.750**	5.0	5.200 **5.250**	V V
η	Efficiency	V_{IN} = 12V, I_{LOAD} = 0.1A, V_{OUT} = 5V		78		%
SYSTEM PARAMETERS, 12V REGULATORS (Note 3) Test Circuit *Figure 3*						
V_{OUT}	Output Voltage	V_{IN} = 25V, I_{LOAD} = 0.1A, V_{OUT} = 12V	11.760	12	12.240	V
V_{OUT}	Output Voltage (LM2574-12)	$0.1A \le I_{LOAD} \le 0.5A$, $15V \le V_{IN} \le 40V$, V_{OUT} = 12V	11.520 **11.400**	12	12.480 **12.600**	V V
η	Efficiency	V_{IN} = 25V, I_{LOAD} = 0.1A		88		%
SYSTEM PARAMETERS, 15V REGULATORS (Note 3) Test Circuit *Figure 3*						
V_{OUT}	Output Voltage	V_{IN} = 30V, I_{LOAD} = 0.1A, V_{OUT} = 15V	14.700	15	15.300	V
V_{OUT}	Output Voltage (LM2574-15)	$0.1A \le I_{LOAD} \le 0.5A$, $18V \le V_{IN} \le 40V$, V_{OUT} = 15V	14.400 **14.250**	15	15.600 **15.750**	V V
η	Efficiency	V_{IN} = 30V, I_{LOAD} = 0.1A		88		%

Electrical Characteristics (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Units
DEVICE PARAMETERS, ADJUSTABLE REGULATOR						
I_B	Feedback Bias Current	V_{OUT} = 5V		50	100 **500**	nA nA
DEVICE PARAMETERS, FIXED and ADJUSTABLE REGULATORS						
f_o	Oscillator Frequency	**Note 8**	47 **42**	52	58 **63**	kHz kHz
V_{SAT}	Saturation Voltage	I_{OUT} = 0.5A, **Note 4**		0.8	1.2 **1.4**	V V
DC	Max Duty Cycle (ON)	**Note 5**	93	98		%
I_{CL}	Current Limit	Peak Current, $t_{ON} \leq 3\mu s$, **Note 4**	0.7 **0.65**	1.0	1.6 **1.8**	A
I_L	Output Leakage Current	V_{IN}, **Note 6**, Output = 0V **Note 6**, Output = –1V		 7.5	2 30	mA
I_Q	Quiescent Current	**Note 6**		5	10	mA
I_{STBY}	Standby Quiescent Current	ON/OFF Pin = 5V (OFF)		50	200	µA
θ_{JA}	Thermal Resistance	N Package, Junction to Ambient, **Note 7** WM Package, Junction to Ambient, **Note 7**		85 100		°C/W °C/W
ON/OFF CONTROL, FIXED and ADJUSTABLE REGULATORS Test Circuit *Figures 2, 3*						
V_{IH}	ON/OFF Input Level	V_{OUT} = 0V	2.2 **2.4**	1.4		V V
V_{IL}	ON/OFF Input Level	V_{OUT} = 15V or 5V		1.2	1.0 **0.8**	V V
I_{IH}	ON/OFF Logic Current	ON/OFF = 5V (OFF)		4	30	µA
I_{IL}	ON/OFF Logic Current	ON/OFF = 0V (ON)		0.01	10	µA

Note 1 Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 2 All limits guaranteed at room temperature (standard type face) and at **temperature extremes (bold type face)**. All room temperature limits are 100% production tested. All limits at **temperature extremes** are guaranteed via testing.

Note 3 External components such as the catch diode, inductor, input and output capacitors can affect switching regulator system performance. When the LM2574 is used as shown in *Figure 1* test circuit, system performance will be shown in system parameters section of Electrical Characteristics.

Note 4 Output (pin 2) sourcing current. No diode, inductor, or capacitor connected to input.

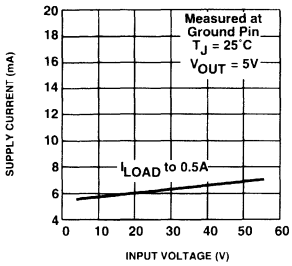
Note 5 Feedback (pin 4) removed from output and connected to 0V.

Note 6 Feedback (pin 4) removed from output and connected to 12V to force the output transistor OFF.

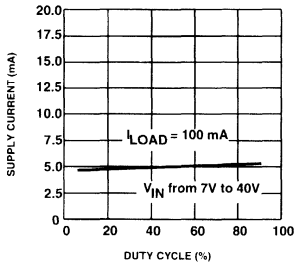
Note 7 Junction to ambient thermal resistance with approximately 1 square inches of PC board copper surrounding the leads.

Typical Performance Characteristics (Circuit of Figure 1)

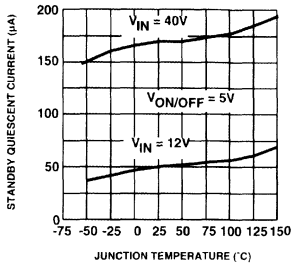
Supply Current



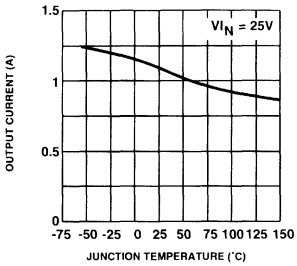
Supply Current vs. Duty Cycle



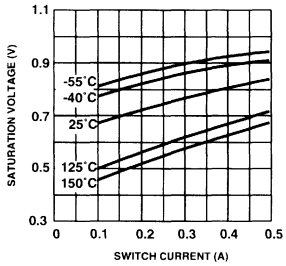
Standby Quiescent Current



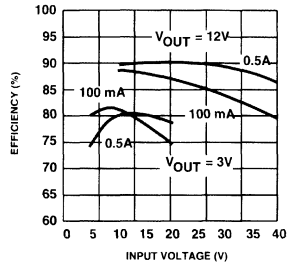
Current Limit



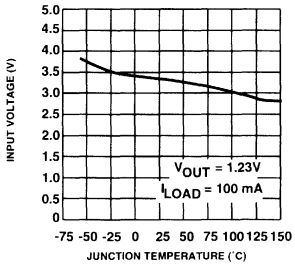
Switch Saturation Voltage



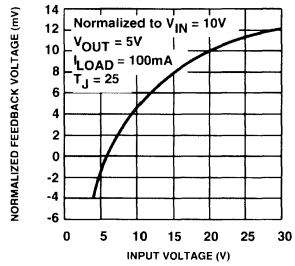
Efficiency



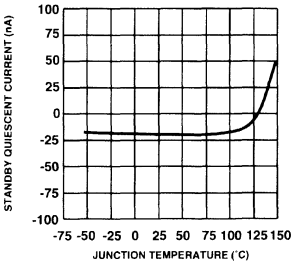
Minimum Operating Voltage



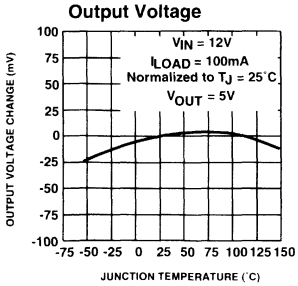
Line Regulation



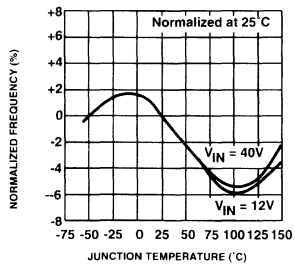
Feedback Pin Current



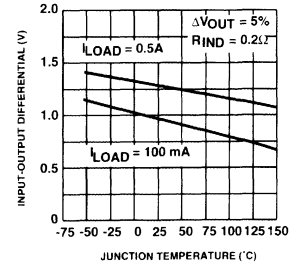
Normalized Output Voltage



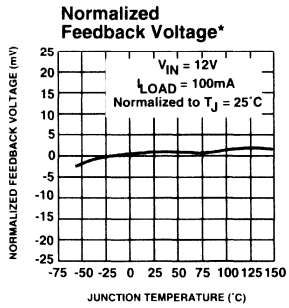
Oscillator Frequency

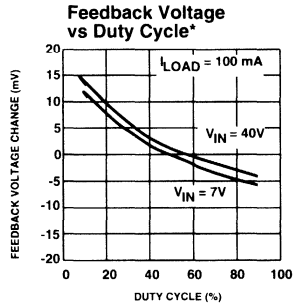


Dropout Voltage



Typical Performance Characteristics (continued)





* Adjustable version only

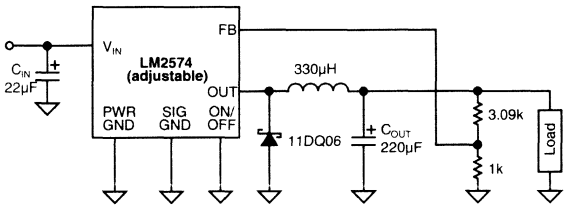


Figure 2. Adjustable Regulator Test Circuit

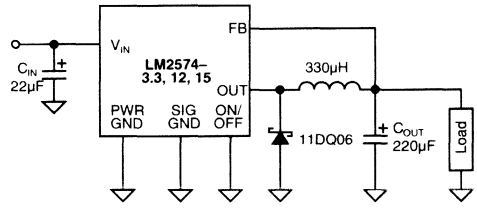
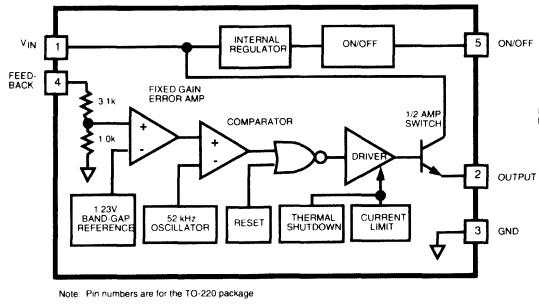


Figure 3. Fixed Regulator Test Circuit

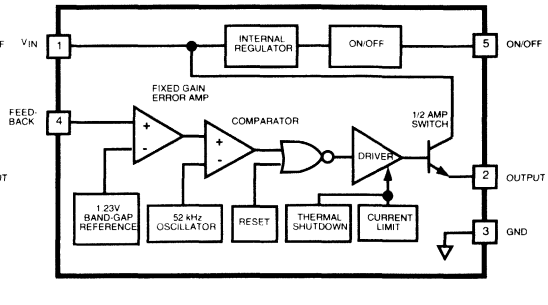
7

Block Diagrams



Note: Pin numbers are for the TO-220 package

Fixed Regulator



Adjustable Regulator

LM2575/1575

52kHz Simple 1A Buck Voltage Regulator

General Description

The LM2575/1575 series of monolithic integrated circuits provide all the active functions for a step-down (buck) switching regulator. Fixed versions are available with a 3.3V, 5V, 12V, or 15V fixed output. Adjustable versions have an output voltage range from 1.23V to 37V. Both versions are capable of driving a 1A load with excellent line and load regulation.

These regulators are simple to use because they require a minimum number of external components and include internal frequency compensation and a fixed-frequency oscillator.

The LM2575 series offers a high efficiency replacement for popular three-terminal adjustable linear regulators. It substantially reduces the size of the heat sink, and in many cases no heat sink is required.

A standard series of inductors available from several different manufacturers are ideal for use with the LM2575 series. This feature greatly simplifies the design of switch-mode power supplies.

The feedback voltage is guaranteed to ±2% tolerance for adjustable versions, and the output voltage is guaranteed to ±3% for fixed versions, within specified input voltages and output load conditions. The oscillator frequency is guaranteed to ±10%. External shutdown is included, featuring less than 200µA standby current. The output switch includes cycle-by-cycle current limiting and thermal shutdown for full protection under fault conditions.

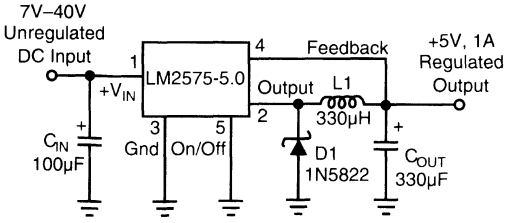
Features

- 3.3V, 5V, 12V, 15V, and adjustable output versions
- Voltage over specified line and load conditions:
  Fixed version: ±3% max. output voltage
  Adjustable version: ±2% max. feedback voltage
- Guaranteed 1A output current
- Wide input voltage range:
  4V to 40V
- Wide output voltage range
  1.23V to 37V
- Requires only 4 external components
- 52kHz fixed frequency internal oscillator
- Low power standby mode I_Q typically < 200µA
- 80% efficiency (adjustable version typically > 80%)
- Uses readily available standard inductors
- Thermal shutdown and current limit protection
- 100% electrical thermal limit burn-in

Applications

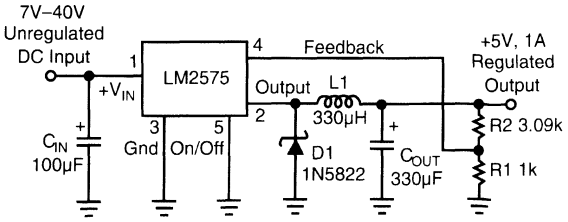
- Simple high-efficiency step-down (buck) regulator
- Efficient pre-regulator for linear regulators
- On-card switching regulators
- Positive to negative converter (inverting Buck-Boost)
- Isolated Flyback Converter using minimum number of external components
- Negative Boost Converter

Typical Applications



Note: Pin numbers are for TO-220 Package

Fixed Regulator in Typical Application



Note: Pin numbers are for TO-220 Package

$$V_{OUT} = 1.23 \left(1 + \frac{R2}{R1}\right)$$

Adjustable Regulator in Fixed Output Application

Ordering Information

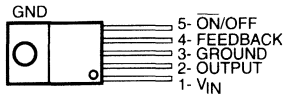
Part Number‡	Temperature Range	Package
LM1575AK*	–55°C to +125°C	4-pin TO-3
LM1575-5.0AK	–55°C to +125°C	4-pin TO-3
LM2575BN	–40°C to +85 °C	16-pin Plastic DIP
LM2575-3.3BN	–40°C to +85 °C	16-pin Plastic DIP
LM2575-5.0BN	–40°C to +85 °C	16-pin Plastic DIP
LM2575-12BN	–40°C to +85 °C	16-pin Plastic DIP
LM2575-15BN	–40°C to +85 °C	16-pin Plastic DIP
LM2575BWM*	–40°C to +85°C	24-pin Wide SOIC
LM2575-3.3BWM	–40°C to +85°C	24-pin Wide SOIC
LM2575-5.0BWM	–40°C to +85°C	24-pin Wide SOIC
LM2575-12BWM	–40°C to +85°C	24-pin Wide SOIC
LM2575-15BWM	–40°C to +85°C	24-pin Wide SOIC
LM2575BT*†	–40°C to +85°C	5-lead TO-220
LM2575-3.3BT†	–40°C to +85°C	5-lead TO-220
LM2575-5.0BT†	–40°C to +85°C	5-lead TO-220
LM2575-12BT†	–40°C to +85°C	5-lead TO-220
LM2575-15BT†	–40°C to +85°C	5-lead TO-220
LM2575BU*	–40°C to +85°C	5-lead TO-263
LM2575-3.3BU	–40°C to +85°C	5-lead TO-263
LM2575-5.0BU	–40°C to +85°C	5-lead TO-263
LM2575-12BU	–40°C to +85°C	5-lead TO-263
LM2575-15BU	–40°C to +85°C	5-lead TO-263

* Adjustable output regulators.
† Contact factory for bent or staggered leads option.

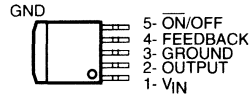
7

Pin Configurations

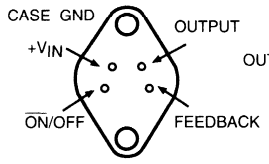
5-LEAD TO-220 (T)



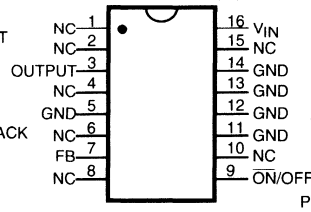
5-LEAD TO-263 (U)



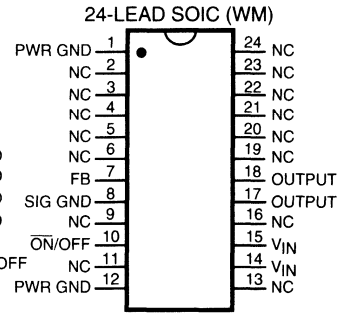
4-LEAD TO-3 (K)



16-LEAD DIP (N)



24-LEAD SOIC (WM)



Absolute Maximum Ratings (Note 1)

Maximum Supply Voltage	
LM1575/LM2575	45V
ON/OFF Pin Input Voltage	$-0.3V \le V \le +40V$
Output Voltage to Ground (Steady State)	−1V
Power Dissipation	Internally Limited
Storage Temperature Range	−65°C to +150°C
Minimum ESD Rating	
C = 100pF, R = 1.5kΩ	2 kV
FB Pin	1 kV
Lead Temperature (soldering, 10 sec.)	260°C
Maximum Junction Temperature	150°C

Operating Ratings

Temperature Range	
LM1575	$-55°C \le T_J \le +150°C$
LM2575	$-40°C \le T_J \le +125°C$
Supply Voltage	
LM2575/1575	40V

Electrical Characteristics

Specifications with standard typeface are for T_J = 25°C, and those with **boldface type** apply over **full Operating Temperature Range.** Unless otherwise specified, V_{IN} = 12V, and I_{LOAD} = 200mA.

Symbol	Parameter	Conditions	Typ	LM1575 Limit (Note 2)	LM2575 Limit (Note 3)	Units (Limits)
SYSTEM PARAMETERS, ADJUSTABLE REGULATORS (Note 4) Test Circuit *Figure 1*						
V_{OUT}	Feedback Voltage	V_{IN} = 12V , I_{LOAD} = 0.2A V_{OUT} = 5V	1.230	 1.217 1.243	 1.217 1.243	V V(min) V(max)
V_{OUT}	Feedback Voltage LM1575/2575	$0.2A \le I_{LOAD} \le 1A$, $8V \le V_{IN} \le 40V$ V_{OUT} = 5V	1.230	 1.205/**1.193** 1.255/**1.267**	 1.193/**1.180** 1.267/**1.280**	V V(min) V(max)
η	Efficiency	V_{IN} = 12V, I_{LOAD} = 1A, V_{OUT} = 5V	82			%
SYSTEM PARAMETERS, 3.3V REGULATORS (Note 4) Test Circuit *Figure 1*						
V_{OUT}	Output Voltage	V_{IN} = 12V , I_{LOAD} = 0.2A V_{OUT} = 3.3V	3.3	 3.267 3.333	 3.234 3.366	V V(min) V(max)
V_{OUT}	Output Voltage LM1575-3.3/2575-3.3	$0.2A \le I_{LOAD} \le 1A$, $8V \le V_{IN} \le 40V$ V_{OUT} = 3.3V	3.3	 3.201/**3.168** 3.399/**3.432**	 3.168/**3.135** 3.432/**3.465**	V V(min) V(max)
η	Efficiency	V_{IN} = 12V, I_{LOAD} = 1A	75			%
SYSTEM PARAMETERS, 5V REGULATORS (Note 4) Test Circuit *Figure 1*						
V_{OUT}	Output Voltage	V_{IN} = 12V , I_{LOAD} = 0.2A V_{OUT} = 5V	5.0	 4.950 5.050	 4.900 5.100	V V(min) V(max)
V_{OUT}	Output Voltage LM1575-5.0/2575-5.0	$0.2A \le I_{LOAD} \le 1A$, $8V \le V_{IN} \le 40V$ V_{OUT} = 5V	5.0	 4.850/**4.800** 5.150/**5.200**	 4.800/**4.750** 5.200/**5.250**	V V(min) V(max)
η	Efficiency	V_{IN} = 12V, I_{LOAD} = 1A	82			%
SYSTEM PARAMETERS, 12V REGULATORS (Note 4) Test Circuit *Figure 1*						
V_{OUT}	Output Voltage	V_{IN} = 25V , I_{LOAD} = 0.2A V_{OUT} = 12V	12	 11.880 12.120	 11.760 12.240	V V(min) V(max)
V_{OUT}	Output Voltage LM1575-12/LM2575-12	$0.2A \le I_{LOAD} \le 1A$, $15V \le V_{IN} \le 40V$ V_{OUT} = 12V	12	 11.640/**11.520** 12.360/**12.480**	 11.520/**11.400** 12.480/**12.600**	V V(min) V(max)
η	Efficiency	V_{IN} = 25V, I_{LOAD} = 1A	88			%

Electrical Characteristics (continued)

Symbol	Parameter	Conditions	Typ	LM1575 Limit (Note 2)	LM2575 Limit (Note 3)	Units (Limits)
SYSTEM PARAMETERS, 15V REGULATORS (Note 4) Test Circuit *Figure 1*						
V_{OUT}	Output Voltage	V_{IN} = 30V , I_{LOAD} = 0.2A V_{OUT} = 15V	15	 14.850 15.150	 14.700 15.300	V V(min) V(max)
V_{OUT}	Output Voltage LM1575-15/2575-15	0.2A ≤ I_{LOAD} ≤ 1A, 18V ≤ V_{IN} ≤ 40V V_{OUT} = 15V	15	 14.550/**14.400** 15.450/**15.600**	 14.400/**14.250** 15.600/**15.750**	V V(min) V(max)
η	Efficiency	V_{IN} = 30V, I_{LOAD} = 1A	88			%
DEVICE PARAMETERS, ADJUSTABLE REGULATOR						
I_B	Feedback Bias Current	V_{OUT} = 5V	50	100/**500**	100/**500**	nA
DEVICE PARAMETERS, FIXED and ADJUSTABLE REGULATORS						
f_O	Oscillator Frequency	(Note 11)	52	 47/**43** 58/**62**	 47/**42** 58/**63**	kHz kHz (min) kHz (max)
V_{SAT}	Saturation Voltage	I_{OUT} = 1A (Note 5)	0.9	 1.2/**1.4**	 1.2/**1.4**	V V(max)
DC	Max Duty Cycle (ON)	(Note 6)	98	 93	 93	% %(min)
I_{CL}	Current Limit	Peak Current, t_{ON} ≤ 3µs (Note 5)	2.2	 1.7/**1.3** 3.0/**3.2**	 1.7/**1.3** 3.0/**3.2**	A A(min) A(max)
I_L	Output Leakage Current	V_{IN} = 40V, (Note 7), Output = 0V Output = –1V (Note 7) Output = –1V	 7.5	2 30	2 30	mA(max) mA mA(max)
I_Q	Quiescent Current	(Note 7)	5	 10/**12**	 10	mA mA(max)
I_{STBY}	Standby Quiescent Current	ON/OFF Pin = 5V (OFF)	50	 200/**500**	 200	µA µA(max)
θ_{JA} θ_{JC} θ_{JA} θ_{JA} θ_{JC} θ_{JA} θ_{JA}	Thermal Resistance	K Package, Junction to Ambient K Package, Junction to Case T Package, Junction to Ambient (Note 8) T Package, Junction to Ambient (Note 9) T Package, Junction to Case N Package, Junction to Ambient (Note 10) WM Package, Junction to Amb. (Note 10)	35 1.5 65 45 2 85 100			°C/W

7

Electrical Characteristics (continued)

Symbol	Parameter	Conditions	Typ	LM1575 Limit (Note 2)	LM2575 Limit (Note 3)	Units (Limits)
ON/OFF CONTROL, FIXED and ADJUSTABLE REGULATORS Test Circuit *Figure 1*						
V_{IH} V_{IL}	ON/OFF Pin Logic Input Level	V_{OUT} = 0V V_{OUT} = 5V	1.4 1.2	2.2/**2.4** 1.0/**0.8**	2.2/**2.4** 1.0/**0.8**	V(min) V(max)
I_{IH}	ON /OFF Pin Logic Current	ON /OFF Pin = 5V (OFF)	4	30	30	µA µA(max)
I_{IL}		ON/OFF Pin = 0V (ON)	0.01	10	10	µA µA(max)

Note 1: Absolute Maximum Rating indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 2: All limits guaranteed at room temperature (standard type face) and at **temperature extremes (bold type face)**. All limits are used to calculate Average Outgoing Quality level, and all are 100% production tested.

Note 3: All limits guaranteed at room temperature (standard type face) and at **temperature extremes (bold type face)**. All room temperature limits are 100% production tested. All limits at **temperature extreme** are guaranteed via testing.

Note 4: External components such as the catch diode, inductor, input and output capacitors can affect switching regulator system performance. When the LM2575/LM1575 is used as shown in *Figure 1* test circuit, system performance will be shown in system parameters section of Electrical Characteristics.

Note 5: Output (pin 2) sourcing current. No diode, inductor or capacitor connected to output.

Note 6: Feedback (pin 4) removed from output and connected to 0V.

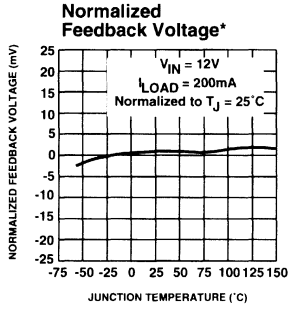
Note 7: Feedback (pin 4) removed from output and connected to 12V to force the output transistor OFF.

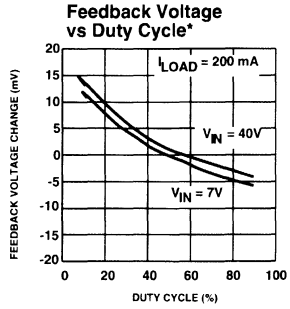
Note 8: Junction to ambient thermal resistance (no external heat sink) for the 5-lead TO-220 package mounted vertically, with 1/2" leads in a socket, or on PC board with minimum copper area.

Note 9: Junction to ambient thermal resistance (no external heat sink) for the 5-lead TO-220 package mounted vertically, with 1/4" leads soldered to PC board containing approximately 4 square inches of copper area surrounding the leads.

Note 10: Junction to ambient thermal resistance with approximately 1 square inch of pc board copper surrounding the leads. Additional copper will lower thermal resistance further.

Typical Performance Characteristics

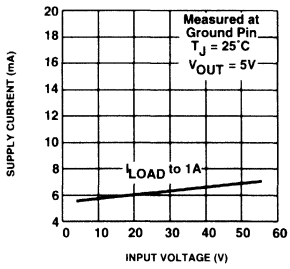




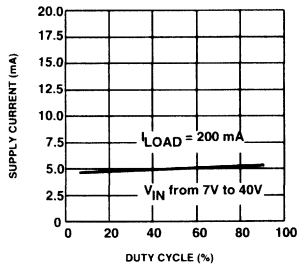
* Adjustable version only

Typical Performance Characteristics (continued) (Circuit of *Figure 1*)

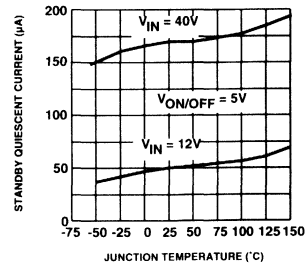
Supply Current



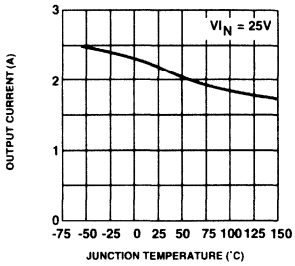
Supply Current vs. Duty Cycle



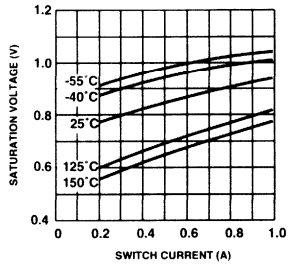
Standby Quiescent Current



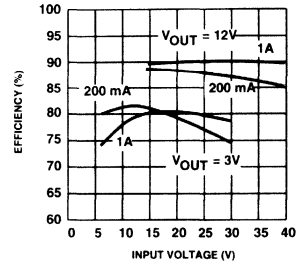
Current Limit



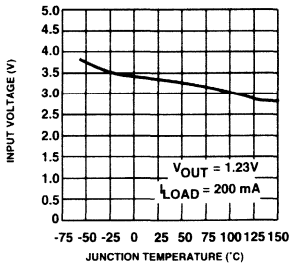
Switch Saturation Voltage



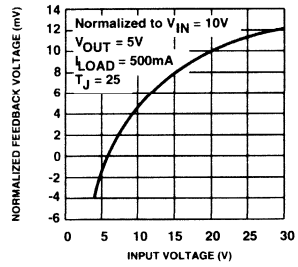
Efficiency



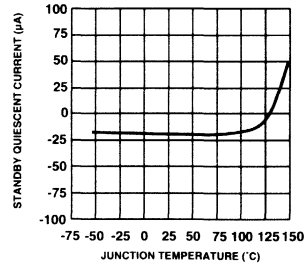
Minimum Operating Voltage



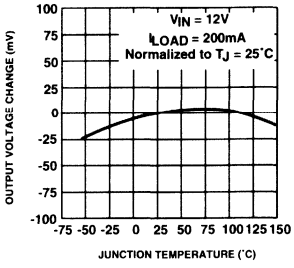
Line Regulation



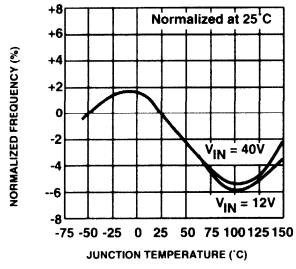
Feedback Pin Current



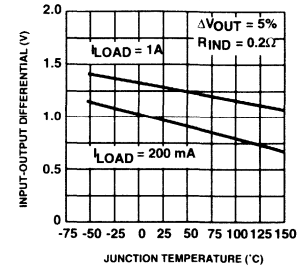
Normalized Output Voltage



Oscillator Frequency



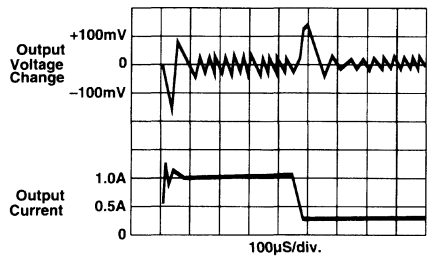
Dropout Voltage



7

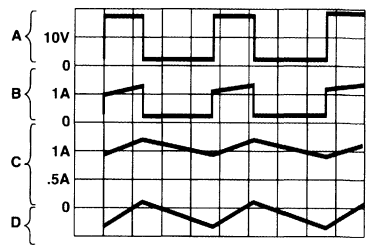
Typical Performance Characteristics (Circuit of *Figure 1*)

Load Transient Response



V_{OUT} = 5V

Switching Waveforms

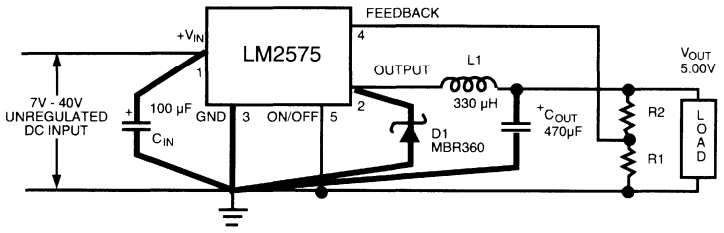


V_{OUT} = 5V V_{IN} = 20V

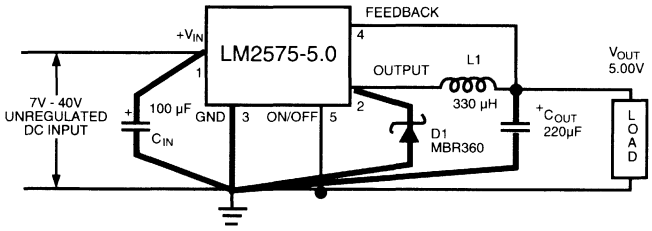
A: Output pin voltage 10V/div
B: Output pin current 1A/div
C: Inductor current 0.5A/div
D: Output ripple voltage 20 mV/div. AC coupled

Horizontal Time Base: 5µs/div

Test Circuits and Layout Guidelines



C_{IN} — 100µF, 75V Aluminum Electrolytic
C_{OUT} — 470µF, 15V Aluminum Electrolytic
D1 — Schottky, MBR360
L1 — 330µH, 415-0926 (AIE)
R1 — 1k, 0.01%
R2 — 3.065k, 0.01%
5-pin TO-220 socket—2936 (Loranger Mfg. Co.)
4-pin TO-3 socket—8112-AG7 (Augat Inc.)



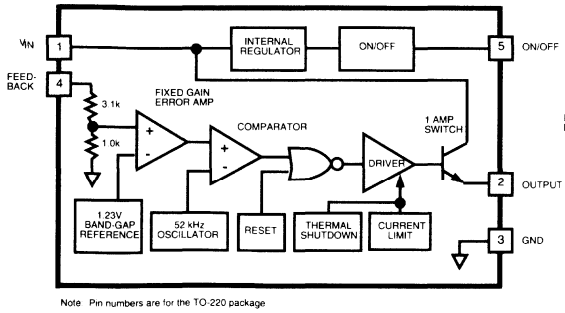
C_{IN} — 100µF, 75V Aluminum Electrolytic
C_{OUT} — 330µF, 15V Aluminum Electrolytic
D1 — Schottky, MBR360
L1 — 330µH, 415-0926 (AIE)
5-pin TO-220 socket—2936 (Loranger Mfg. Co.)
4-pin TO-3 socket—8112-AG7 (Augat Inc.)

Note: Pin numbers are for TO-220 Package

Figure 1.

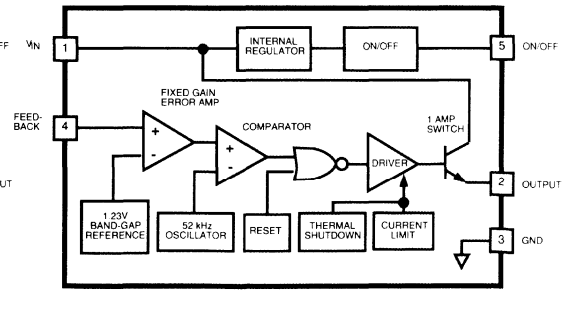
As in any switching regulator, layout is very important. Rapidly switching currents associated with wiring inductance generate voltage transients which can cause problems. For minimal stray inductance and ground loops, the length of the leads indicated by heavy lines should be kept as short as possible. Single-point grounding (as indicated) or ground plane construction should be used for best results.

Block Diagrams



Note Pin numbers are for the TO-220 package

Fixed Regulator



Adjustable Regulator

LM2576/1576

52kHz Simple 3A Buck Voltage Regulator

General Description

The LM2576 series of monolithic integrated circuits provide all the active functions for a step-down (buck) switching regulator. Fixed versions are available with a 3.3V, 5V, 12V, or 15V fixed output. Adjustable versions have an output voltage range from 1.23V to 37V. Both versions are capable of driving a 3A load with excellent line and load regulation.

These regulators are simple to use because they require a minimum number of external components and include internal frequency compensation and a fixed-frequency oscillator.

The LM2576 series offers a high efficiency replacement for popular three-terminal adjustable linear regulators. It substantially reduces the size of the heat sink, and in many cases no heat sink is required.

A standard series of inductors available from several different manufacturers are ideal for use with the LM2576 series. This feature greatly simplifies the design of switch-mode power supplies.

The feedback voltage is guaranteed to ±2% tolerance for adjustable versions, and the output voltage is guaranteed to ±3% for fixed versions, within specified input voltages and output load conditions. The oscillator frequency is guaranteed to ±10%. External shutdown is included, featuring less than 200μA standby current. The output switch includes cycle-by-cycle current limiting and thermal shutdown for full protection under fault conditions.

Features

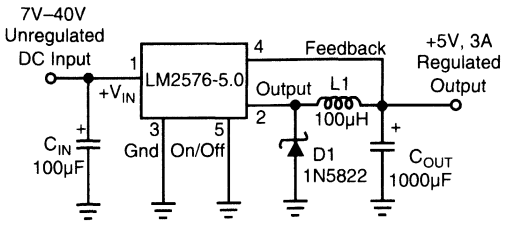
- 3.3V, 5V, 12V, 15V, and adjustable output versions
- Voltage over specified line and load conditions:
  Fixed version: ±3% max. output voltage
  Adjustable version: ±2% max. feedback voltage
- Guaranteed 3A output current
- Wide input voltage range:
  4V to 40V
- Wide output voltage range
  1.23V to 37V
- Requires only 4 external components
- 52kHz fixed frequency internal oscillator
- Low power standby mode I_Q typically < 200μA
- 80% efficiency (adjustable version typically > 80%)
- Uses readily available standard inductors
- Thermal shutdown and current limit protection
- 100% electrical thermal limit burn-in

Applications

- Simple high-efficiency step-down (buck) regulator
- Efficient pre-regulator for linear regulators
- On-card switching regulators
- Positive to negative converter (inverting Buck-Boost)
- Isolated Flyback Converter using minimum number of external components
- Negative Boost Converter

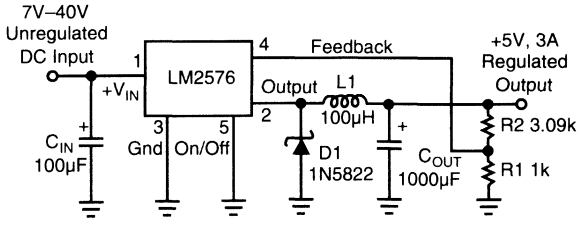
7

Typical Applications



Note: Pin numbers are for TO-220 Package

Fixed Regulator in Typical Application



Note: Pin numbers are for TO-220 Package

$$V_{OUT} = 1.23\left(1 + \frac{R2}{R1}\right)$$

Adjustable Regulator in Fixed Output Application

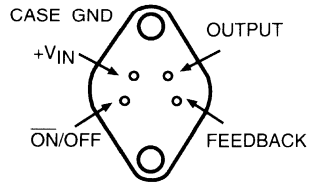
Ordering Information

Part Number‡	Temperature Range	Package
LM1576AK*	–55°C to +125°C	4-pin TO-3
LM1576-3.3AK	–55°C to +125°C	4-pin TO-3
LM1576-5.0AK	–55°C to +125°C	4-pin TO-3
LM1576-12AK	–55°C to +125°C	4-pin TO-3
LM1576-15AK	–55°C to +125°C	4-pin TO-3
LM2576BT*†	–40°C to +85°C	5-lead TO-220
LM2576-3.3BT†	–40°C to +85°C	5-lead TO-220
LM2576-5.0BT†	–40°C to +85°C	5-lead TO-220
LM2576-12BT†	–40°C to +85°C	5-lead TO-220
LM2576-15BT†	–40°C to +85°C	5-lead TO-220
LM2576BU*	–40°C to +85°C	5-lead TO-263
LM2576-3.3BU	–40°C to +85°C	5-lead TO-263
LM2576-5.0BU	–40°C to +85°C	5-lead TO-263
LM2576-12BU	–40°C to +85°C	5-lead TO-263
LM2576-15BU	–40°C to +85°C	5-lead TO-263

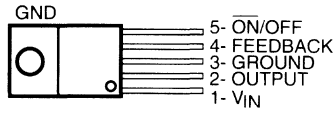
* Adjustable output regulators.
† Contact factory for bent or staggered leads option.

Pin Configurations

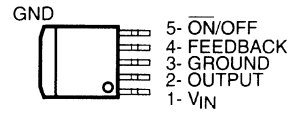
4-LEAD TO-3 (K)



5-LEAD TO-220 (T)



5-LEAD TO-263 (U)



Absolute Maximum Ratings (Note 1)

Maximum Supply Voltage	
LM1576/LM2576	45V
ON/OFF Pin Input Voltage	$-0.3V \le V \le +40V$
Output Voltage to Ground (Steady State)	−1V
Power Dissipation	Internally Limited
Storage Temperature Range	−65°C to +150°C
Minimum ESD Rating	
C = 100pF, R = 1.5kΩ	2 kV
FB Pin	1 kV
Lead Temperature (soldering, 10 sec.)	260°C
Maximum Junction Temperature	150°C

Operating Ratings

Temperature Range	
LM1576	$-55°C \le T_J \le +150°C$
LM2576	$-40°C \le T_J \le +125°C$
Supply Voltage	
LM2576/1576	40V

Electrical Characteristics

Specifications with standard typeface are for T_J = 25°C, and those with **boldface type** apply over **full Operating Temperature Range.** Unless otherwise specified, V_{IN} = 12V, and I_{LOAD} = 500mA.

Symbol	Parameter	Conditions	Typ	LM1576 Limit (Note 2)	LM2576 Limit (Note 3)	Units (Limits)
SYSTEM PARAMETERS, ADJUSTABLE REGULATORS (Note 4) Test Circuit *Figure 1*						
V_{OUT}	Feedback Voltage	V_{IN} = 12V , I_{LOAD} = 0.5A V_{OUT} = 5V	1.230	 1.217 1.243	 1.217 1.243	V V(min) V(max)
V_{OUT}	Feedback Voltage LM1576/2576	$0.5A \le I_{LOAD} \le 3A$, $6V \le V_{IN} \le 40V$ V_{OUT} = 5V	1.230	 1.205/**1.193** 1.255/**1.267**	 1.193/**1.180** 1.267/**1.280**	V V(min) V(max)
η	Efficiency	V_{IN} = 12V, I_{LOAD} = 3A, V_{OUT} = 5V	82			%
SYSTEM PARAMETERS, 3.3V REGULATORS (Note 4) Test Circuit *Figure 1*						
V_{OUT}	Output Voltage	V_{IN} = 12V , I_{LOAD} = 0.5A V_{OUT} = 3.3V	3.3	 3.267 3.333	 3.234 3.366	V V(min) V(max)
V_{OUT}	Output Voltage LM1576-3.3/2576-3.3	$0.5A \le I_{LOAD} \le 3A$, $6V \le V_{IN} \le 40V$ V_{OUT} = 3.3V	3.3	 3.201/**3.168** 3.399/**3.432**	 3.168/**3.135** 3.432/**3.465**	V V(min) V(max)
η	Efficiency	V_{IN} = 12V, I_{LOAD} = 3A	75			%
SYSTEM PARAMETERS, 5V REGULATORS (Note 4) Test Circuit *Figure 1*						
V_{OUT}	Output Voltage	V_{IN} = 12V , I_{LOAD} = 0.5A V_{OUT} = 5V	5.0	 4.950 5.050	 4.900 5.100	V V(min) V(max)
V_{OUT}	Output Voltage LM1576-5.0/2576-5.0	$0.5A \le I_{LOAD} \le 3A$, $8V \le V_{IN} \le 40V$ V_{OUT} = 5V	5.0	 4.850/**4.800** 5.150/**5.200**	 4.800/**4.750** 5.200/**5.250**	V V(min) V(max)
η	Efficiency	V_{IN} = 12V, I_{LOAD} = 3A	82			%
SYSTEM PARAMETERS, 12V REGULATORS (Note 4) Test Circuit *Figure 1*						
V_{OUT}	Output Voltage	V_{IN} = 25V , I_{LOAD} = 0.5A V_{OUT} = 12V	12	 11.880 12.120	 11.760 12.240	V V(min) V(max)
V_{OUT}	Output Voltage LM1576-12/LM2576-12	$0.5A \le I_{LOAD} \le 3A$, $15V \le V_{IN} \le 40V$ V_{OUT} = 12V	12	 11.640/**11.520** 12.360/**12.480**	 11.520/**11.400** 12.480/**12.600**	V V(min) V(max)
η	Efficiency	V_{IN} = 25V, I_{LOAD} = 3A	88			%

7

Electrical Characteristics (continued)

Symbol	Parameter	Conditions	Typ	LM1576 Limit (Note 2)	LM2576 Limit (Note 3)	Units (Limits)
SYSTEM PARAMETERS, 15V REGULATORS (Note 4) Test Circuit *Figure 1*						
V_{OUT}	Output Voltage	V_{IN} = 30V , I_{LOAD} = 0.5A V_{OUT} = 15V	15	 14.850 15.150	 14.700 15.300	V V(min) V(max)
V_{OUT}	Output Voltage LM1576-15/2576-15	0.5A ≤ I_{LOAD} ≤ 3A, 18V ≤ V_{IN} ≤ 40V V_{OUT} = 15V	15	 14.550/**14.400** 15.450/**15.600**	 14.400/**14.250** 15.600/**15.750**	V V(min) V(max)
η	Efficiency	V_{IN} = 30V, I_{LOAD} = 3A	88			%
DEVICE PARAMETERS, ADJUSTABLE REGULATOR						
I_B	Feedback Bias Current	V_{OUT} = 5V	50	100/**500**	100/**500**	nA
DEVICE PARAMETERS, FIXED and ADJUSTABLE REGULATORS						
f_O	Oscillator Frequency	(Note 11)	52	 47/**43** 58/**62**	 47/**42** 58/**63**	kHz kHz (min) kHz (max)
V_{SAT}	Saturation Voltage	I_{OUT} = 3A (Note 5)	1.4	 1.8/**2.0**	 1.8/**2.0**	V V(max)
DC	Max Duty Cycle (ON)	(Note 6)	98	 93	 93	% %(min)
I_{CL}	Current Limit	Peak Current, t_{ON} ≤ 3µs (Note 5)	5.8	 4.2/**3.5** 6.9/**7.5**	 4.2/**3.5** 6.9/**7.5**	A A(min) A(max)
I_L	Output Leakage Current	V_{IN} = 40V, (Note 7), Output = 0V Output = –1V (Note 7) Output = –1V	 7.5	2 30	2 30	mA(max) mA mA(max)
I_Q	Quiescent Current	(Note 7)	5	 10/**12**	 10	mA mA(max)
I_{STBY}	Standby Quiescent Current	ON/OFF Pin = 5V (OFF)	50	 200/**500**	 200	µA µA(max)
θ_{JA} θ_{JC} θ_{JA} θ_{JA} θ_{JC}	Thermal Resistance	K Package, Junction to Ambient K Package, Junction to Case T,U Package, Junction to Ambient (Note 8) T,U Package, Junction to Ambient (Note 9) T,U Package, Junction to Case	35 1.5 65 45 2			°C/W

Electrical Characteristics (continued)

Symbol	Parameter	Conditions	Typ	LM1576 Limit (Note 2)	LM2576 Limit (Note 3)	Units (Limits)
ON/OFF CONTROL, FIXED and ADJUSTABLE REGULATORS Test Circuit *Figure 1*						
V_{IH} V_{IL}	ON/OFF Pin Logic Input Level	V_{OUT} = 0V V_{OUT} = 5V	1.4 1.2	2.2/**2.4** 1.0/**0.8**	2.2/**2.4** 1.0/**0.8**	V(min) V(max)
I_{IH}	ON /OFF Pin Logic Current	ON /OFF Pin = 5V (OFF)	4	30	30	µA µA(max)
I_{IL}		ON/OFF Pin = 0V (ON)	0.01	10	10	µA µA(max)

Note 1: Absolute Maximum Rating indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 2: All limits guaranteed at room temperature (standard type face) and at **temperature extremes (bold type face)**. All limits are used to calculate Average Outgoing Quality level, and all are 100% production tested.

Note 3: All limits guaranteed at room temperature (standard type face) and at **temperature extremes (bold type face)**. All room temperature limits are 100% production tested. All limits at **temperature extreme** are guaranteed via testing.

Note 4: External components such as the catch diode, inductor, input and output capacitors can affect switching regulator system performance. When the LM2576/LM1576 is used as shown in *Figure 1* test circuit, system performance will be shown in system parameters section of Electrical Characteristics.

Note 5: Output (pin 2) sourcing current. No diode, inductor or capacitor connected to output.

Note 6: Feedback (pin 4) removed from output and connected to 0V.

Note 7: Feedback (pin 4) removed from output and connected to 12V to force the output transistor OFF.

Note 8: Junction to ambient thermal resistance (no external heat sink) for the 5-lead TO-220 package mounted vertically, with 1/2" leads in a socket, or on PC board with minimum copper area.

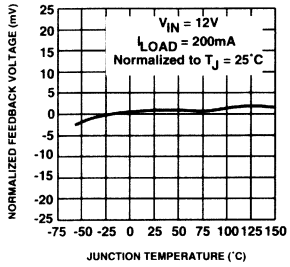
Note 9: Junction to ambient thermal resistance (no external heat sink) for the 5-lead TO-220 package mounted vertically, with 1/4" leads soldered to PC board containing approximately 4 square inches of copper area surrounding the leads.

Note 10: Junction to ambient thermal resistance with approximately 1 square inch of pc board copper surrounding the leads. Additional copper will lower thermal resistance further.

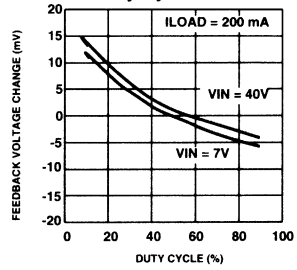
7

Typical Performance Characteristics

Normalized Feedback Voltage*



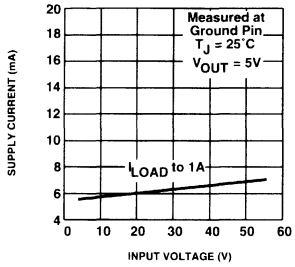
Feedback Voltage vs Duty Cycle*



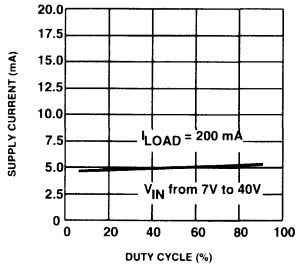
* Adjustable version only

Typical Performance Characteristics (continued) (Circuit of *Figure 1*)

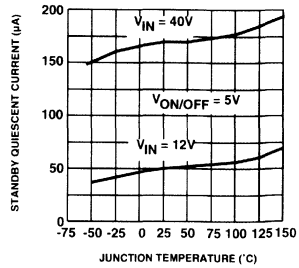
Supply Current



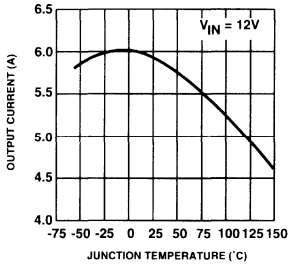
Supply Current vs. Duty Cycle



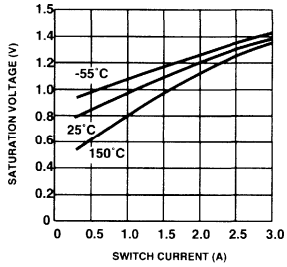
Standby Quiescent Current



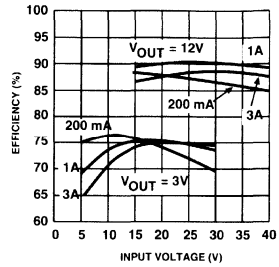
Current Limit



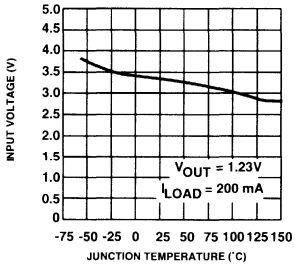
Switch Saturation Voltage



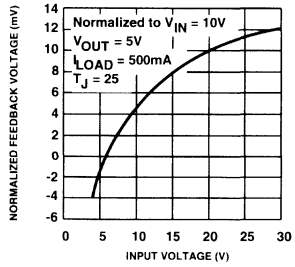
Efficiency



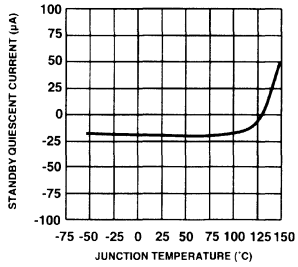
Minimum Operating Voltage



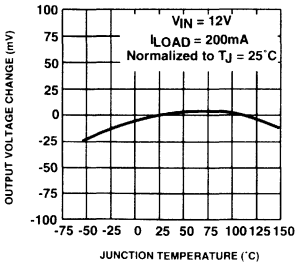
Line Regulation



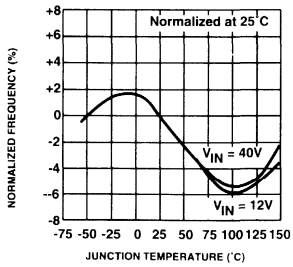
Feedback Pin Current



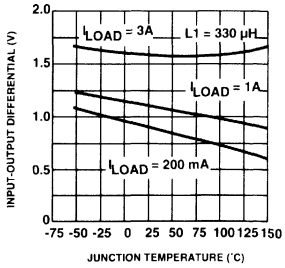
Normalized Output Voltage



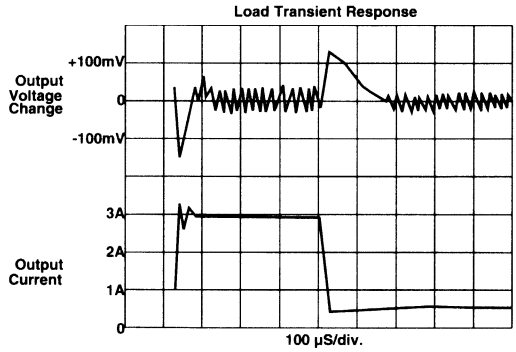
Oscillator Frequency

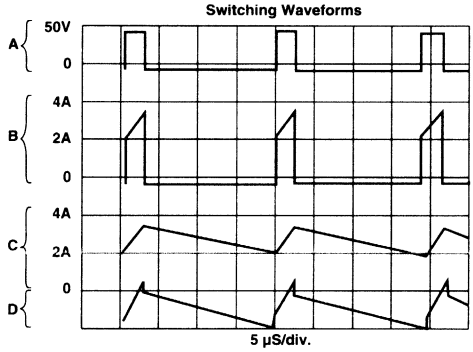


Dropout Voltage



Typical Performance Characteristics (Circuit of *Figure 1*)





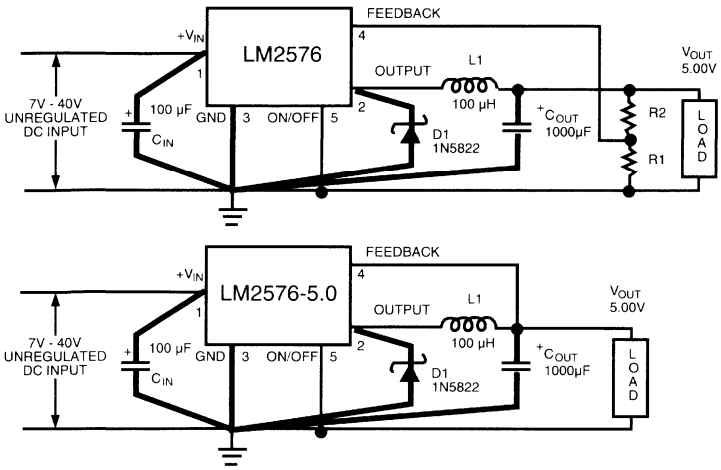
V_{OUT} = 5V V_{IN} = 45V

A: Output pin voltage 50V/div
B: Output pin current 2A/div
C: Inductor current 2A/div
D: Output ripple voltage 50 mV/div., AC coupled

Horizontal Time Base: 5µS/div

7

Test Circuits and Layout Guidelines



C_{IN} — 100µF, 75V Aluminum Electrolytic
C_{OUT} — 1000µF, 15V Aluminum Electrolytic
D1 — Schottky, 1N5822
L1 — 100µH, PE-92108 (Pulse Engineering)
R1 — 1k, 0.01%
R2 — 3.065k, 0.01%
5-pin TO-220 socket—2936 (Loranger Mfg. Co.)
4-pin TO-3 socket—8112-AG7 (Augat Inc.)

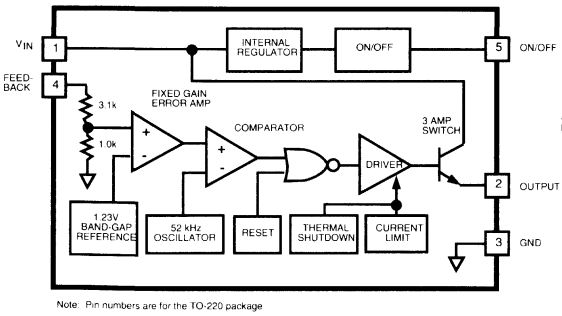
C_{IN} — 100µF, 75V Aluminum Electrolytic
C_{OUT} — 1000µF, 15V Aluminum Electrolytic
D1 — Schottky, 1N5822
L1 — 330µH, PE-92108 (Pulse Engineering)
5-pin TO-220 socket—2936 (Loranger Mfg. Co.)
4-pin TO-3 socket—8112-AG7 (Augat Inc.)

Note: Pin numbers are for TO-220 Package

Figure 1.

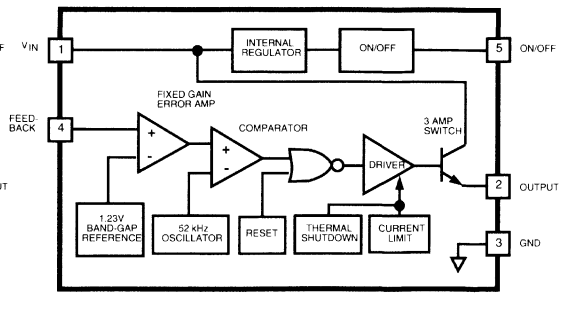
As in any switching regulator, layout is very important. Rapidly switching currents associated with wiring inductance generate voltage transients which can cause problems. For minimal stray inductance and ground loops, the length of the leads indicated by heavy lines should be kept as short as possible. Single-point grounding (as indicated) or ground plane construction should be used for best results.

Block Diagrams



Note: Pin numbers are for the TO-220 package

Fixed Regulator



Adjustable Regulator

MIC4574

200kHz Simple 0.5A Buck Voltage Regulator

Advance Information–Production Q2 '94

General Description

The MIC4574 is a series of easy to use fixed and adjustable BiCMOS step-down (buck) switching voltage regulators. The 200kHz MIC4574 duplicates the pinout and function of the 52kHz LM2574, while the higher switching frequency can result in nearly a 4 to 1 reduction in output filter inductor and capacitor values, reducing printed circuit board space requirements.

The MIC4574 is available in 3.3V, 5V, 12V, and 15V fixed output versions, or an adjustable version with an output voltage range of 1.23V to 37V. Output voltage is guaranteed to ±4% for specified input and load conditions.

The MIC4574 can supply 0.5A while maintaining excellent line and load regulation. The output switch includes cycle-by-cycle current limiting, as well as thermal shutdown for full protection under fault conditions.

An external shutdown connection selects operating or standby modes. Standby current is less than 200µA.

Heat sinks are generally unnecessary due the regulator's high efficiency. Adequate heat transfer is usually provided by soldering all package pins to a printed circuit board.

The MIC4574 includes internal frequency compensation and the internal 200kHz fixed frequency oscillator is guaranteed to ±10%.

Circuits constructed around the MIC4574 use a standard series of inductors which are available from several different manufacturers.

Features

- Fixed 200kHz operation
- Pin compatible with industry standard LM2574
- 3.3V, 5V, 12V, 15V, and adjustable output versions
- Adjustable version output 1.23V to 37V
- ±4% max. over line and load conditions.
- Guaranteed 0.5A output current
- Wide input voltage, up to 40V
- Thermal shutdown and current limit protection
- Requires only 4 external components.
- Shutdown capability (standby mode)
- Low power standby mode < 200µA typical
- High efficiency
- Uses standard inductors

Applications

- Simple high-efficiency step-down (buck) regulator
- Efficient pre-regulator for linear regulators
- On-card switching regulators
- Positive to negative (buck-boost) converter

7

Typical Application

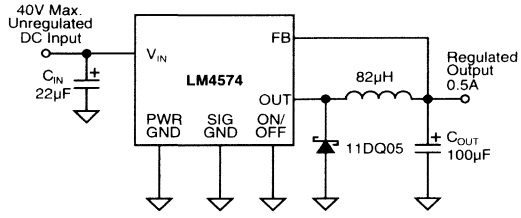
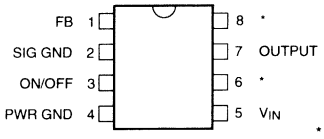


Figure 1. Fixed Output Regulator Circuit

Ordering Information

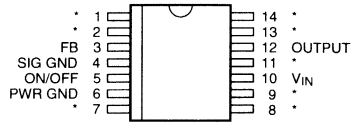
Part Number	Temp. Range	Package
MIC4574BN	–40°C to +85°C	8-pin Plastic DIP
MIC4574BWM	–40°C to +85°C	14-pin Wide SOIC
MIC4574-3.3BN	–40°C to +85°C	8-pin Plastic DIP
MIC4574-3.3BWM	–40°C to +85°C	14-pin Wide SOIC
MIC4574-5.0BN	–40°C to +85°C	8-pin Plastic DIP
MIC4574-5.0BWM	–40°C to +85°C	14-pin Wide SOIC
MIC4574-12BN	–40°C to +85°C	8-pin Plastic DIP
MIC4574-12BWM	–40°C to +85°C	14-pin Wide SOIC
MIC4574-15BN	–40°C to +85°C	8-pin Plastic DIP
MIC4574-15BWM	–40°C to +85°C	14-pin Wide SOIC

Pin Configuration



8-pin DIP (N)

* NC: solder to printed circuit for maximum heat transfer



14-pin SOIC (WM)

MIC4575

200kHz Simple 1A Buck Voltage Regulator

Advance Information–Production Q2 '94

General Description

The MIC4575 is a series of easy to use fixed and adjustable BiCMOS step-down (buck) switching voltage regulators. The 200kHz MIC4575 duplicate the pinout and function of the 52kHz LM1575 and LM2575, while the higher switching frequency can result in nearly a 4 to 1 reduction in output filter inductor and capacitor values, reducing circuit board space requirements.

The MIC4575 is available as a 3.3V, 5V, 12V, or 15V fixed output version or an adjustable output version with an output voltage range from 1.23V to 37V. Both versions are capable of driving a 1A load with excellent line and load regulation.

The MIC4575 can be used as a high efficiency replacement for popular three-terminal adjustable linear regulators. It substantially reduces the size of the heat sink, and in many cases no heat sink is required.

These regulators are simple to use because they require a minimum number of external components and include internal frequency compensation and a fixed-frequency oscillator.

A standard series of inductors available from several different manufacturers are ideal for use with the MIC4575 series. This feature greatly simplifies the design of switch-mode power supplies.

The feedback voltage is guaranteed to ±2% tolerance for adjustable versions, and the output voltage is guaranteed to ±3% for fixed versions, within specified input voltages and output load conditions. The oscillator frequency is guaranteed to ±10%. External shutdown is included, featuring less than 200µA standby current. The output switch includes cycle-by-cycle current limiting and thermal shutdown for full protection under fault conditions.

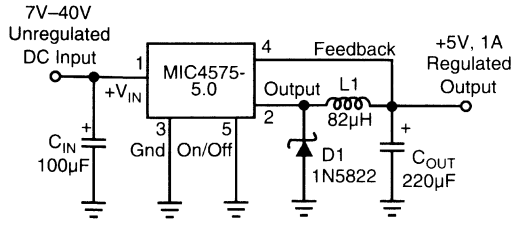
Features

- Fixed 200kHz operation
- Pin compatible with industry standard LM2575
- 3.3V, 5V, 12V, 15V, and adjustable output versions
- Voltage over specified line and load conditions:
  Fixed version: ±3% max. output voltage
  Adjustable version: ±2% max. feedback voltage
- Guaranteed 1A output current
- Wide input voltage range:
  4V to 40V
- Wide output voltage range:
  1.23V to 37V
- Requires only 4 external components
- Low power standby mode I_Q typically < 200µA
- 80% efficiency (adjustable version typically > 80%)
- Uses readily available standard inductors
- Thermal shutdown and current limit protection
- 100% electrical thermal limit burn-in

Applications

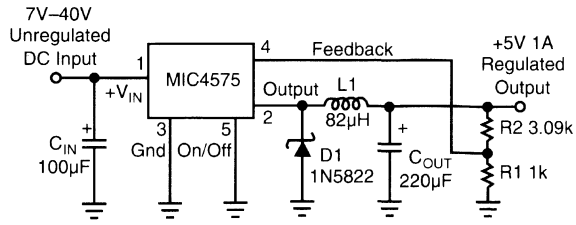
- Simple high-efficiency step-down (buck) regulator
- Efficient pre-regulator for linear regulators
- On-card switching regulators
- Positive to negative converter (inverting buck-boost)
- Isolated flyback converter using minimum number of external components
- Negative boost converter

Typical Applications



Note: Pin numbers are for TO-220 Package

Fixed Regulator in Typical Application



Note: Pin numbers are for TO-220 Package

$$V_{OUT} = 1.23\left(1 + \frac{R2}{R1}\right)$$

Adjustable Regulator in Fixed Output Application

Ordering Information

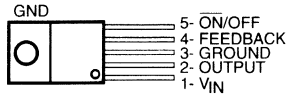
Part Number	Temperature Range	Package
MIC4575AK*	–55°C to +125°C	4-pin TO-3
MIC4575-5.0AK	–55°C to +125°C	4-pin TO-3
MIC4575BN	–40°C to +85 °C	16-pin Plastic DIP
MIC4575-3.3BN	–40°C to +85 °C	16-pin Plastic DIP
MIC4575-5.0BN	–40°C to +85 °C	16-pin Plastic DIP
MIC4575-12BN	–40°C to +85 °C	16-pin Plastic DIP
MIC4575-15BN	–40°C to +85 °C	16-pin Plastic DIP
MIC4575BWM*	–40°C to +85°C	24-pin Wide SOIC
MIC4575-3.3BWM	–40°C to +85°C	24-pin Wide SOIC
MIC4575-5.0BWM	–40°C to +85°C	24-pin Wide SOIC
MIC4575-12BWM	–40°C to +85°C	24-pin Wide SOIC
MIC4575-15BWM	–40°C to +85°C	24-pin Wide SOIC
MIC4575BT*†	–40°C to +85°C	5-lead TO-220
MIC4575-3.3BT†	–40°C to +85°C	5-lead TO-220
MIC4575-5.0BT†	–40°C to +85°C	5-lead TO-220
MIC4575-12BT†	–40°C to +85°C	5-lead TO-220
MIC4575-15BT†	–40°C to +85°C	5-lead TO-220
MIC4575BU*	–40°C to +85°C	5-lead TO-263
MIC4575-3.3BU	–40°C to +85°C	5-lead TO-263
MIC4575-5.0BU	–40°C to +85°C	5-lead TO-263
MIC4575-12BU	–40°C to +85°C	5-lead TO-263
MIC4575-15BU	–40°C to +85°C	5-lead TO-263

* Adjustable output regulators.
† Contact factory for bent or staggered leads option.

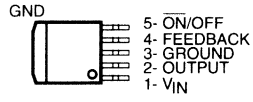
7

Pin Configurations

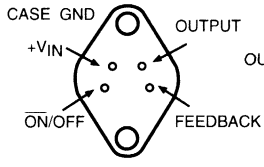
5-LEAD TO-220 (T)



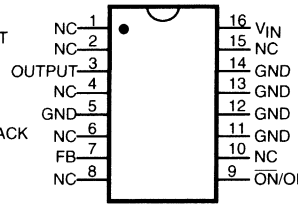
5-LEAD TO-263 (U)



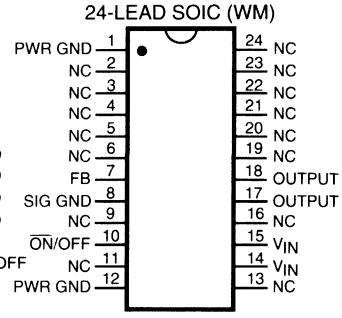
4-LEAD TO-3 (K)



16-LEAD DIP (N)



24-LEAD SOIC (WM)



MIC4576

200kHz Simple 3A Buck Voltage Regulator

Advance Information–Production Q2 '94

General Description

The MIC4576 is a series of easy to use fixed and adjustable BiCMOS step-down (buck) switching voltage regulators. The 200kHz MIC4576 duplicates the pinout and function of the 52kHz LM2576, while the higher switching frequency can result in nearly a 4 to 1 reduction in output filter inductor and capacitor values, reducing printed circuit board space requirements.

The MIC4576 is available in 3.3V, 5V, 12V, and 15V fixed output versions, or and adjustable version with an output voltage range of 1.23 to 37V. Both versions are capable of driving a 3A load with excellent line and load regulation.

The MIC4576 can be used as a high efficiency replacement for popular 3-terminal adjustable linear regulators. It substantially reduces the size of the heat sink, and in many cases, no heat sink is required.

These regulators are simple to use because they require a minimum number of external components and include internal frequency compensation and a fixed-frequency oscillator.

A standard series of inductors, available from several different manufacturers, are ideal for use with the MIC4576. This simplifies the design of switch-mode power supplies.

The feedback voltage is guaranteed to ±2% tolerance for adjustable versions, and the output voltage is guaranteed to ±3% for fixed versions, within specified input voltages and output load conditions. The oscillator frequency is guaranteed to ±10%. External shutdown is included, featuring less than 200µA standby current. The output switch includes cycle-by-cycle current limiting and thermal shutdown for full protection under fault conditions.

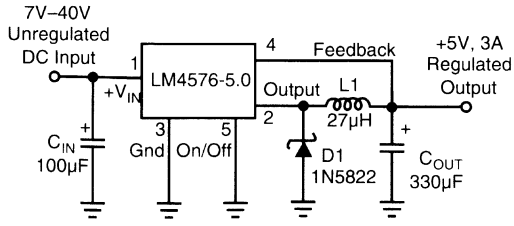
Features

- Fixed 200kHz operation
- Pin compatible with industry standard LM2576
- 3.3V, 5V, 12V, 15V, and adjustable output versions
- Voltage over specified line and load conditions:
  Fixed version: ±3% max. output voltage
  Adjustable version: ±2% max. feedback voltage
- Guaranteed 3A output current
- Wide input voltage range: 4V to 40V
- Wide output voltage range: 1.23V to 37V
- Requires only 4 external components
- Low power standby mode I_Q typically < 200µA
- 80% efficiency (adjustable version typically > 80%)
- Uses readily available standard inductors
- Thermal shutdown and current limit protection
- 100% electrical thermal limit burn-in

Applications

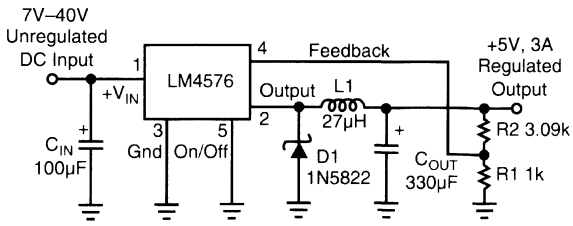
- Simple high-efficiency step-down (buck) regulator
- Efficient pre-regulator for linear regulators
- On-card switching regulators
- Positive to negative converter (inverting buck-boost)
- Isolated flyback converter using minimum number of external components
- Negative boost converter

Typical Applications



Note: Pin numbers are for TO-220 Package

Fixed Regulator in Typical Application



Note: Pin numbers are for TO-220 Package

$$V_{OUT} = 1.23\left(1 + \frac{R2}{R1}\right)$$

Adjustable Regulator in Fixed Output Application

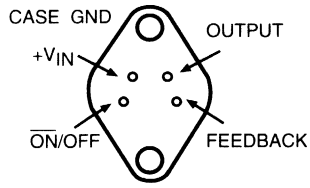
Ordering Information

Part Number	Temperature Range	Package
MIC4576AK*	–55°C to +125°C	4-pin TO-3
MIC4576-3.3AK	–55°C to +125°C	4-pin TO-3
MIC4576-5.0AK	–55°C to +125°C	4-pin TO-3
MIC4576-12AK	–55°C to +125°C	4-pin TO-3
MIC4576-15AK	–55°C to +125°C	4-pin TO-3
LM4576BT*†	–40°C to +85°C	5-lead TO-220
LM4576-3.3BT†	–40°C to +85°C	5-lead TO-220
LM4576-5.0BT†	–40°C to +85°C	5-lead TO-220
LM4576-12BT†	–40°C to +85°C	5-lead TO-220
LM4576-15BT†	–40°C to +85°C	5-lead TO-220
LM4576BU*	–40°C to +85°C	5-lead TO-263
LM4576-3.3BU	–40°C to +85°C	5-lead TO-263
LM4576-5.0BU	–40°C to +85°C	5-lead TO-263
LM4576-12BU	–40°C to +85°C	5-lead TO-263
LM4576-15BU	–40°C to +85°C	5-lead TO-263

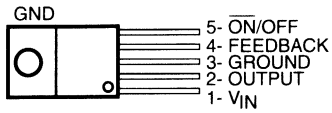
* Adjustable output regulators.
† Contact factory for bent or staggered leads option.

Pin Configurations

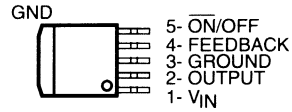
4-LEAD TO-3 (K)



5-LEAD TO-220 (T)



5-LEAD TO-263 (U)



MIC2172/3172

100kHz 1.25A Switching Regulators

Preliminary Information

General Description

The MIC2172 and MIC3172 are complete 100kHz SMPS current-mode controllers with internal 65V 1.25A power switches. The MIC2172 features external frequency synchronization or frequency adjustment while the MIC3172 features an enable/shutdown control input.

Although primarily intended for voltage step-up applications, the floating switch architecture of the MIC2172/3172 makes it practical for step-down, inverting, and "Cuk" configurations as well as isolated topologies.

Operating from 3V to 40V, the MIC2172/3172 draws only 6mA of quiescent current making it attractive for battery operated supplies.

The MIC3172 is for applications that require on/off control of the regulator. The MIC3172 is externally shutdown by applying a TTL low signal to EN (enable). When disabled, the MIC3172 draws only leakage current (typically less than 1μA). EN must be high for normal operation. For applications not requiring control, EN must be tied to V_{IN} (supply).

The MIC2172 is for applications requiring two or more SMPS regulators that operate from the same input supply. The MIC2172 features a SYNC input which allows locking of its internal oscillator to an external reference. This makes it possible to avoid the audible beat frequencies that result from the unequal oscillator frequencies of independent SMPS regulators.

A reference signal can be supplied by one MIC2172 designated as a master. To insure locking of the slave's oscillators, the reference oscillator must be greater than the slaves'. The master MIC2172's oscillator frequency is increased up to 135kHz by connecting a resistor from SYNC to ground (see applications information).

The MIC2172/3172 is available in an 8-pin plastic DIP or SOIC for –40°C to +85°C operation and the 8-pin ceramic DIP for –55°C to +125°C operation.

Features

- 1.25A, 65V internal switch rating
- 3V to 40V input voltage range
- Current-mode operation
- Internal cycle-by-cycle current limit
- Thermal shutdown
- Low external parts count
- Operates in most switching topologies
- 6mA quiescent current (operating)
- <1μA quiescent current, shutdown mode (MIC3172)
- TTL shutdown compatibility (MIC3172)
- External frequency synchronization (MIC2172)
- External frequency trim (MIC2172)
- Fits most LT1172 sockets (see applications info)

Applications

- Laptop/palmtop computers
- Toys
- Hand-held instruments
- Off-line converter up to 50W (requires external power switch)
- Predriver for higher power capability
- Master/slave configurations (MIC2172)

Typical Applications

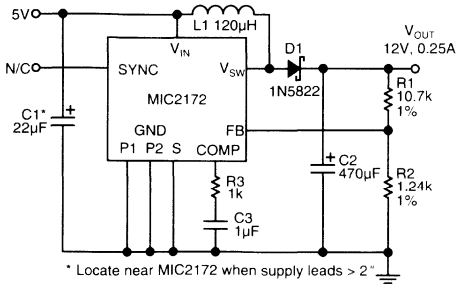


Figure 1.
MIC2172 5V to 12V Boost Converter

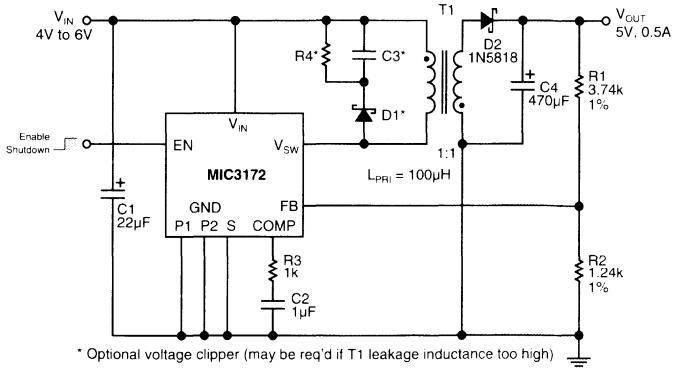
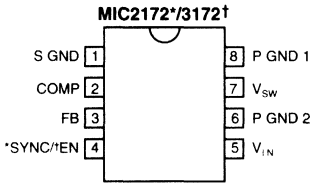


Figure 2.
MIC3172 5V Flyback Converter

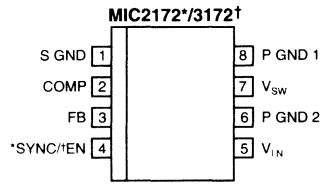
Ordering Information

Part Number	Temperature Range	Package
MIC2172BN	–40°C to +85°C	8-pin plastic DIP
MIC2172BM	–40°C to +85°C	8-lead SOIC
MIC2172AJ	–55°C to +125°C	8-pin ceramic DIP
MIC3172BN	–40°C to +85°C	8-pin plastic DIP
MIC3172BM	–40°C to +85°C	8-lead SOIC
MIC3172AJ	–55°C to +125°C	8-pin ceramic DIP

Pin Configuration



8-lead DIP (N)

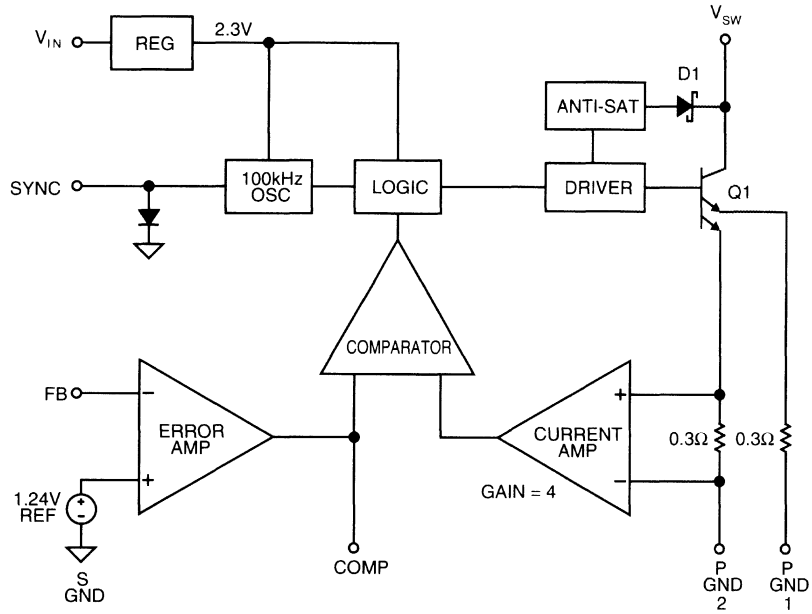


8-lead SOIC (M)

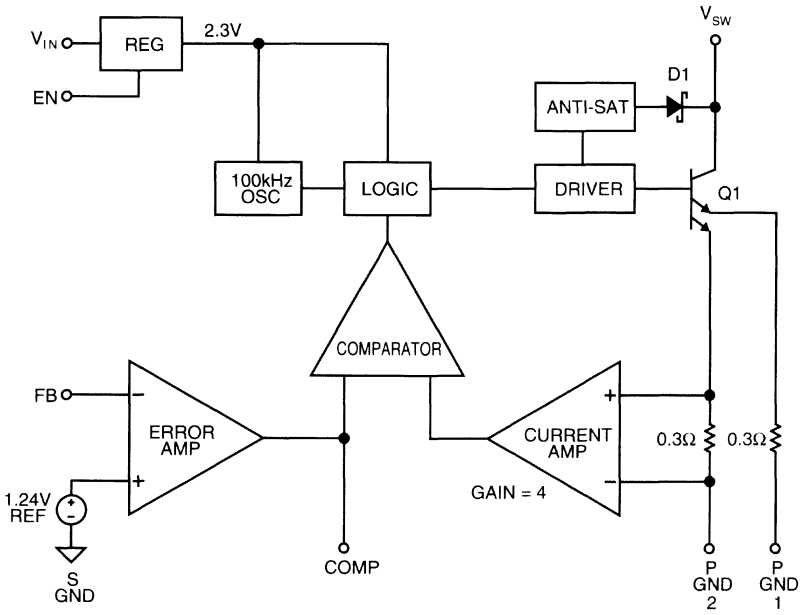
Pin Description

Pin Number	Pin Name	Pin Function
1	S GND	Signal Ground: Internal analog circuit ground. Connect directly to the input filter capacitor for proper operation (see applications info). Keep separate from power grounds.
2	COMP	Frequency Compensation: Output of transconductance type error amplifier. Primary function is for loop stabilization. Can also be used for output voltage soft-start and current limit tailoring.
3	FB	Feedback: Inverting input of error amplifier. Connect to external resistive divider to set power supply output voltage.
4 (MIC2172)	SYNC	Synchronization/Frequency Adjust: Capacitively coupled signal greater than device's free running frequency (up to 135kHz) will lock device's oscillator on falling edge. Oscillator frequency can be trimmed up to 135kHz by adding a resistor to ground. If unused, pin must float (no connection).
4 (MIC3172)	EN	Enable: Apply TTL high or connect to V_{IN} to enable the regulator. Apply TTL low or connect to ground to disable the regulator. Device draws only leakage current (<1μA) when disabled.
5	V_{IN}	Supply Voltage: 3.0V to 40V
6	P GND 2	Power Ground #2: One of two NPN power switch emitters with 0.3Ω current sense resistor in series. Required. Connect to external inductor or input voltage ground depending on circuit topology.
7	V_{SW}	Power Switch Collector: Collector of NPN switch. Connect to external inductor or input voltage depending on circuit topology.
8	P GND 1	Power Ground #1: One of two NPN power switch emitters with 0.3Ω current sense resistor in series. Optional. For maximum power capability connect to P GND 2. Floating pin reduces current limit by a factor of two.

Block Diagram MIC2172



Block Diagram MIC3172



Absolute Maximum Ratings MIC2172

Supply Voltage 40V
Switch Output Voltage 65V
Sync Pin Current 50mA
Feedback Pin Voltage (Transient, 1ms) ..... ±15V
Operating Temperature Range
8-pin PDIP ..... –40 to +85°C
8-pin SOIC ..... –40 to +85°C
8-pin CerDIP ..... –55 to +125°C
Junction Temperature ..... –55°C to 150°C
Thermal Resistance
θ_{JA} 8-pin PDIP ..... 130°C/W
θ_{JA} 8-pin SOIC ..... 120°C/W
θ_{JA} 8-pin CerDIP ..... 100°C/W
Storage Temperature ..... –65°C to 150°C
Soldering (10 sec.) ..... 300°C

Electrical Characteristics MIC2172 (Unless otherwise specified, V_{IN} = 5V)

Parameter	Conditions	Min	Typ	Max	Units
Output Voltage (V_{REF})	Measured at Feedback Pin V_{COMP} = 1.24V	1.224 **1.214**	1.244	1.264 **1.274**	V V
Feedback Input Current (I_B)	$V_{FB} = V_{REF}$		350	750 **1100**	nA nA
Error Amplifier Transconductance (gm)	ΔI_{COMP} = ±25µA	3000 **2400**	4400	6000 **7000**	µS µS
Error Amplifier Source/ Sink Current	V_{COMP} = 1.5V	150 **120**	200	350 **400**	µA µA
Error Amplifier Clamp Voltage	High Clamp, V_{FB} = 1V Low Clamp, V_{FB} = 1.5V	1.8 0.25	2.0 0.38	2.3 0.52	V V
Reference Voltage Regulation	3V ≤ V_{IN} ≤ 40V V_{COMP} = 1.24V			**0.03**	%/V
Error Amp Voltage Gain (A_V)	0.9V ≤ V_{COMP} ≤ 1.4V	500	800	2000	V/V
Minimum Input Voltage			2.6	**3.0**	V
Supply Current (I_Q)	3V ≤ V_{IN} ≤ 40V, V_{COMP} = 0.6V		6	9	mA
Compensation Pin Threshold	Duty Cycle = 0	0.8 **0.6**	0.9	1.08 **1.25**	V V
Output Switch Breakdown Voltage (BV)	3V ≤ V_{IN} ≤ 40V I_{SW} = 5mA	**65**	75		V
Output Switch ON Resistance (V_{SAT})	I_{SW} = 1A, V_{FB} = 0.8V		0.6	**1**	Ω
Comp Voltage to Switch Current Transconductance			2		A/V
Switch Current Limit	Duty Cycle = 50%, $T_J \geq 25°C$ Duty Cycle = 50%, $T_J < 25°C$ Duty Cycle = 80% **Note 1**	**1.25** **1.25** **1**		**3** **3.5** **2.5**	A A A
Supply Current Increase During Switch ON Time ($\Delta I_{IN}/\Delta I_{SW}$)	I_{SW} ≤ 1.25A		7	20	mA/A
Switching Frequency (f)		88 **85**	100	112 **115**	kHz kHz
Maximum Switch Duty Cycle [δ(max)]		80	90	95	%
Sync Coupling Capacitor Required for Frequency Lock	V_{PP} = 3.0V V_{PP} = 40V	22 2.2	51 4.7	120 10	pF pF
Peak-to-Peak Voltage Required for Frequency Lock	$C_{COUPLING}$ = 12pF	2.2	12	30	V

Bold type denotes specifications applicable to the full operating temperature range.

Note 1 For duty cycles (δ) between 50% and 95%, minimum guaranteed switch current is given by I_{CL} = 0.833 (2-δ) for the MIC3172.

Absolute Maximum Ratings MIC3172

Supply Voltage 40V
Switch Output Voltage 65V
Enable Pin Voltage 40V
Feedback Pin Voltage (Transient, 1ms) ..... ±15V
Operating Temperature Range
8-pin PDIP ..... –40 to +85°C
8-pin SOIC ..... –40 to +85°C
8-pin CerDIP ..... –55 to +125°C
Junction Temperature ..... –55°C to 150°C
Thermal Resistance
θ_{JA} 8-pin PDIP ..... 130°C/W
θ_{JA} 8-pin SOIC ..... 120°C/W
θ_{JA} 8-pin CerDIP ..... 100°C/W
Storage Temperature ..... –65°C to 150°C
Soldering (10 sec.) ..... 300°C

Electrical Characteristics MIC3172 (Unless otherwise specified, V_{IN} = 5V)

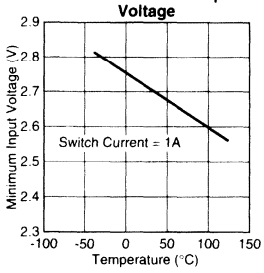
Parameter	Conditions	Min	Typ	Max	Units
Output Voltage (V_{REF})	Measured at Feedback Pin V_{COMP} = 1.24V	1.224 **1.214**	1.244	1.264 **1.274**	V V
Feedback Input Current (I_B)	$V_{FB} = V_{REF}$		350	750 **1100**	nA nA
Error Amplifier Transconductance (gm)	ΔI_{COMP} = ±25µA	3000 **2400**	4400	6000 **7000**	µS µS
Error Amplifier Source/ Sink Current	V_{COMP} = 1.5V	150 **120**	200	350 **400**	µA µA
Error Amplifier Clamp Voltage	High Clamp, V_{FB} = 1V Low Clamp, V_{FB} = 1.5V	1.8 0.25	2.0 0.38	2.3 0.52	V V
Reference Voltage Regulation	3V ≤ V_{IN} ≤ 40V V_{COMP} = 1.24V		0.07		%/V
Error Amp Voltage Gain (A_V)	0.9V ≤ V_{COMP} ≤ 1.4V	500	800	2000	V/V
Minimum Input Voltage			2.6	**3.0**	V
Supply Current (I_Q)	3V ≤ V_{IN} ≤ 40V, V_{COMP} = 0.6V Shutdown, V_{EN} = 0V		6 0.1	9 **5**	mA µA
Compensation Pin Threshold	Duty Cycle = 0	0.8 **0.6**	0.9	1.08 **1.25**	V V
Output Switch Breakdown Voltage (BV)	3V ≤ V_{IN} ≤ 40V I_{SW} = 5mA	**65**	75		V
Output Switch ON Resistance (V_{SAT})	I_{SW} = 1A, V_{FB} = 0.8V		0.6	**1**	Ω
Comp Voltage to Switch Current Transconductance			2		A/V
Switch Current Limit	Duty Cycle = 50%, $T_J \geq 25°C$ Duty Cycle = 50%, $T_J < 25°C$ Duty Cycle = 80% **Note 1**	**1.25** **1.25** **1**		**3** **3.5** **2.5**	A A A
Supply Current Increase During Switch ON Time ($\Delta I_{IN}/\Delta I_{SW}$)	I_{SW} ≤ 1.25A		7	20	mA/A
Switching Frequency (f)		88 **85**	100	112 **115**	kHz kHz
Maximum Switch Duty Cycle [δ(max)]		80	90	95	%
Enable Input Threshold		**0.4**	1.2	**2.4**	V
Enable Input Current	V_{EN} = 0V V_{EN} = 2.4V	–1	0 2	1 **10**	µA µA

Bold type denotes specifications applicable to the full operating temperature range.

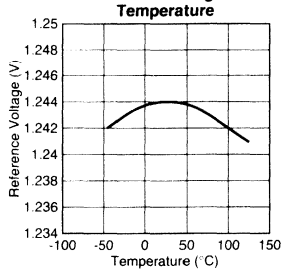
Note 1 For duty cycles (δ) between 50% and 95%, minimum guaranteed switch current is given by I_{CL} = 0.833 (2-δ) for the MIC3172.

Typical Performance Characteristics

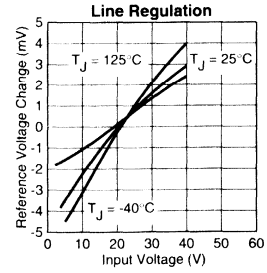
MIC2172 Minimum Input Voltage



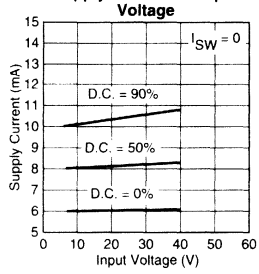
Reference Voltage vs. Temperature



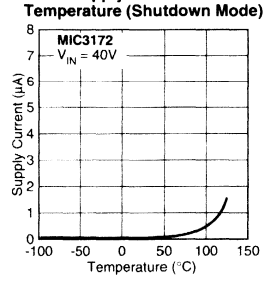
Line Regulation



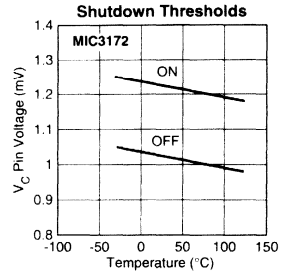
Supply Current vs. Input Voltage



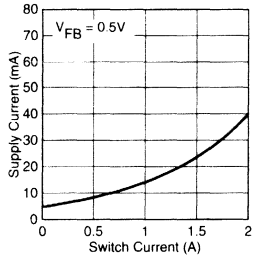
Supply Current vs. Temperature (Shutdown Mode)



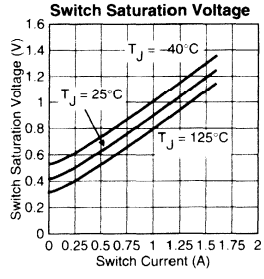
Shutdown Thresholds



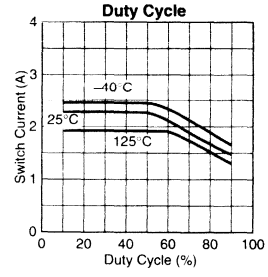
Supply Current vs. Switch Current



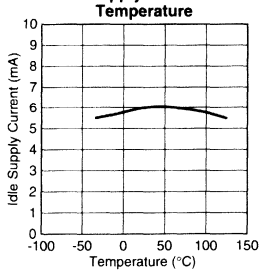
Switch Saturation Voltage



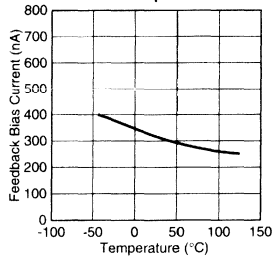
Switch Current Limit vs. Duty Cycle



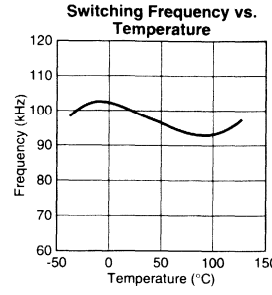
Idle Supply Current vs. Temperature



Feedback Bias Current vs. Temperature

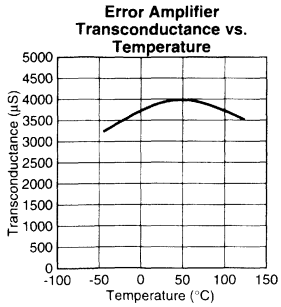


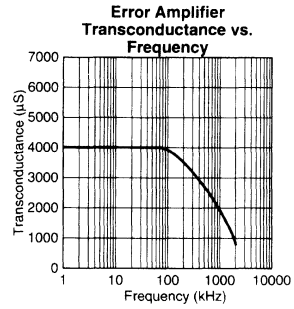
Switching Frequency vs. Temperature

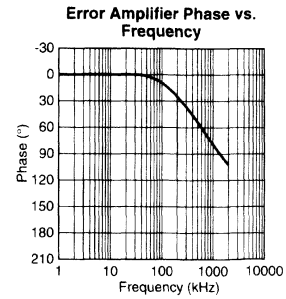


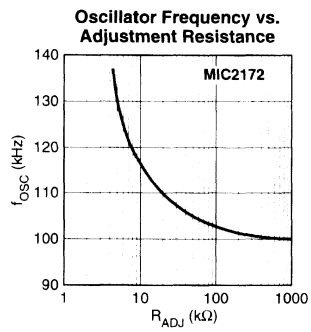
7

Typical Performance Characteristics









Functional Description

Refer to "Block Diagram MIC2172" and "Block Diagram MIC3172."

Internal Power

The MIC2172/3172 operates when V_{IN} is ≥ 2.6V (and V_{EN} ≥ 2.0V for the MIC3172). An internal 2.3V regulator supplies biasing to all internal circuitry including a precision 1.24V band gap reference.

The enable control (MIC3172 only) enables or disables the internal regulator which supplies power to all other internal circuitry.

PWM Operation

The 100kHz oscillator block generates a signal with a duty cycle of approximately 90%. The current-mode comparator output is used to reduce the duty cycle when the current amplifier output voltage exceeds the error amplifier output voltage. The resulting PWM signal controls a driver which supplies base current to output transistor Q1.

Current Mode Advantages

The MIC2172/3172 operates in current mode rather than voltage mode. There are three distinct advantages to this technique. Feedback loop compensation is greatly simplified because inductor current sensing removes a pole from the closed loop response. Inherent cycle-by-cycle current limiting greatly improves the power switch reliability and provides automatic output current limiting. Finally, current-mode operation provides automatic input voltage feed forward which prevents instantaneous input voltage changes from disturbing the output voltage setting.

Anti-Saturation

The anti-saturation diode (D1) increases the usable duty cycle range of the MIC2172/3172 by eliminating the base to collector stored charge which would delay Q1's turn-off.

Compensation

Loop stability compensation of the MIC2172/3172 can be accomplished by connecting an appropriate network from either COMP to circuit ground (Typical Applications) or COMP to FB.

The error amplifier output (COMP) is also useful for soft start and current limiting. Because the error amplifier output is a transconductance type, the output impedance is relatively high which means the output voltage can be easily clamped or adjusted externally.

Typical Application

MIC3172 5V Flyback Converter

Refer to figure 2.

Flyback Topology Advantages

The schematic diagram shows a practical flyback converter design using the MIC3172. Flyback topology is used when the input voltage is less than or greater than the required output voltage. Because the input voltage can be above or below the output voltage, it requires a transformer (T1). Also, the converter's higher power output requires it to operate in continuous mode. (The decision to operate the storage magnetics in continuous versus discontinuous mode for a given application is discussed in "Design Hints: Boost Conversion.")

Flyback Converter Operation

During Q1's on time (Q1 is the internal NPN transistor—see "Block Diagram MIC3172"), energy is stored in T1's primary inductance. During Q1's off time, stored energy is partially discharged into C4 (output filter capacitor). Careful selection of a low ESR capacitor for C4 may provide satisfactory output ripple voltage making additional filter stages unnecessary.

C1 (input capacitor) may be reduced or eliminated if the MIC3172 is located near a low impedance voltage source.

Output Diode

The output diode allows T1 to store energy in its primary inductance (D2 nonconducting) and release energy into C4 (D2 conducting). The low forward voltage drop of a Schottky diode minimizes power loss in D2.

Frequency Compensation

A simple frequency compensation network consisting of R3 and C2 prevents output oscillations.

High impedance output stages (transconductance type) in the MIC2172/3172 often permit simplified loop-stability solutions to be connected to circuit ground, although a more conventional technique of connecting the components from the error amplifier output to its inverting input is also possible.

Voltage Clipper

Care must be taken to minimize T1's leakage inductance, otherwise it may be necessary to incorporate the voltage clipper consisting of D1, R4, and C3 to avoid second breakdown (failure) of the MIC3172's power NPN Q1.

Enable/Shutdown

The MIC3172 includes the enable/shutdown feature. When the device is shutdown, total supply current is less than 1μA. This is ideal for battery applications where portions of a system are powered only when needed. If this feature is not required, simply connect EN to V_{IN} or to a TTL high voltage.

Applications Information

Using the MIC3172 Enable Control (New Designs)

For new designs requiring enable/shutdown control, connect EN to a TTL or CMOS control signal (figure 3). The very low driver current requirement ensures compatibility regardless of the driver or gate used.

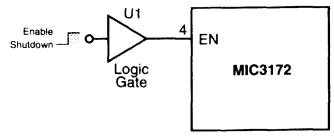


Figure 3. MIC3172 TTL Enable/Shutdown

Using the MIC3172 in LT1172 Applications

The MIC3172 can be used in most original LT1172 applications by adapting the MIC3172's enable/shutdown feature to the existing LT1172 circuit.

Unlike the LT1172 which can be shutdown by reducing the voltage on pin 2 (V_C) below 0.15V, the MIC3172 has a dedicated enable/shutdown pin. To replace the LT1172 with the MIC3172, determine if the LT1172's shutdown feature is used.

Circuits without Shutdown

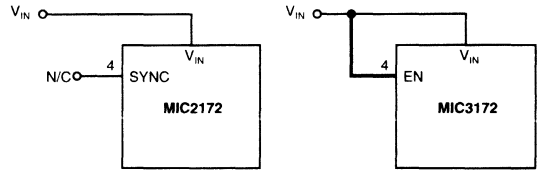


Figure 4. MIC2172/3172 Always Enabled

If the shutdown feature is not being used, connect EN to V_{IN} to continuously enable the MIC3172 or use an MIC2172 with SYNC open (figure 4).

Circuits with Shutdown

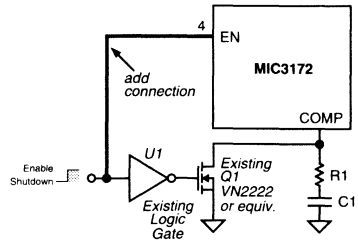


Figure 5. Adapting to the LT1172 Socket

If shutdown was used in the original LT1172 application, connect EN to a logic gate that produces a TTL logic-level output signal that matches the shutdown signal. The MIC3172

7

will be enabled by a logic-high input and shutdown with a logic-low input (figure 5). The actual components performing the functions of U1 and Q1 may vary according to the original application.

By using the MIC3172, U1 and Q1 shown in figure 5 can be eliminated, reducing the total components count.

Synchronizing the MIC2172

Using several unsynchronized switching regulators in the same circuit will cause beat frequencies to appear on the inputs and outputs. These beat frequencies can be very low making them difficult to filter.

Micrel's MIC2172 can be synchronized to a single master frequency avoiding the possibility of undesirable beat frequencies in multiple regulator circuits. The master frequency can be an external oscillator or a designated master MIC2172. The master frequency should be 1.05 to 1.20 times the slave's 100kHz nominal frequency to guarantee synchronization.

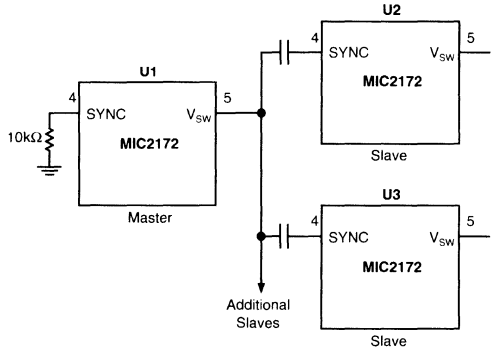


Figure 6. Master/Slave Synchronization

Figure 6 shows a typical application where several MIC2172s operate from the same supply voltage. U1's oscillator frequency is increased above U2's and U3's by connecting a resistor from SYNC to ground. U2-SYNC and U3-SYNC are capacitively coupled to the master's output (V_{SW}). The slaves lock to the negative (falling edge) of U1's output waveform.

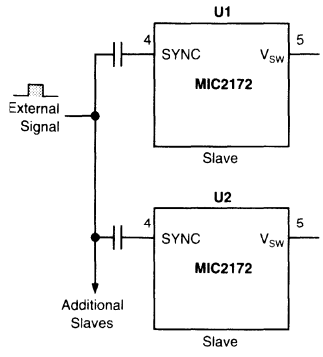


Figure 7. External Synchronization

Care must be exercised to insure that the master MIC2172 is always operating in continuous mode, otherwise the slaves may lock to the inductor's exponentially decaying sinusoid waveform.

Figure 7 shows how one or more MIC2172s can be locked to an external reference frequency. The slaves lock to the negative (falling edge) of the external reference waveform.

Soft Start

A diode-coupled capacitor from COMP to circuit ground slows the output voltage rise at turn on (figure 8).

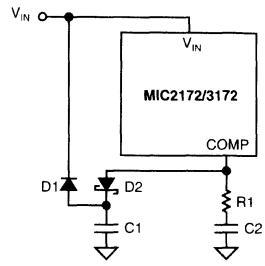


Figure 8. Soft Start

The additional time it takes for the error amplifier to charge the capacitor is corresponds to the time it takes the output to reach regulation. Diode D1 discharges C1 when V_{IN} is removed.

Current Limit

For designs demanding less output current than the MIC2172/3172 is capable of delivering, P GND 1 can be left open reducing the current capability of Q1 by one-half.

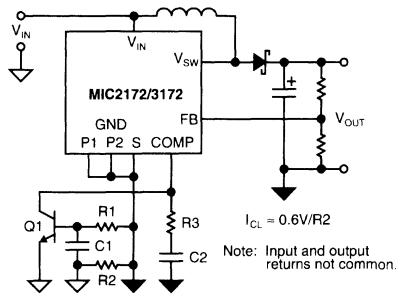


Figure 9. Current Limit

Alternatively, the maximum current limit of the MIC2172/3172 can be reduced by adding a voltage clamp to the COMP output (figure 9). This feature can be useful in applications requiring either a complete shutdown of Q1's switching action or a form of current fold-back limiting. This use of the COMP output does not disable the oscillator, amplifiers or other circuitry, therefore the supply current is never less than approximately 5mA.

Thermal Management

Although the MIC2172/3172 family contains thermal protection circuitry, for best reliability avoid prolonged operation with junction temperatures near the rated maximum.

The junction temperature is determined by first calculating the power dissipation of the device. For the MIC2172/3172, the total power dissipation is the sum of the device operating losses and power switch losses.

The device operating losses are the dc losses associated with biasing all of the internal functions plus the losses of the power switch driver circuitry. The dc losses are calculated from the supply voltage (V_{IN}) and device supply current (I_Q). The MIC2172/3172 supply current is almost constant regardless of the supply voltage (see "Electrical Characteristics"). The driver section losses (not including the switch) are a function of supply voltage, power switch current, and duty cycle.

$$P_{(bias+driver)} = (V_{IN}\, I_Q) + V_{IN}\left[I_{SW}\left(\frac{0.004+\delta}{50}\right)\right]$$

where:

$P_{(bias+driver)}$ = device operating losses
V_{IN} = supply voltage
I_Q = quiescent supply current
I_{SW} = power switch current
(see " Design Hints: Switch Current Calculations")
δ = duty cycle

$$\delta = \frac{V_{OUT} + V_F - V_{IN}}{V_{OUT} + V_F}$$

V_{OUT} = output voltage
V_F = D1 forward voltage drop

As a practical example refer to figure 1.

V_{IN} = 5.0V
I_Q = 0.006A
I_{SW} = 0.625A
δ = 60% (0.6)

Then:

$$P_{(bias+driver)} = (5 \times 0.006) + 5\left[0.625\left(\frac{0.004+0.6}{50}\right)\right]$$

$$P_{(bias+driver)} = 0.068W$$

Power switch dissipation calculations are greatly simplified by making two assumptions which are usually fairly accurate. First, the majority of losses in the power switch are due to on-losses. To find these losses, assign a resistance value to the collector/emitter terminals of the device using the saturation voltage versus collector current curves (see Typical Performance Characteristics). Power switch losses are calculated by modeling the switch after a resistor with the switch duty cycle modifying the average power dissipation.

$$P_{SW} = (I_{SW})^2\, R_{SW}\, \delta$$

From the Typical performance Characteristics:

$$R_{SW} = 1\Omega$$

Then:

$$P_{SW} = (0.625)^2 \times 1 \times 0.6$$
$$= 0.234W$$
$$P_{(total)} = 0.068 + 0.234$$
$$P_{(total)} = 0.302W$$

The junction temperature for any semiconductor is calculated using the following:

$$T_J = T_A + P_{(total)}\, \theta_{JA}$$

Where:

T_J = junction temperature
T_A = ambient temperature (maximum)
$P_{(total)}$ = total power dissipation
θ_{JA} = junction to ambient thermal resistance

For the practical example:

T_A = 70°C
θ_{JA} = 130°C/W (for plastic DIP)

Then:

$$T_J = 70 + 0.30 \times 130$$
$$T_J = 109°C$$

This junction temperature is below the rated maximum of 150°C.

Grounding

Refer to figure 10. Heavy lines indicate high current paths.

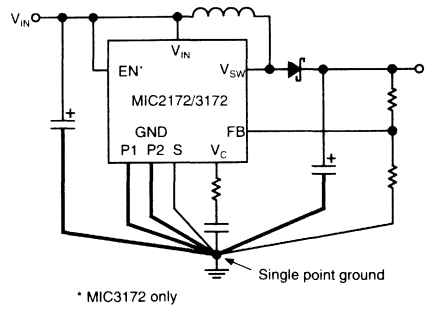


Figure 10. Single Point Ground

A single point ground is strongly recommended for proper operation.

The signal ground, compensation network ground, and feedback network connections are sensitive to minor voltage variations. The input and output capacitor grounds and power ground conductors will exhibit voltage drop when carrying large currents. Keep the sensitive circuit ground traces separate from the power ground traces. Small voltage variations applied to the sensitive circuits can prevent the MIC2172/3172 or any switching regulator from functioning properly.

7

Design Hints

Access to both the collector and emitter(s) of the NPN power switch makes the MIC2172/3172 extremely versatile and suitable for use in most PWM power supply topologies.

The most effective application for the MIC2172/3172 is probably the voltage step-up converter. When implemented with a transformer, it is commonly called a flyback converter. When no transformer is used, it is called a boost converter.

Boost Conversion

Refer to figure 11 for a typical boost conversion application where a +5 volt logic supply is available but +12V at 0.14A is required.

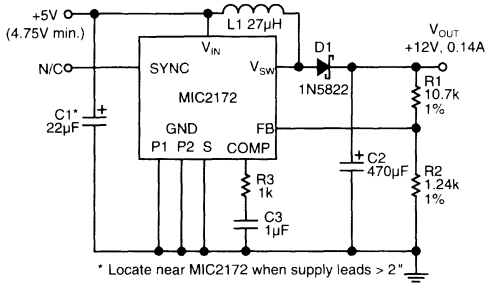


Figure 11. 5V to 12V Boost Converter

The first step in designing a boost converter is determining whether inductor L1 should operate in continuous or discontinuous mode.

When L1 discharges its current completely during the MIC2172/3172's off-time, it is operating in discontinuous mode. Discontinuous operation is generally chosen for low output power. When there is a demand for moderate output power, operation changes into continuous mode.

L1 is operating in continuous mode if it does not discharge completely before the MIC2172/3172 power switch is turned on again.

Discontinuous Mode Operation

Given the maximum output current, solve equation (1) to determine whether the device can operate in discontinuous mode without initiating the internal device current limit.

$$(1) \quad I_{OUT} \leq \frac{\left(\frac{I_{CL}}{2}\right) V_{IN}\, \delta}{V_{OUT}}$$

$$(1a) \quad \delta = \frac{V_{OUT} + V_F - V_{IN}}{V_{OUT} + V_F}$$

Where:

I_{CL} = internal switch current limit
I_{CL} = 1.25A when $\delta < 50\%$
$I_{CL} = 0.833\ (2 - \delta)$ when $\delta \geq 50\%$
(Refer to Electrical Characteristics.)

I_{OUT} = maximum output current
V_{IN} = minimum input voltage
δ = duty cycle
V_{OUT} = required output voltage
V_F = D1 forward voltage drop

For the example in figure 11.

I_{OUT} = 0.14A
I_{CL} = 1.147A
V_{IN} = 4.75V (minimum)
δ = 0.623
V_{OUT} = 12.0V
V_F = 0.6V

Then:

$$I_{OUT} \leq \frac{\left(\frac{1.147}{2}\right) \times 4.75 \times 0.623}{12}$$

$$I_{OUT} \leq 0.141A$$

This value is greater than the 0.14A output current requirement so we can proceed to find the inductance value of L1.

$$(2) \quad L1 \leq \frac{(V_{IN}\, \delta)^2}{2\, P_{OUT}\, f_{SW}}$$

Where:

$P_{OUT} = 12 \times 0.14 = 1.68W$
$f_{SW} = 1 \times 10^5 Hz$ (100kHz)

For our practical example:

$$L1 \leq \frac{(4.75 \times 0.623)^2}{2 \times 1.68 \times 1 \times 10^5}$$

$$\leq 26.062\mu H \text{ (use } 27\mu H)$$

Equation (3) solves for L1's maximum current value.

$$(3) \quad I_{L1(peak)} = \frac{V_{IN}\, T_{ON}}{L1}$$

Where:

$T_{ON} = \delta / f_{SW} = 6.23 \times 10^{-6}$ sec

$$I_{L1(peak)} = \frac{4.75 \times 6.23 \times 10^{-6}}{27 \times 10^{-6}}$$

$I_{L1(peak)}$ = 1.096A

Use a 27µH inductor with a peak current rating of at least 1.4A.

Discontinuous Mode Disadvantages

Applications where the inductor is operating in discontinuous mode will result in higher peak currents than a similar design which uses continuous mode. These peak currents can be difficult to filter when a low output ripple voltage is specified, often requiring more than one low ESR capacitor or a post filter comprised of a series inductor followed by an additional

capacitor. Additional input filtering may also be needed to prevent these currents from affecting other circuitry operating from the same supply. Furthermore, discontinuous-mode peak currents may be too close to the internal current limiting of the MIC2172/3172 in certain applications.

Continuous Mode Operation

Refer to figure 1.

Find the minimum inductor value that forces the inductor current to be continuous.

$$(4) \quad L1 > \frac{V_{IN}^2 \, \delta^2}{2 f_{SW} (I_{CL} V_{IN} \delta - P_{OUT})}$$

Where:

L1 = minimum inductance value (Henries)

From the application:

$V_{IN} = 4.75V$

$\delta = 0.623$

$f_{SW} = 1 \times 10^5$

$I_{CL} = 1.147A$

$V_{OUT} = 12V$

$I_{OUT} = 0.25A$

$P_{OUT} = V_{OUT} I_{OUT} = 3W$

Then:

$$L1 > \frac{4.75^2 \times 0.623^2}{2 \times 1 \times 10^5 (1.147 \times 4.75 \times 0.623 - 3)}$$

$$L1 \geq 111.1\mu H$$

A 120µH inductor was chosen for L1 to minimize the ripple current seen by the output capacitor C2.

The peak inductor current is:

$$(5) \quad I_{L1(peak)} = \frac{P_{OUT}}{V_{IN} \delta} + \frac{V_{IN} \delta}{f_{SW} 2 L1}$$

Then:

$$I_{L1(peak)} = \frac{3}{4.75 \times 0.623} + \frac{4.75 \times 0.623}{1 \times 10^5 \times 2 \times 1.2 \times 10^{-4}}$$

$$I_{L1} = 1.137A$$

L1's peak current rating should be at least 1.5A.

Switch Current Calculations

When finding the device junction temperature it is necessary to know the power switch average current.

Approximation for discontinuous mode:

$$(6) \quad I_{SW(avg)} = \frac{I_{L1(peak)}}{2}$$

Approximation for continuous mode:

$$(7) \quad I_{SW(avg)} = \frac{I_{OUT}}{1 - \delta}$$

Flyback Conversion

Refer to figure 12.

Whenever a low power converter requires voltage isolation or whenever the input voltage can be less than or greater than the output voltage, a flyback converter is the most economical design choice. As with the step-up converter the inductor (transformer primary) current can be continuous or discontinuous.

Discontinuous Flyback

When designing a discontinuous flyback, first determine whether the device can safely handle the peak primary current demand placed on it by the output power. Equation (8) finds the maximum duty cycle required for a given input voltage and output power. If the duty cycle is greater than 0.8 discontinuous operation cannot be used. Consider attempting continuous mode calculations.

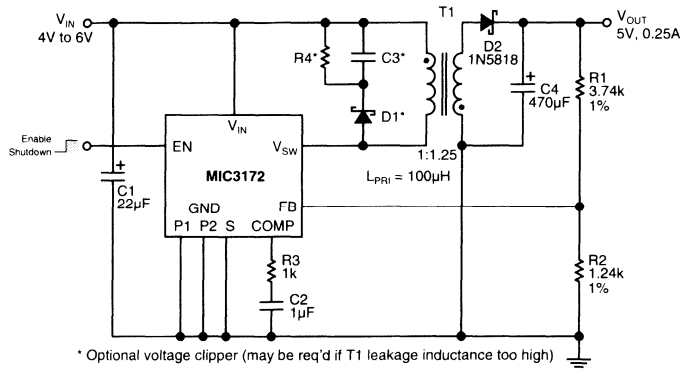


Figure 12. MIC3172 5V 0.25A Flyback Converter

(8) $$\delta \geq \frac{2\ P_{OUT}}{I_{CL}\ V_{IN(min)}}$$

For a practical example let:

$P_{OUT} = 5.0V \times 0.25A = 1.25W$

$V_{IN} = 4.0V$ to $6.0V$

$I_{CL} = 1.25A$ when $\delta < 50\%$

$0.833\ (2 - \delta)$ when $\delta \geq 50\%$

Then:

$$\delta \geq \frac{2 \times 1.25}{1.25 \times 4}$$

$\delta \geq 0.5$ (50%) Use 0.55.

The slightly higher duty cycle value is used to overcome circuit inefficiencies. A few iterations of equation (8) may be required if the duty cycle is found to be greater than 50%.

Calculate the maximum transformer turns ratio **a**, or N_{PRI}/N_{SEC}, that will guarantee safe operation of the MIC2172/3172 power switch.

(9) $$\mathbf{a} \leq \frac{V_{CE}\ F_{CE} - V_{IN(max)}}{V_{SEC}}$$

Where:

a = transformer maximum turns ratio

V_{CE} = power switch collector to emitter maximum voltage

F_{CE} = safety derating factor (0.8 for most commercial and industrial applications)

$V_{IN(max)}$ = maximum input voltage

V_{SEC} = transformer secondary voltage ($V_{OUT} + V_F$)

For the practical example:

$V_{CE} = 65V$ max. for the MIC2172/3172

$F_{CE} = 0.8$

$V_{SEC} = 5.6V$

Then:

$$\mathbf{a} \leq \frac{65 \times 0.8 - 6.0}{5.6}$$

$\mathbf{a} \leq 8.2143$

Next, calculate the maximum primary inductance required to store the needed output energy with a power switch duty cycle of 55%.

(10) $$L_{PRI} \leq \frac{0.5\ f_{SW}\ V_{IN(min)}^{\ 2}\ T_{ON}^{\ 2}}{P_{OUT}}$$

Where:

L_{PRI} = maximum primary inductance

f_{SW} = device switching frequency (100kHz)

$V_{IN(min)}$ = minimum input voltage

T_{ON} = power switch on time

Then:

$$L_{PRI} \leq \frac{0.5 \times 1\times10^{5} \times 4.0^{2} \left(5.5\times10^{-6}\right)^{2}}{1.25}$$

$L_{PRI} \leq 19.23\mu H$

Use an 18µH primary inductance to overcome circuit inefficiencies.

To complete the design the inductance value of the secondary is found which will guarantee that the energy stored in the transformer during the power switch on time will be completed discharged into the output during the off-time. This is necessary when operating in discontinuous-mode.

(11) $$L_{SEC} \leq \frac{0.5\ f_{SW}\ V_{SEC}^{\ 2}\ T_{OFF}^{\ 2}}{P_{OUT}}$$

Where:

L_{SEC} = maximum secondary inductance

T_{OFF} = power switch off time

Then:

$$L_{SEC} \leq \frac{0.5 \times 1\times10^{5} \times 5.6^{2} \times \left(4.5\times10^{-6}\right)^{2}}{1.25}$$

$L_{SEC} \leq 25.4\mu H$

Finally, recalculate the transformer turns ratio to insure that it is less than the value earlier found in equation (9).

(12) $$\mathbf{a} \leq \sqrt{\frac{L_{PRI}}{L_{SEC}}}$$

Then:

$$\mathbf{a} \leq \sqrt{\frac{1.8\times10^{-5}}{2.54\times10^{-5}}}$$

$\mathbf{a} \leq 0.84$ Use 0.8 (same as 1:1.25).

This ratio is less than the ratio calculated in equation (9). When specifying the transformer it is necessary to know the primary peak current which must be withstood without saturating the transformer core.

(13) $$I_{PEAK(pri)} = \frac{V_{IN(min)}\ T_{ON}}{L_{PRI}}$$

So:

$$I_{PEAK(pri)} = \frac{4.0 \times 5.5\times10^{-6}}{18\mu H}$$

$I_{PEAK(pri)} = 1.22A$

Now find the minimum reverse voltage requirement for the output rectifier. This rectifier must have an average current rating greater than the maximum output current of 0.25A.

$$(14)\quad V_{BR} \geq \frac{V_{IN(max)} + (V_{OUT}\,\mathbf{a})}{F_{BR}\,\mathbf{a}}$$

Where:

V_{BR} = output rectifier maximum peak reverse voltage rating

$\mathbf{a}$ = transformer turns ratio (0.8)

F_{BR} = reverse voltage safety derating factor (0.8)

Then:

$$V_{BR} \geq \frac{6.0 + (5.0 \times 0.8)}{0.8 \times 0.8}$$

$V_{BR} \geq 15.625V$

A 1N5817 will safely handle voltage and current requirements in this example.

Continuous Mode

As with the step-up converter, continuous-mode transformer operation can produce higher output powers than a similar discontinuous-mode design. First find the minimum duty cycle required to produce the necessary output power.

$$(15)\quad \delta \geq \frac{V_{SEC}\,I_{OUT}}{V_{IN(min)}\,I_{CL}}$$

For a practical example use the following design parameters for the circuit shown in the Typical Flyback Application.

$V_{SEC} = V_{OUT} + V_F = 5.6$ V

$I_{OUT} = 0.5A$

$V_{IN} = 4.0V$ to 6.0 V

$I_{CL} = 1.25A$ when $\delta < 50\%$

$0.833\ (2 - \delta)$ when $\delta \geq 50\%$

Then:

$$\delta \geq \frac{5.6 \times 0.5}{4.0 \times 1.25}$$

$\delta \geq 0.60$ Use 0.60

If the duty cycle is greater than 50%, equation (15) should be recalculated with the new value of I_{CL}.

Find the maximum turns ratio which allows safe operation of the device's power switch [equation (16)]. Also find the maximum turns ratio which will force the converter to operate in continuous mode [equation (17)].

$$(16)\quad \mathbf{a} \leq \frac{(V_{CE}\,F_{CE} - V_{IN(max)})}{V_{SEC}}$$

$$\mathbf{a} \leq \frac{65 \times 0.8 - 6.0}{5.6}$$

$\mathbf{a} \leq 8.2143$

and,

$$(17)\quad \mathbf{a} \leq \frac{V_{IN(min)}\,\delta}{V_{SEC}\,(1 - \delta)}$$

$$\mathbf{a} \leq \frac{4.0 \times 0.6}{5.6\,(1 - 0.6)}$$

$\mathbf{a} \leq 1.07$

Using a turns ratio of less than 1.07 will satisfy equations (15) and (16). To complete the turns ratio calculation it is necessary to find the minimum ratio which will allow the output rectifier (1N5817) to operate reliably.

$$(18)\quad \mathbf{a} \geq \frac{V_{IN(max)}}{F_{BR}\,V_{BR} - V_{OUT}}$$

Where:

$F_{BR} = 0.8$

$V_{BR} = 30$ V

$V_{OUT} = 5.0V$

$$\mathbf{a} \geq \frac{6.0}{0.8 \times 30 - 5.0}$$

$\mathbf{a} \geq 0.32$

Use a turns ratio of 1.0. To complete the design the minimum value of L_{SEC} must be found.

$$(19)\quad L_{SEC} > \frac{(V_{OUT} + V_F)\,(1 - \delta)^2}{f_{SW}\,2\,I_{OUT}}$$

$$L_{SEC} > \frac{5.6 \times 0.16}{1 \times 10^5 \times 2 \times 0.5}$$

$L_{SEC} > 8.96\mu H$

Again, to reduce the output ripple without costly additional filtering, a 100µH inductance value is chosen. The primary inductance in this example is the same as the secondary which will not always be the case. To find the primary inductance solve equation (20).

$$(20)\quad L_{PRI} = \mathbf{a}^2\,L_{SEC}$$

Forward Converters

Like the LT1172, Micrel's MIC2172/3172 can be used in several circuit configurations to generate an output voltage which is less than the input voltage (buck or step-down topology). Figure 13 shows the MIC2172 in a voltage step-down application. Because of the internal architecture of these devices, more external components are required to implement a step-down regulator than with other devices offered by Micrel (refer to the LM257x or LM457x family of buck switchers). However, for step-down conversion requiring a transformer (forward), the MIC2172/3172 is a good choice.

A 12V to 5V step-down converter using transformer isolation (forward) is shown in figure 14. Unlike the isolated flyback converter which stores energy in the primary inductance

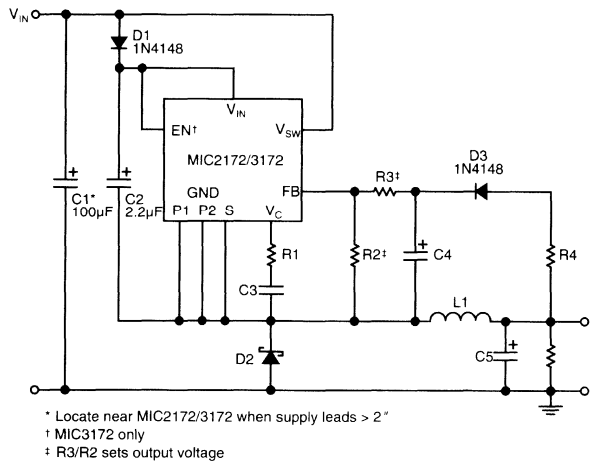


Figure 13. Step-Down or Buck Converter

during the controller's on-time and releases it to the load during the off-time, the forward converter transfers energy to the output during the on-time, using the off-time to reset the transformer core. In the application shown, the transformer core is reset by the tertiary winding discharging T1's peak magnetizing current through D2.

For most forward converters the duty cycle is limited to 50%, allowing the transformer flux to reset with only two times the input voltage appearing across the power switch. Although during normal operation this circuit's duty cycle is well below 50%, the MIC2172 (and MIC3172) has a maximum duty cycle capability of 90%. If 90% was required during operation (start-up and high load currents), a complete reset of the transformer during the off-time would require the voltage across the power switch to be ten times the input voltage. This would limit the input voltage to 6V or less for forward converter applications.

To prevent core saturation, the application given here uses a duty cycle limiter consisting of Q1, C4 and R3. Whenever the MIC3172 exceeds a duty cycle of 50%, T1's reset winding current turns Q1 on. This action reduces the duty cycle of the MIC3172 until T1 is able to reset during each cycle.

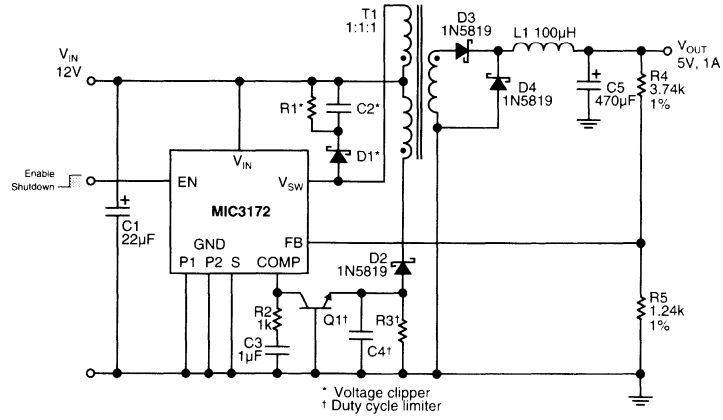


Figure 14. 12V to 5V Forward Converter

Specialized Application

Fluorescent Lamp Supply

An extremely useful application of the MIC3172 is generating an ac voltage for fluorescent lamps used as liquid crystal display back lighting in portable computers.

Figure 15 shows a complete power supply for lighting a fluorescent lamp. Transistors Q1 and Q2 together with capacitor C2 form a Royer oscillator. The Royer oscillator generates a sine wave whose frequency is determined by the series L/C circuit comprised of T1 and C2. Assuming that the MIC3172 and L1 are absent, and the transistors' emitters are grounded, circuit operation is described in "Oscillator Operation."

Oscillator Operation

Resistor R2 provides initial base current that turns transistor Q1 on and impresses the input voltage across one half of T1's primary winding (Pri 1). T1's feedback winding provides additional base drive (positive feedback) to Q1 forcing it well into saturation for a period determined by the Pri 1/C2 time constant. Once the voltage across C2 has reached its maximum circuit value, Q1's collector current will no longer increase. Since T1 is in series with Q1, this drop in primary current causes the flux in T1 to change and because of the mutual coupling to the feedback winding further reduces primary current eventually turning Q1 off. The primary windings now change state with the feedback winding forcing Q2 on repeating the alternate half cycle exactly as with Q1. This action produces a sinusoidal voltage wave form; whose amplitude is proportional to the input voltage, across T1's primary winding which is stepped up and capacitively coupled to the lamp.

Lamp Current Regulation

Initial ionization (lighting) of the fluorescent lamp requires several times the ac voltage across it than is required to sustain current through the device. It is the current through the lamp which is sampled and regulated by the MIC3172 to achieve a given intensity. The MIC3172 uses L1 to maintain a constant average current through the transistor emitters. It is the value of this current which controls the voltage amplitude of the Royer oscillator and maintains the lamp current. During the negative half cycle, lamp current is rectified by D3. During the positive half cycle, lamp current is rectified by D2 through R4 and R5. R3 and C5 filter the voltage dropped across R4 and R5 and present it to the MIC3172's feedback pin. The MIC3172 maintains a constant lamp current by adjusting its duty cycle to keep the feedback voltage at 1.24V. The intensity of the lamp is adjusted using potentiometer R5. The MIC3172 simply adjusts its duty cycle accordingly to bring the average voltage across R4 and R5 back to 1.24V.

On/Off Control

Especially important for battery powered applications, the lamp can be remotely or automatically turned off using the MIC3172's EN pin. The entire circuit draws less than 1µA while shutdown.

Efficiency

To obtain maximum circuit efficiency careful selection of Q1 and Q2 for low collector to emitter saturation voltage is a must. Inductor L1 should be chosen for minimal core and copper losses at the switching frequency of the MIC3172, and T1 should be carefully constructed from magnetic materials optimized for the output power required at the Royer oscillator frequency.

7

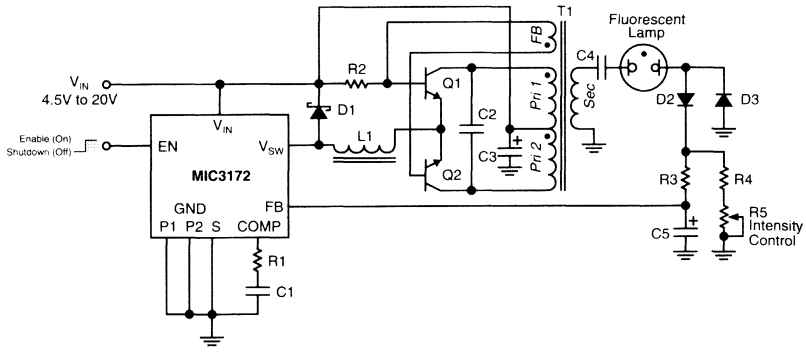


Figure 15. Fluorescent Lamp Supply

MIC3830/3831/3832/3833

Current Fed PWM Controllers

Preliminary Information–Production Q3 '94

General Description

The MIC3830 is a family of unique PWM controllers designed for use in current fed multiple output or push–pull switched mode power supply topologies. Current fed topologies, in which the inductor current as opposed to supply voltage is fed directly to the isolation transformer, eliminates the often encountered problem of core saturation created by shoot through or cross conduction of the power transistors. Stresses on the switching transistors are greatly reduced as well.

The MIC3830 and MIC3831 devices have one PWM stage capable of operating at 500kHz, and two output stages, Q and $\overline{Q}$, that operate at 1/4 the system frequency at a fixed 50% duty cycle. The MIC3832 and MIC3833 have Q and $\overline{Q}$ operating at 1/2 the system frequency and are ideally suited for the push-pull topology.

The MIC3830 and MIC3832 are high voltage devices, with an undervoltage lockout that doesn't allow startup until 16 V is supplied. The lockout voltage for these devices is 10V. The MIC3831 and MIC3833 are designed for lower voltage operation, with the startup voltage set at 8.4V and lockout at 7.6V.

The three output stages are hefty totem pole drivers, capable of supplying 1A peak current to startup a power FET, BJT or IGBT.

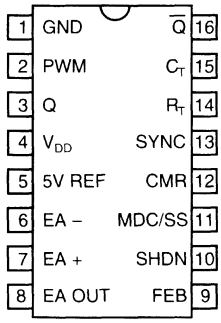
Features

- 7.6V to 21V or 10V to 21V Operation
- Undervoltage Lockout with Hysteresis
- 21V Zener Clamp on Supply Pin
- 0.5mA Max. Start-up Current
- Totem Pole Output Drive Stages
- 1A Peak Output Current
- 50ns Maximum Rise and Fall Times
- 500kHz PWM stage
- Voltage or Current Mode Control
- Soft Start Function
- Cycle–by–Cycle Current Limit
- Programmable Front Edge Current Pulse Blanking
- PWM Latch to Eliminate Multiple Outputs due to Noise or Ringing

Applications

- High Power Multiple Output Switched Mode Power Supplies/DC to DC Converters
- Current Fed Push-Pull Switched Mode Power Supplies/ DC to DC Converters

Pin Configuration



Ordering Information

Part Number	Temperature Range	Package
MIC3830AJ	–55°C to +125°C	16-pin CerDIP
MIC3830BN	–40°C to +85°C	16-pin Plastic DIP
MIC3830BWM	–40°C to +85°C	16-pin Wide SOIC
MIC3831AJ	–55°C to +125°C	16-pin CerDIP
MIC3831BN	–40°C to +85°C	16-pin Plastic DIP
MIC3831BWM	–40°C to +85°C	16-pin Wide SOIC
MIC3832AJ	–55°C to +125°C	16-pin CerDIP
MIC3832BN	–40°C to +85°C	16-pin Plastic DIP
MIC3832BWM	–40°C to +85°C	16-pin Wide SOIC
MIC3833AJ	–55°C to +125°C	16-pin CerDIP
MIC3833BN	–40°C to +85°C	16-pin Plastic DIP
MIC3833BWM	–40°C to +85°C	16-pin Wide SOIC

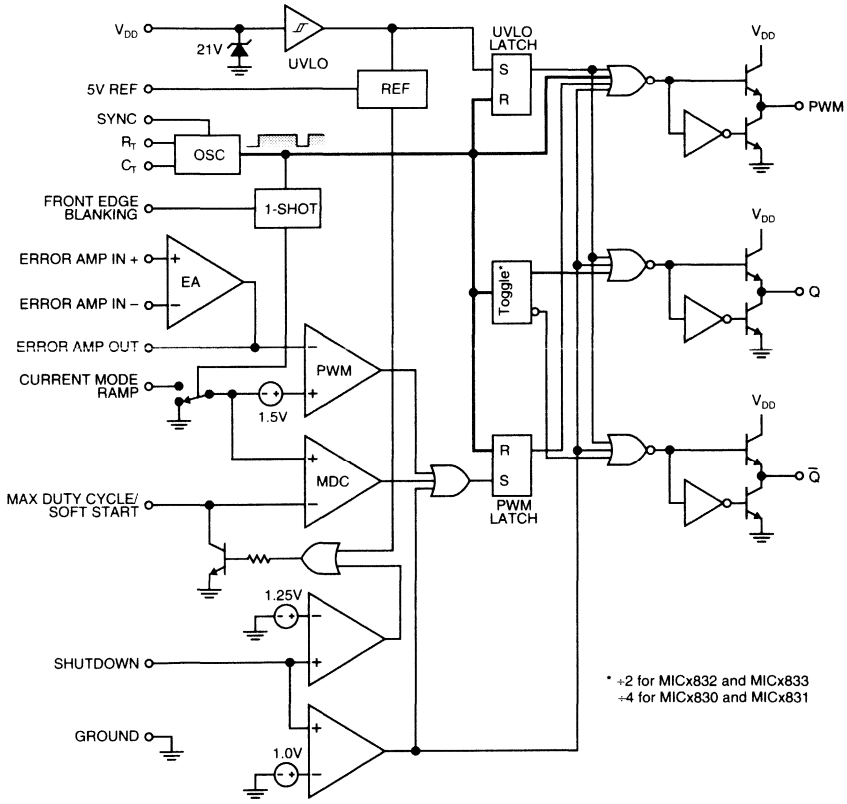
General Description (Continued)

Either current or voltage mode control can be used, giving the designer added flexibility in specifying the feedback components/compensation schemes.

These ICs have been "bullet–proofed" by the addition of UVLO with hysteresis, soft start with a programmable time constant, a PWM latch to eliminate multiple outputs due to noise or ringing, cycle–by–cycle current limit, and programmable front-edge blanking.

Front-edge blanking allows the systems designer to delay the onset of current sensing until all systems transients have died down. This is especially important when current mode control is used, as a spurious transient can result in system instabilities.

Block Diagram



7

Pin Description

Pin Number	Pin Name	Pin Function
1	GND	Ground
2	PWM	PWM Output: Totem pole output. Output signal is variable duty cycle.
3	Q	Switch Output: Totem pole output. Non-inverting 50% duty cycle output (180° out-of-phase with $\overline{Q}$).
4	V_{DD}	Supply Voltage Input: Clamped to 21V by internal Zener diode.
5	5V REF	5V Bandgap Reference Output
6	EA –	Inverting Error Amplifier Input: Biasing configuration (inverting vs. noninverting op amp configuration) determines power supply polarity.
7	EA +	Non-inverting Error Amplifier Input: See EA –.
8	EA OUT	Error Amplifier Output: Connect to the appropriate feedback network to adjust the open loop gain or frequency response.
9	FEB	Front Edge Blanking: Prevents initial system transients (due to device parasitics) from activating the overcurrent protection or causing system instabilities. Default length of the blanking pulse is approximately 100ns (FEB open). Capacitor to ground lengthens blanking time. Resistor to 5V REF decreases blanking time. (See Typical Performance Characteristics.)
10	SHDN	Overcurrent Shutdown: >1 V disables outputs, >1.25V initiates soft-start restart. For cycle-by-cycle current limiting, even in voltage-mode control applications, connect to current sense resistor. Ground if current sense is not used.
11	MDC/SS	Maximum Duty Cycle/Soft Start: Apply voltage to adjust maximum duty cycle. Adjust soft start by adding capacitance to increase turn-on time during initial start up or restart after overcurrent shutdown.
12	CMR	Current Mode Ramp: Feed point for inductor current when using current mode control. For voltage-mode control, connect to the C_T pin.
13	SYNC	Synchronization Input: Optional input from an external master clock (reference) signal. Normally synchronize all controllers to a single reference when a single system uses more than two controllers (power supplies). A high-level signal will prematurely terminate the voltage ramp on C_T.
14	R_T	Oscillator Timing Resistor
15	C_T	Oscillator Timing Capacitor
16	$\overline{Q}$	Switch Output: Totem pole output. Inverting 50% duty cycle output (180° out-of-phase with Q).

Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{DD}	21V
Source/Sink Load Current	1A
Maximum Supply (Zener) Current	50mA
Junction Temperature	150°C
Lead Temperature, Soldering	260°C, 10s
θ_{JA}CerDIP	100°C/W
θ_{JA}Plastic DIP	130°C/W

Operating Ratings

Storage Temperature Range	–65°C to +150°C
Operating Temperature Range	–40°C to +85°C
Reference Load Current	25mA
Supply Voltage (V_{DD}): MIC3830/3832	16V to 21V
Supply Voltage (V_{DD}): MIC3831/3833	7.6V to 21V
Oscillator Frequency Range	10kHz to 500kHz
Oscillator Timing Resistor	1kΩ to 100kΩ
Oscillator Timing Capacitor	2.2nF to 0.01µF
Available Deadtime Range	150ns to 4µs

Electrical Characteristics(Note 2)

T_A = –40°C to +85°C, V_{DD} = 15V, f = 52kHz unless otherwise specified.

Parameter	Conditions	Min	Typical	Max	Units
Reference Section					
Output Voltage	I_o = 1mA, T_A = 25°C	4.90	5.0	5.10	V
Input Regulation	V_{CC} = 12V to 25V		2.0	20	mV
Output Regulation	I_O = 1mA to 20mA		3.0	25	mV
Temperature Stability			–0.2		mV/°C
Total Output Variation			50		mV
Output Noise Voltage	f = 10Hz to 10kHz, T_A = 25°C		50		µV
Long Term Stability	T_A = 125°C, 1000hrs.		5.0		mV
Output Short Circuit Current	V_{REF} = 0	25	60	160	mA
Oscillator Section					
Frequency	T_A = 25°C	47	52	57	kHz
Voltage Stability	V_{CC} = 12V to 25V		0.5		%
Amplitude			1.7		V_{P-P}
Discharge Current	T_A = 25°C –40°C to +85°C		5 6		mA mA
Error Amplifier Section					
Input Offset Voltage		–15	±2	15	mV
Input Bias Current			0.6	3.0	µA
Input Offset Current			0.1	1.0	µA
Open Loop Gain	1V < V_O < 4V	60	95		dB
CMRR	1.5V < V_{CM} < 5.5V	75	95		dB
PSRR	10V < V_{CM} < 30V	85	110		dB
Output Sink Current	$V_{PIN\ 8}$ = 1V	1.0	2.5		mA
Output Source Current	$V_{PIN\ 8}$ = 4V	–0.5	–1.3		mA
Output High Voltage	$I_{PIN\ 8}$ = –0.5mA	4.0	4.7	5.0	V
Output Low Voltage	$I_{PIN\ 8}$ = 1mA		0.5	1.0	V
Soft Start/Max Duty Cycle Section					
Bias Current			–1.2		µA
Discharge Current		1			mA
Duty Cycle Clamp Accuracy		40	50	60	%

7

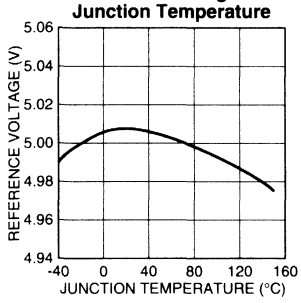
Parameter	Conditions	Min	Typical	Max	Units
Current Limit/Shutdown Section					
Bias Current			−1.2		µA
Current Limit Threshold		0.9	1.0	1.1	V
Shutdown Threshold		1.125	1.25	1.375	V
Delay to Output			200	300	ns
PWM Comparator Section					
Bias Current		5	−1	−5	µA
Duty Cycle Range		0		85	%
Delay to Output			200	300	ns
Front Edge Blanking					
Input Bias Current			−1		µA
Blanking Threshold		0.9	1.0	1.1	V
Output Sections					
Output Low Level	I_{SINK} = 20mA		0.1	0.4	V
	I_{SINK} = 200mA		1.5	2.2	V
Output High Level	I_{SOURCE} = 20mA	13			V
	I_{SOURCE} = 200mA	12	13.5		V
Rise Time	C_L = 1000pF		50	150	ns
Fall Time	C_L = 1000pF		50	150	ns
UVLO Saturation			0.7	1.1	V
Undervoltage Lockout Section					
Upper Threshold	MIC3830/32		16		V
	MIC3831/33		8.4		V
Lower Threshold	MIC3830/32		10		V
	MIC3831/33		7.6		V
Total Standby Current					
Startup Current			0.2	0.5	mA
Operating Supply			22		mA
V_{CC} Zener Voltage	I_{CC} = 25mA		21		V

Note 1 **Absolute Maximum Ratings** indicate limits beyond which damage to the device may occur. Electrical specifications do not apply when operating the device beyond its specified **Operating Ratings**.

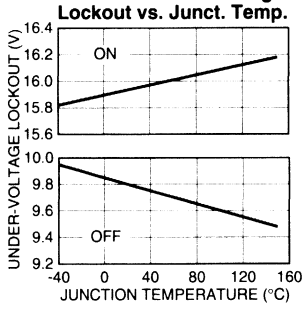
Note 2 Minimum and maximum Electrical Characteristics are 100% tested at T_A = 25°C and T_A = 85°C, and 100% guaranteed over the entire range. Typicals are characterized at 25°C and represent the most likely parametric norm.

Typical Performance Characteristics

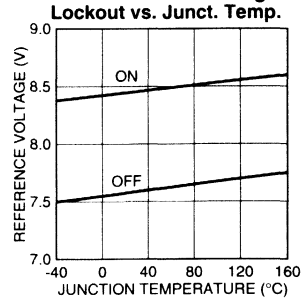
Reference Voltage vs. Junction Temperature



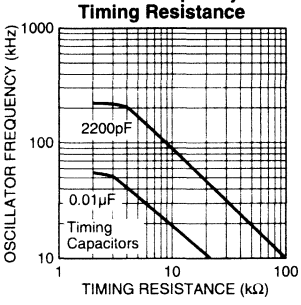
MIC3830/2 Undervoltage Lockout vs. Junct. Temp.



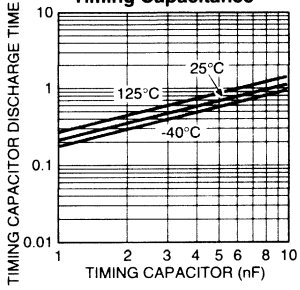
MIC3831/3 Undervoltage Lockout vs. Junct. Temp.



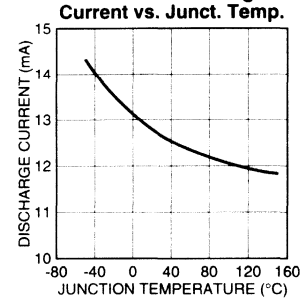
Oscillator Frequency vs. Timing Resistance



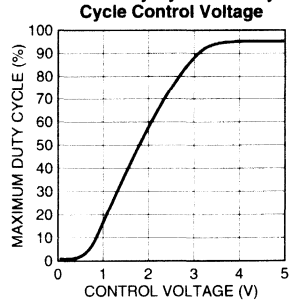
Discharge Time vs. Timing Capacitance



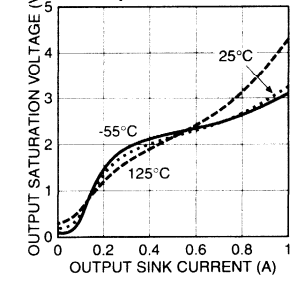
Oscillator Discharge Current vs. Junct. Temp.



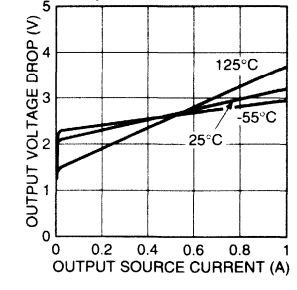
Max. Duty Cycle vs. Duty Cycle Control Voltage



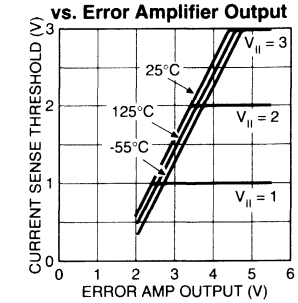
Output Saturation Voltage vs. Output Sink Current



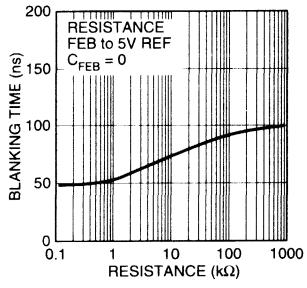
Output Voltage Drop vs. Output Source Current



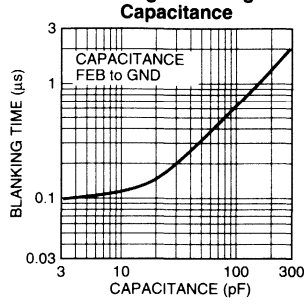
Current Sense Threshold vs. Error Amplifier Output



Front Edge Blanking vs. Resistance

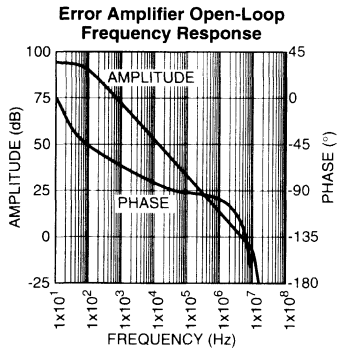


Front Edge Blanking vs. Capacitance



7

Typical Performance Characteristics



Applications Information

Functional Description (Refer to Functional Diagram)

The basic function of the MIC3830 can be described as follows: A sawtooth waveform is fed to the noninverting input of a PWM comparator where it is compared against the output of the error amplifier. The error amplifier compares the output voltage of the power supply with any externally supplied reference voltage (usually 1/2 the 5V reference). The output of the PWM comparator is a square wave, which drives the main output stage (PWM) of the controller.

The two 50% duty cycle stages are driven by the Q and $\overline{Q}$ outputs of one or two cascaded T-flip-flops. These are used to ensure that the two outputs are always 180° out of phase. The internal oscillator provides the T input to the flip–flops. These two outputs are primarily intended to drive power transistors for push-pull, half or full bridge inverter stages. They operate at 1/4 the total system frequency for the MIC3830 and MIC3831, and 1/2 the system frequency for the MIC3832 and MIC3833.

Each output stage is a sturdy totem pole configuration, with 1.0A peak current capability.

The individual stages/features of this controller are described in more detail as follows.

Oscillator

The oscillator stage serves two functions, first is to provide the linear sawtooth waveform fed to the PWM comparator in voltage mode control. Secondly, it toggles the flip-flop which provides the Q and $\overline{Q}$ outputs. The frequency of oscillation is externally programmed via the choice of timing resistor and capacitor. A nominal voltage of 3.6V appears on the R_T pin; the resulting current is then mirrored through the C_T pin which charges the timing capacitor and generates the linear ramp.

It is important to select an appropriate capacitor; at high frequencies effective series resistance, effective series inductance, dielectric loss and dielectric absorption all affect frequency stability and accuracy. RF capacitors such as silver mica, glass, polystyrene, or COG ceramics are recommended. High K ceramics should not be used.

Error Amplifier

The error amplifier is an op amp with a low impedance output that is used to sense output conditions and provide a DC output based on those conditions to the PWM comparator. The output of this stage is provided externally such that the closed loop gain or frequency response of the system can be tailored. The open loop gain of this stage is typically 95dB.

Voltage Reference

This section consists of a 5V bandgap reference internally trimmed to 2% accuracy. It provides not only an internal 5V reference, but can be used to supply 5V to other parts of the system.

PWM Comparator

This compares a sawtooth waveform with the output of the error amplifier. The sawtooth is generally the oscillator waveform on C_T in voltage mode control systems. In current mode control systems, it is often the inductor current waveform developed across a sense resistor connected from the main switch element to ground. Both systems result in a square wave output which, after being NOR'ed with the Max. Duty Cycle output (see below), is used to drive the main (PWM) output stage.

Overcurrent Sensing

Overcurrent sensing and shutdown is accomplished via an external sense resistor connected from the switching element (power transistor) to ground. This voltage is then fed into the noninverting input of two sensing comparators (SHDN). One inverting input is set to 1.0V internally; if the voltage sensed equals or exceeds 1.0V, the corresponding input to the logic gates is pulled low, and the PWM comparator output is overridden. This provides a current limited output. If 1.25V is exceeded, the other comparator is also tripped, activating the soft start feature. The part goes into full overcurrent shutdown.

Soft Start

This feature prevents damage due to large inrush currents generated upon initial application of system power or when the device attempts to restart after having been shut down by the current limit function. The latter feature operates in the same manner as the overcurrent sensing, except that it does not trip until the sensed voltage on the shutdown pin reaches 1.25V. When soft start is activated, the PWM comparator output duty cycle will increase slowly, with a time constant determined by the size of external capacitor chosen on the current limit/SS pin (Timing is $R_{TH}C$, where R_{TH} is the Thevenin equivalent resistance seen by this pin).

Max Duty Cycle

This feature, which uses the same pin as soft start (MDC/SS), provides another method of limiting duty cycle. The voltage seen by this pin determines the maximum duty cycle that can be obtained from the PWM output. As this feature can vary by as much as 15% over temperature, it is not recommended that it be used in place of a well designed feedback loop.

Undervoltage Lockout

Undervoltage lockout is accomplished by means of a Schmitt trigger in which the inverting input is tied to V_{CC} and the noninverting input is tied to an internally generated 16V (or 8.4V) supply. Once functional, the controller will not shut down until the supply drops to 10V (or 7.6V). A 21V zener clamp is used between the inverting input and ground.

Output Drivers

The output drivers are totem pole stages designed to sink and source 1.0A peak current. This peak current was chosen to provide the designer with the option of using bipolar, MOSFET, or IGBT switching elements. To minimize ringing on the output waveform, the series inductance seen by the drivers should be as low as possible. This can be accomplished by keeping the distance between the MIC3830 and the switching elements as short as possible,or using carbon composition resistors in series.

Front Edge Blanking

This feature provides a delay time prior to current sensing becoming active. This prevents the overcurrent sensing function from being falsely tripped by initial systems transients. It is most useful when using current mode control, as an initial systems transient can result in improper information controlling the feedback loop, and subsequent systems instabilities. Timing is set by the size of the capacitor and pullup resistor on this pin; it is roughly 0.35RC. An internal 20k and 15pF sets the delay to a nominal 100ns if this pin is left open. A resistor or short on this pin to V_{ref} can decrease the delay down to approximately 50ns. Conversely, a capacitor to ground can increase the delay. Refer to the electrical characteristics graphs for details.

Current vs. Voltage Mode Control

Current mode control is a method of using the output inductor current waveform (which happens to be a sawtooth), instead of generating a sawtooth waveform internally. It is preferable to voltage mode control as it provides more instantaneous feedback from the output stage, limits peak switching transistor current, removes one pole (the LC filter pole) from the output which simplifies compensation in the negative feedback stage, provides an automatic input voltage feedforward which results in good rejection of input line transients, and results in symmetrical flux excursion (for push-pull stage), eliminating the problem of core saturation. Current mode control is achieved in the MIC3830 by using the current mode ramp pin to input the inductor current.

If voltage mode control is desired, the current mode ramp pin is tied to the C_T pin. The internal oscillator is programmable up to 500kHz by selection of the appropriate resistor and capacitor(see graphs).

Construction Hints

As PWM controllers contain very sensitive on board comparators, careful prototyping techniques are required to prevent oscillations. Traditional solderless breadboards are a great source of noise, and should be completely avoided in all SMPS designs. Copper clad boards with a large area used as a single point ground plane makes a more than adequate substitute.

All timing and loop compensation capacitors and resistors should be kept as close to the leads of the MIC3830 as possible. Wire lengths along the high current path should be kept as short as possible, with appropriate wire gauges being used. Never socket the switching transistors as this can add to the voltage drop and power losses seen.

Circuit Topologies

Current Fed Multiple Output SMPS

Figure 3 illustrates this basic topology, which is basically a forward mode converter in which the center tap of the transformer sees inductor current, not a voltage. As described earlier, this eliminates the possibility of cross-conduction causing catastrophic core saturation of the transformer. As the MIC3830 has three output stages, no additional components (i.e. external flip–flops) are necessary to achieve the multiple outputs.

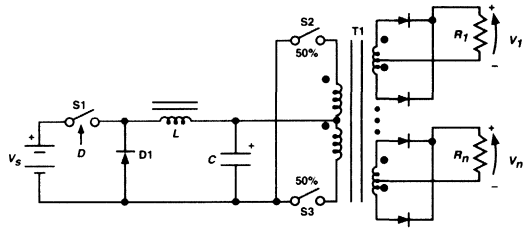


Figure 3: Current Fed Multiple Output Topology

Current Fed Push–Pull SMPS

Figure 4 illustrates this basic topology, which is simply a standard push-pull configuration in which the center tap of the primary is fed with an inductor current instead of a voltage. Push-pull topologies are often used in 100 W and above power supplies as they allow more efficient use of the transformer. The entire range of the B–H curve is used in a push – pull supply, so a transformer of 1/2 the size of one used in a single ended forward mode topology can be used. The space and cost advantages are obvious. This topology can be easily extended to a full bridge, often used in higher power supplies. Here, the two 50% duty cycle stages would be used to drive two FETs each, one for each half of the bridge.

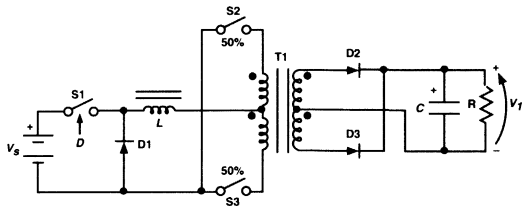


Figure 4: Current Fed Push Pull Topology

Design Example: An 100 kHz 100 W Current Fed Converter

A 5V, 20A max DC to DC converter was designed using the current fed push – pull configuration for increased safety and reduced size/transformer core area.

The input is an unregulated 14 to 32V DC supply, such as is commonly found in aircraft environments. This supply is fed to an MIC2951 low drop out regulator which acts as a housekeeping supply; supplying a steady, well regulated 12 V to the MIC3833.

The main PWM switching element is an IRF540, with gate drive provided by transformer T1. The two 50% duty cycle outputs each drive an IRF540 directly, which in turn drive their respective sides of T2's center tapped primary. The 1N6291A is a transzorb used to protect the FETs from spikes generated by the transformer.

Current mode control was chosen to simplify the stability analysis; with the 0.2Ω 5W resistor being used as the sensing element. As the maximum duty cycle at light loads is greater than 50%, the well characterized problem of subharmonic oscillations found when using current mode control was evident. A ramp was introduced at the sensing element to correct this; the 10kΩ and 470kΩ divider from the oscillator (ramp source) to the sensing element provide the proper slope. As a large resistor value was chosen to place on the oscillator pin, no buffering was necessary.

Front edge blanking was used to eliminate the need for a filter network around the sensing element, and reduce the possibility of turn-on transients causing system instabilities.

Four inexpensive capacitors were paralleled to lower ESR to an acceptable level of 80mΩ without adding too much size or cost.

Error amp compensation was performed using a simple lead – lag network. As current mode control was used, there was no need to compensate the LC filter pole.

A voltage of 2.5 V derived from the reference was fed to the Max duty cycle pin to provide a failsafe. This prevents the PWM out from attaining greater than 75% duty cycle.

Soft start was also implemented to allow slow turn-on in the event of a short circuit.

All magnetics were chosen to minimize losses at 100 kHz. T2 and L1 were wound using Seimen's new N87 material, and T1 using Magnetics Inc's P – type material. T2 and L1 were made using Seimen's new EFD core and bobbin assemblies, which were designed to reduce the height/form factor of the finished supply. T1 is a simple toroid.

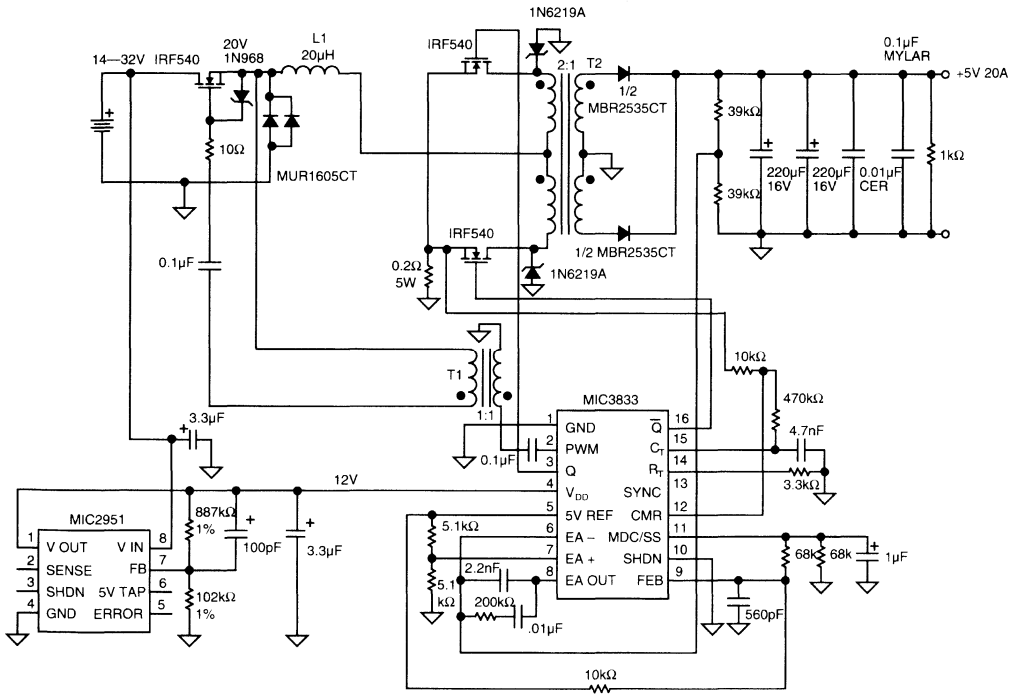


Figure 5: 100 W Current Fed Push – Pull DC to DC Converter (efficiency 75%)

Magnetics Design

T1 : Magnetics Inc # 41303 – TC, P material, Primary = 26 T 30 gauge wire, Secondary = 26 T 30 gauge wire

T2: Seimen's EFD30, N87 material. Primary = 20 T 20 gauge wire, Secondary = 10 T trifilar wound 20 gauge wire. Both are center tapped.

L1: Seimen's EFD20, N87 material. 13 T 20 gauge wire. Gap for 20 μH

MIC38C42/38HC42 Family

BiCMOS Current Mode Switching Regulator

General Description

The MIC38C42 family of devices are fixed frequency, high performance current mode PWM controllers. Although fully pin compatible with the bipolar 3842 family of controllers, the BiCMOS MIC38C42 family features key improvements that optimize performance to meet the need of today's SMPS designs. Start-up current has been reduced to 50µA typical. Operating currents also have been reduced to 4.0 mA typical with a 15V supply. Decreases in rise/fall times of the output drivers allows the use of larger FETs resulting in efficiency improvements. Rail to rail CMOS outputs also increase efficiency, especially at lower supply voltages.

These features, along with trimmed oscillator discharge current and bandgap reference, makes the MIC38C42/38HC42 family ideally suited for SMPS applications where low power loss, increased accuracy and stability, and reduced component count are essential.

Available in both 8-pin and 14-pin packages, the MIC38C42/38HC42 family offers the designer the choice between small package size and the increased performance and efficiency that comes with the separate grounding scheme available in a larger package.

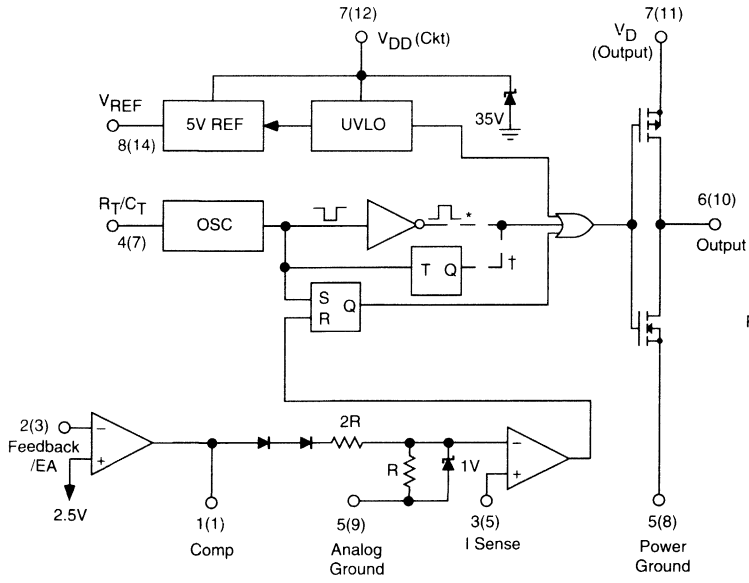
Features

- Fast output rise/fall times:
  - 40ns rise/30ns fall for the MIC38C42
  - 20ns rise/15ns fall for the MIC38HC42
- High performance, low power BiCMOS Process
- Ultra low start-up current (50µA typical)
- Low operating current (4mA typical)
- High output drive (1A peak current, HC version)
- CMOS outputs with rail-to-rail swing
- Current mode operation ≥500kHz
- Trimmed 5V bandgap reference
- Plug-in compatible with UC3842/3843/3844/3845(A)
- Trimmed oscillator discharge current
- UVLO with hysteresis
- Low cross-conduction currents

Applications

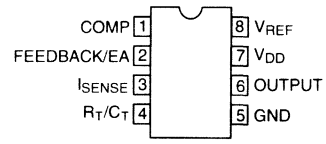
- Current mode off-line SMPS systems.
- Current mode DC to DC converters.

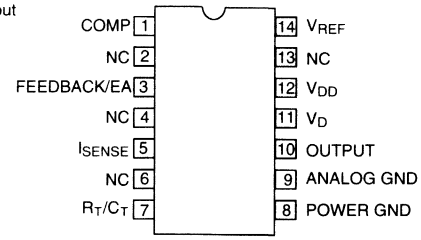
Functional Diagram



* MICx8C42, 43 / MICx8HC42, 43
† MICx8C44, 45 / MICx8HC44, 45

Pin Configurations





Ordering Information

Part Number	Temperature Range	Package
MIC18C42AJ	–55°C to +125°C	8-pin CerDIP
MIC18C43AJ	–55°C to +125°C	8-pin CerDIP
MIC18C44AJ	–55°C to +125°C	8-pin CerDIP
MIC18C45AJ	–55°C to +125°C	8-pin CerDIP
MIC18C42-1AJ	–55°C to +125°C	14-pin CerDIP
MIC18C43-1AJ	–55°C to +125°C	14-pin CerDIP
MIC18C44-1AJ	–55°C to +125°C	14-pin CerDIP
MIC18C45-1AJ	–55°C to +125°C	14-pin CerDIP
MIC38C42BN	–40°C to +85°C	8-pin Plastic DIP
MIC38C43BN	–40°C to +85°C	8-pin Plastic DIP
MIC38C44BN	–40°C to +85°C	8-pin Plastic DIP
MIC38C45BN	–40°C to +85°C	8-pin Plastic DIP
MIC38C42-1BN	–40°C to +85°C	14-pin Plastic DIP
MIC38C43-1BN	–40°C to +85°C	14-pin Plastic DIP
MIC38C44-1BN	–40°C to +85°C	14-pin Plastic DIP
MIC38C45-1BN	–40°C to +85°C	14-pin Plastic DIP
MIC38C42BM	–40°C to +85°C	8-pin SOIC
MIC38C43BM	–40°C to +85°C	8-pin SOIC
MIC38C44BM	–40°C to +85°C	8-pin SOIC
MIC38C45BM	–40°C to +85°C	8-pin SOIC
MIC38C42-1BM	–40°C to +85°C	14-pin SOIC
MIC38C43-1BM	–40°C to +85°C	14-pin SOIC
MIC38C44-1BM	–40°C to +85°C	14-pin SOIC
MIC38C45-1BM	–40°C to +85°C	14-pin SOIC

Part Number	Temperature Range	Package
MIC18HC42AJ	–55°C to +125°C	8-pin CerDIP
MIC18HC43AJ	–55°C to +125°C	8-pin CerDIP
MIC18HC44AJ	–55°C to +125°C	8-pin CerDIP
MIC18HC45AJ	–55°C to +125°C	8-pin CerDIP
MIC18HC42-1AJ	–55°C to +125°C	14-pin CerDIP
MIC18HC43-1AJ	–55°C to +125°C	14-pin CerDIP
MIC18HC44-1AJ	–55°C to +125°C	14-pin CerDIP
MIC18HC45-1AJ	–55°C to +125°C	14-pin CerDIP
MIC38HC42BN	–40°C to +85°C	8-pin Plastic DIP
MIC38HC43BN	–40°C to +85°C	8-pin Plastic DIP
MIC38HC44BN	–40°C to +85°C	8-pin Plastic DIP
MIC38HC45BN	–40°C to +85°C	8-pin Plastic DIP
MIC38HC42-1BN	–40°C to +85°C	14-pin Plastic DIP
MIC38HC43-1BN	–40°C to +85°C	14-pin Plastic DIP
MIC38HC44-1BN	–40°C to +85°C	14-pin Plastic DIP
MIC38HC45-1BN	–40°C to +85°C	14-pin Plastic DIP
MIC38HC42BM	–40°C to +85°C	8-pin SOIC
MIC38HC43BM	–40°C to +85°C	8-pin SOIC
MIC38HC44BM	–40°C to +85°C	8-pin SOIC
MIC38HC45BM	–40°C to +85°C	8-pin SOIC
MIC38HC42-1BM	–40°C to +85°C	14-pin SOIC
MIC38HC43-1BM	–40°C to +85°C	14-pin SOIC
MIC38HC44-1BM	–40°C to +85°C	14-pin SOIC
MIC38HC45-1BM	–40°C to +85°C	14-pin SOIC

Absolute Maximum Ratings

Zener Current 30mA

V_{DD} (8-pin) 20V

V_D (14-pin) 20V

Output Current (18C42/43/44/45, 38HC42/43/44/45) 0.5A

Output Current (18HC42/43/44/45, 38HC42/43/44/45) 1A

I_{SENSE}, FEEDBACK –0.3V to 5.5V

Ambient Temperature Range (T_A)

38C42/43/44/45, 38HC42/43/44/45 –40°C to +85°C

18C42/43/44/45, 18HC42/43/44/45 –55°C to +125°C

T_J Operating Temperature 150°C

Storage Temperature –65°C to 150°C

Operation at or above 18V may require special precautions (see Apps Info).

	UVLO Thresholds	
Duty Cycle	7.6V/8.4V	9V/14.5V
0 to 99%	MIC18C43/HC43 MIC38C43/HC43	MIC18C42/HC42 MIC38C42/HC42
0 to 50%	MIC18C45/HC45 MIC38C45/HC45	MIC18C44/HC44 MIC38C44/HC44

MIC18C/38C, 18HC/38HC	14 pin	8 pin
θ_{JA} (Plastic DIP)	90°C/W	100°C/W
θ_{JA} (Ceramic DIP)	110°C/W	125°C/W
θ_{JA} (SOIC)	145°C/W	170°C/W

Electrical Characteristics

Unless otherwise stated, these specifications apply for
$-55 \le T_A \le 125°C$ for MIC18C42/43/44/45, 18HC42/43/44/45
$-40 \le T_A \le 85°C$ for MIC38C42/43/44/45, 38HC42/43/44/45
V_{CC} = 15V (Note 4), R_T = 10kΩ, C_T = 3.3nF

		MIC18C42/43/44/45 MIC18HC42/43/44/45			MIC38C42/43/44/45 MIC38HC42/43/44/45			
Parameter	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Reference Section								
Output Voltage	T_A = 25°C, I_O = 1mA	4.95	5.00	5.05	4.90	5.00	5.10	V
Line Regulation	12V ≤ V_{DD} ≤ 18V, I_O = 5 µA (Note 6)		2	20		2	20	mV
Load Regulation	1 ≤ I_O ≤ 20 mA		1	25		1	25	mV
Temp. Stability	(Note 1)		0.2			0.2		mV/°C
Total Output Variation	Line, Load, Temp. (Note 1)	4.9		5.1	4.82		5.18	V
Output Noise Voltage	10Hz ≤ f ≤ 10kHz, T_A = 25°C (Note 1)		50			50		µV
Long Term Stability	T_A = 125 °C, 1000 Hrs. (Note 1)		5	25		5	25	mV
Output Short Circuit		–30	–80	–180	–30	–80	–180	mA
Oscillator Section								
Initial Accuracy	T_A = 25°C (Note 5)	49	52	55	49	52	55	kHz
Voltage Stability	12 ≤ V_{DD} ≤ 18V (Note 6)		0.2	1.0		0.2	1.0	%
Temp. Stability	$T_{MIN} \le T_A \le T_{MAX}$ (Note 1)		0.04			0.04		%/°C
Clock Ramp	T_A = 25°C, $V_{RT/CT}$ = 2V	8.1	8.4	8.7	8.1	8.4	8.7	mA
Reset Current	$T_A = T_{MIN}$ to T_{MAX}	7.5	8.4	9.3	7.5	8.4	9.3	mA
Amplitude	$V_{RT/CT}$ peak to peak		1.9			1.9		Vp–p
Error Amp Section								
Input Voltage	V_{COMP} = 2.5V	2.45	2.50	2.55	2.42	2.50	2.58	V
Input Bias Current	$V_{FEEDBACK}$ = 5.0V		–0.1	–1		–0.1	–2	µA
A_{VOL}	2 ≤ V_O ≤ 4V	65	90		65	90		dB
Unity Gain Bandwidth	(Note 1)	0.7	1.0		0.7	1.0		MHz
PSRR	12 ≤ V_{DD} ≤ 18V	60			60			dB
Output Sink Current	$V_{FEEDBACK}$ = 2.7V, V_{COMP} = 1.1V	2	14		2	14		mA
Output Source Current	$V_{FEEDBACK}$ = 2.3V, V_{COMP} = 5V	–0.5	–1		–0.5	–1		mA
V_{OUT} High	$V_{FEEDBACK}$ = 2.3V, R_L = 15k to ground	5	6.8		5	6.8		V
V_{OUT} Low	$V_{FEEDBACK}$ = 2.7V, R_L = 15k to V_{REF}		0.1	1.1		0.1	1.1	V
Current Sense								
Gain	(Notes 2 & 3)	2.85	3.0	3.15	2.85	3.0	3.15	V/V
MaximumThreshold	V_{COMP} = 5V (Note 2)	0.9	1	1.1	0.9	1	1.1	V
PSRR	12 ≤ V_{DD} ≤ 18V (Note 2)		70			70		dB
Input Bias Current			–0.1	–1		–0.1	–2	µA
Delay to Output			120	250		120	250	ns

7

Parameter	Test Conditions	MIC18C42/43/44/45 MIC18HC42/43/44/45 Min	Typ	Max	MIC38C42/43/44/45 MIC38HC42/43/44/45 Min	Typ	Max	Units
Output Section								
$R_{DS(ON)}$ 'C' High	I_{SOURCE} = 200 mA		20			20		Ω
$R_{DS(ON)}$ 'C' Low	I_{SINK} = 200 mA		11			11		Ω
$R_{DS(ON)}$ 'HC' High	I_{SOURCE} = 200 mA		10			10		Ω
$R_{DS(ON)}$ 'HC' Low	I_{SINK} = 200 mA		5.5			5.5		Ω
Rise Time: 'C' version	T_A = 25°C, C_L = 1 nF		40	80		40	80	ns
Fall Time: 'C' version	T_A = 25°C, C_L = 1 nF		30	60		30	60	ns
Rise Time: 'HC' version	T_A = 25°C, C_L = 1 nF		20	50		20	50	ns
Fall Time: 'HC' version	T_A = 25°C, C_L = 1 nF		15	40		15	40	ns
Under-Voltage Lockout								
Start Threshold	38C42/4, 18C42/4, 38HC42/4, 18HC42/4	13.5	14.5	15.5	13.5	14.5	15.5	V
	38C43/5, 18C43/5, 38HC43/5, 18HC43/5	7.8	8.4	9.0	7.8	8.4	9.0	V
Min. Operating Voltage	38C42/4, 18C42/4, 38C42/4, 18HC42/4	8	9	10	8	9	10	V
	38C43/5, 38C43/5, 38HC43/5, 38HC43/5	7.0	7.6	8.2	7.0	7.6	8.2	V
PWM Section								
Maximum Duty Cycle	38C42/3, 18C42/3, 38HC42/3, 18HC42/3	94	96		94	96		%
	38C44/5, 18C44/5, 38HC44/5, 18HC44/5	46	50		46	50		%
Minimum Duty Cycle				0			0	%
Total Standby Current								
Start-Up Current	V_{DD} = 13V for x8C42/44, x8HC42/44 V_{DD} = 7.5V for x8C43/45, x8HC43/45		50	150		50	200	µA
Operating Supply Current	$V_{FEEDBACK}$ = $V_{I\ SENSE}$ = 0V		4.0	6.0		4.0	6.0	mA
Zener Voltage (V_{DD})	I_{DD} = 25mA (Note 6)	30	37		30	37		V

Note 1: These parameters, although guaranteed, are not 100% tested in production.
Note 2: Parameter measured at trip point of latch with V_{EA} = 0.
Note 3: Gain defined as:

$$A = \frac{\Delta V_{PIN1}}{V_{TH}(I_{SENSE})} ; 0 \leq V_{TH}(I_{SENSE}) \leq 0.8V$$

Note 4: Adjust V_{DD} above the start threshold before setting at 15V.
Note 5: Output frequency equals oscillator frequency for the '8C42 and '8C43. Output frequency for the '8C44, and '8C45 equals one half the oscillator frequency.
Note 6: On 8-pin version, 20V is maximum input on pin 7, as this is also the supply pin for the output stage. On 14-pin version, 40V is maximum for pin 12 and 20V maximum for pin 11.

Application Information

The Advantage of Micrel's 38C4x/38HC4x

Designed to be completely compatible with the popular 384xA series current-mode PWM controllers, Micrel's BiCMOS process now provides the power supply engineer with several enhanced features making the 38C4x/38HC4x attractive for new as well as existing designs.

Start-up current has been reduced to an ultra-low 50µA (typical) allowing higher value bootstrap resistors to be used. Resistor wattage values can be reduced which saves PC board space.

Operating current has been reduced by more than half over the bipolar converter (4mA typical). Reduced current provides a cooler running part and reduces the amount of capacitance required to hold up the V_{DD} pin while the power supply starts. This reduced capacitance, coupled with the high valued bootstrap resistor, reduces the restarting frequency the power supply experiences during output overloads*. This feature increases the reliability of the supply to sustain abnormal conditions.

The most powerful enhancement offered by this converter is its rail-to-rail output drive stage. A complementary CMOS

Applications Information (continued)

pair makes up this stage making it an ideal choice for direct drive of conventional power MOSFET designs. The low $R_{DS(ON)}$ values together with the high I_{peak} capabilities allow the designer to drive MOSFETs with input capacitance of greater than 1000pF. In fact, the value of output capacity which can be handled is determined only by the rise/fall time requirements which are directly proportional to the output capacity and the power dissipation of the IC. Useful designs can now approach switching frequencies of 1MHz as long as these two criteria are kept in mind.

Caution:

Because of the CMOS construction of the output stage care must be exercised when operating near the absolute maximum rating of 20V. Due to circuit transients, voltages can exist in practical applications that can permanently damage the device. The use of a 0.1µF low ESR capacitor from V_{DD} (V_D for 14-pin version) to ground is recommended to reduce or eliminate these transients. To be effective this capacitor must be located as close to the MIC38C4X as possible. A good choice for this capacitor is a Wima film type series MKS2.

Care should be taken when designing high frequency converters to avoid capacitive and inductive coupling of the switching waveform into high impedance circuitry such as the error amplifier, oscillator, and current sense amplifier. Avoid long PC traces and component lead lengths. Locate oscillator and compensation circuitry near the IC. Use high frequency decoupling capacitors on V_{REF} and, if necessary, on V_{DD}. Return high di/dt currents directly to the source and use large area ground planes where possible.

500kHz MIC38C42 25W Buck DC-DC Converter

Upon application of at least 26 volts to the input, C5 is charged through R2 until the voltage V_{DD} is greater than the under-voltage-lockout of the MIC38C42. Output switching then begins with the turn on of Q1 via the gate drive transformer T1, charging the output filter capacitor C3 through L1.

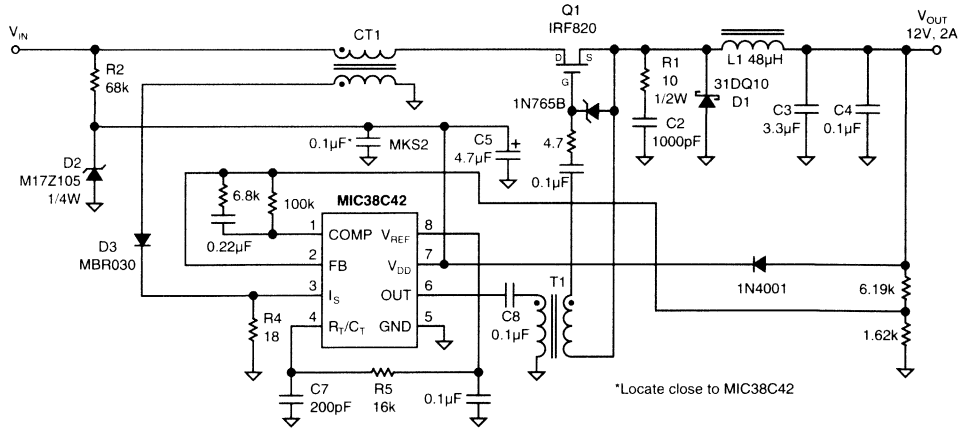
Current sense transformer CT1 implements current mode operation and cycle-by-cycle current limiting. This scheme eliminates the need for an inefficient sense resistor and the resulting level shift needed to reference the voltage to input ground.

Using a 100V Schottky for the catch diode D1 puts a lower V_F in the main current path and results in higher circuit efficiency than could be accomplished using an ultra-fast-recovery diode. The R1 and C2 combination suppresses parasitic oscillations from D1.

Using a high value inductance for L1 and a low ESR capacitor for C3 permits using a small capacitance for C3 while producing minimal output ripple. This inductance value also improves circuit efficiency by reducing the flux swing in L1.

Magnetic components were carefully chosen for minimal losses at 500kHz and contribute significantly to higher efficiency. CT1 and T1 are wound on Magnetics, Inc. P type material toroids. L1 is wound on a Siemens N49 EFD core.

*The power supply will restart whenever the output load increases beyond the design maximum. This reduces the voltage to the V_{DD} pin until it shuts the IC off. The bootstrap resistor then recharges the V_{DD} capacitor and the power supply operates again until V_{DD} falls. This cycle continues at a rate determined by the bootstrap resistor and V_{DD} capacitor.



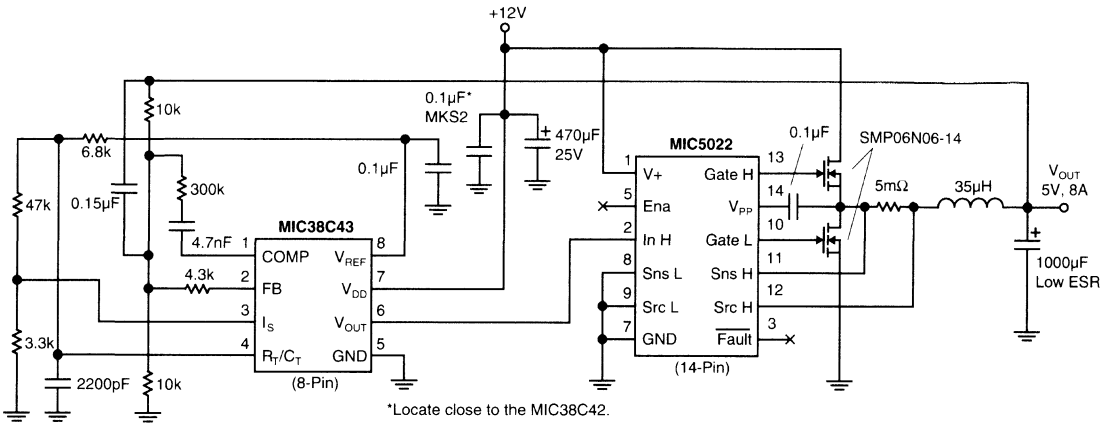
500kHz 25W Buck DC-DC Converter

Test	Conditions	Results
Line Regulation	V_{IN} = 26V to 80V, I_O = 2A	0.5%
Load Regulation	V_{IN} = 48V, I_O = 0.2A to 2A	0.6%
Efficiency	V_{IN} = 48V, I_O = 2A	90%
Output Ripple	V_{IN} = 48V, I_O = 2A (20MHz BW)	100mV

Symbol	Custom Coil[1]	ETS[2]
CT1	4923	ETS 92420
T1	4924	ETS 92418
L1	4925	ETS 92421

1. Custom Coils, Alcester, SD tel: (605) 934-2460
2. Energy Transformation Systems, Inc. tel: (415) 324-4949.

Applications Information (continued)



100kHz High Efficiency Synchronous Buck Rectifier

MIC631/32/33 and MIC641/42/43

Step-Up Switching Regulators

General Description

The MIC631/641, MIC632/642, and MIC633/643 are fixed frequency, hysteretic-mode, step-up (boost) regulators. Switching at 50kHz, and requiring only two external components, these controllers form a completely functional, fully regulated dc-dc converter. Ideal for battery powered operation, these parts operate from a supply voltage of 2V to 16.5V and feature a low quiescent current of typically 120µA with V_{OUT} = 5V.

The MIC63x controller is useful for low power (≤ 150mW) applications and has a charge pump output on pin 6 for external voltage doubling/inverting. The MIC64x is intended for higher power applications (up to 10W) where pin 6 is designed to drive an external MOSFET.

Designed to be completely compatible with the MAX631/641 family of controllers the MIC631/641 is also offered in a 3.3V output version and features full thermal shutdown when the junction temperature exceeds 150°C. Furthermore, the oscillator frequency dependency on V_{OUT} has been greatly reduced resulting in higher output power capabilities at low values of V_{OUT}.

The MIC631/641-3.3, MIC631/641, MIC632/642, and MIC633/643 are +3.3V, +5V, +12V, and +15V fixed output devices. All parts of this family feature V_{OUT} programming from 1.275V to 16.5V with the addition of two external resistors. Higher output voltages can be accommodated using the MIC64x and an external FET with appropriate $V_{DS(MAX)}$ rating (see Applications Information).

Available in 8-pin SOIC or DIP, the MIC631/632/633 and MIC641/642/643 are offered in two temperature ranges: –40°C to +85°C or –55°C to +125°C.

Features

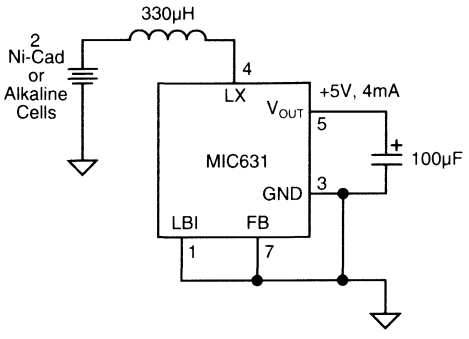
- Pin-for-pin plug-in replacement for the MAX631/632/633 and MAX641/642/643
- Fixed +3.3V, +5V, +12V, +15V output voltage
- Adjustable output using 2 external resistors
- Minimum parts count (2 external components)
- Typical operating current reduced to 120µA
- Thermal shutdown
- Improved 4% output voltage tolerance over temperature
- Charge pump output (MIC63x)
- External MOSFET gate drive (MIC64x)
- Low battery detect input
- Low battery output

Applications

- Hand-held computers
- Laptop computers
- Cellular phones
- Toys
- DC-DC converters
- Distributed power

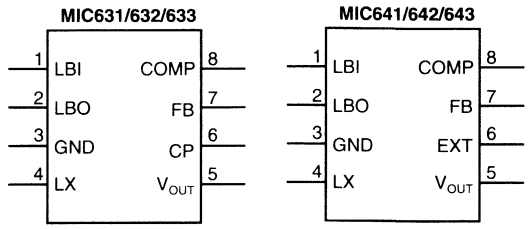
7

Typical Application



+5V Battery Operated Converter

Pin Configuration



Top View

Ordering Information MIC63x

Part Number	Temperature Range	Voltage	Package
MIC631-3.3BN	–40°C to +85°C	3.3V	8-pin Plastic DIP
MIC631-3.3BM	–40°C to +85°C	3.3V	8-pin SOIC
MIC631-3.3AJ	–55°C to +125°C	3.3V	8-pin Ceramic DIP
MIC631BN	–40°C to +85°C	5.0V	8-pin Plastic DIP
MIC631BM	–40°C to +85°C	5.0V	8-pin SOIC
MIC631AJ	–55°C to +125°C	5.0V	8-pin Ceramic DIP
MIC632BN	–40°C to +85°C	12.0V	8-pin Plastic DIP
MIC632BM	–40°C to +85°C	12.0V	8-pin SOIC
MIC632AJ	–55°C to +125°C	12.0V	8-pin Ceramic DIP
MIC633BN	–40°C to +85°C	15.0V	8-pin Plastic DIP
MIC633BM	–40°C to +85°C	15.0V	8-pin SOIC
MIC633AJ	–55°C to +125°C	15.0V	8-pin Ceramic DIP

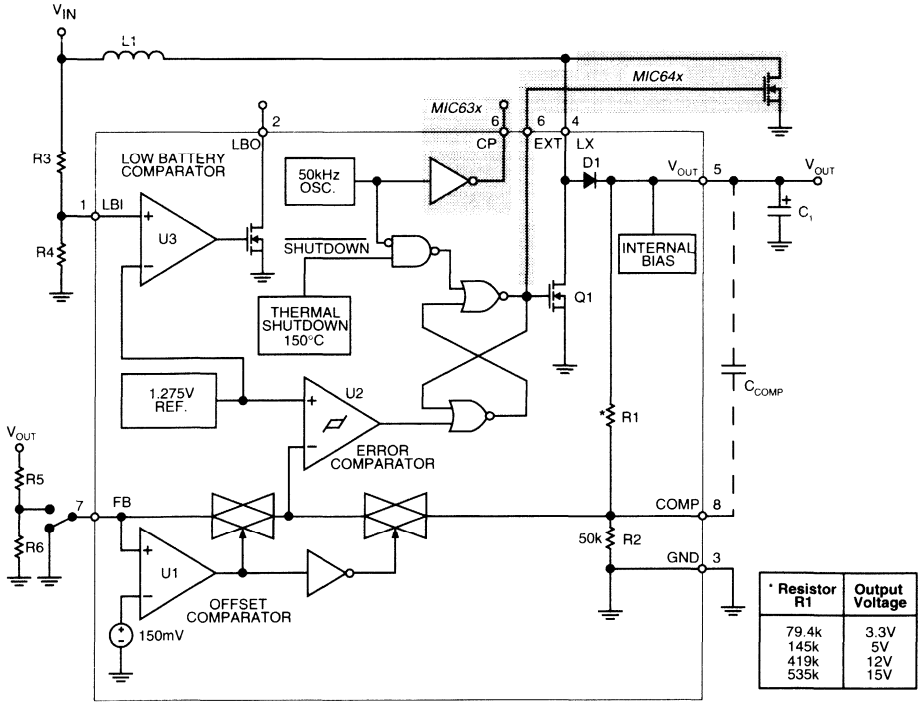
Ordering Information MIC64x

Part Number	Temperature Range	Voltage	Package
MIC641-3.3BN	–40°C to +85°C	3.3V	8-pin Plastic DIP
MIC641-3.3BM	–40°C to +85°C	3.3V	8-pin SOIC
MIC641-3.3AJ	–55°C to +125°C	3.3V	8-pin Ceramic DIP
MIC641BN	–40°C to +85°C	5.0V	8-pin Plastic DIP
MIC641BM	–40°C to +85°C	5.0V	8-pin SOIC
MIC641AJ	–55°C to +125°C	5.0V	8-pin Ceramic DIP
MIC642BN	–40°C to +85°C	12.0V	8-pin Plastic DIP
MIC642BM	–40°C to +85°C	12.0V	8-pin SOIC
MIC642AJ	–55°C to +125°C	12.0V	8-pin Ceramic DIP
MIC643BN	–40°C to +85°C	15.0V	8-pin Plastic DIP
MIC643BM	–40°C to +85°C	15.0V	8-pin SOIC
MIC643AJ	–55°C to +125°C	15.0V	8-pin Ceramic DIP

Pin Description

Pin Number	Pin Name	Pin Function
1	LBI	Low Battery Detect Input: Compares this voltage to the internal reference (1.275V). When LBI is less than the reference, LBO switches to a low state capable of sinking 50mA.
2	LBO	Low Battery Detect Output: Open drain FET which is active (sinking current) when LBI is less than 1.275V.
3	GND	Ground
4	LX	Storage Inductor Connection: Internally connected to the drain of the power switching FET
5	V_{OUT}	Internal Rectifier Diode (Cathode): Connect directly to the output filter capacitor.
6 (MIC63x)	CP	Charge Pump Output (MIC63x only): Buffered (and inverted) internal oscillator signal. Can be used for voltage inverting and/or doubling of V_{OUT}.
6 (MIC64x)	EXT	External Output (MIC64x only): Internally connected to the gate of the power FET and is used to drive an external FET to achieve higher output power.
7	FB	Feedback Input: Dual purpose. If grounded, the output voltage is the fixed value set by internal feedback resistors. The output voltage is adjustable when FB is connected to an external resistor divider between V_{OUT} and GND.
8	COMP	Compensation Input: May be used with a capacitor from V_{OUT} to improve transient response of V_{OUT} and reduce peak to peak output ripple voltage.

Block Diagram



Absolute Maximum Ratings

Supply Voltage (V_{OUT}) ..... +18V
Output Voltage (LX, LBO) ..... +18V
Input Voltage
(LBI, FB, LBO, COMP) ..... –0.3V to (V_{OUT} +0.3V)
Output Current
LX ..... 450mA Peak
LBO 50mA
Lead Temperature (Soldering, 10 sec) ..... +300°C

Operating Ratings

Power Dissipation
Plastic DIP (derate 8.33mW/°C above +50°C) 625mW
SOIC (derate 6mW/°C above +50°C) 450mW
CerDIP (derate 8mW/°C above +50°C) 800mW
Operating Ambient Temperature Range
MIC6xxBN ..... –40°C to +85°C
MIC6xxBM ..... –40°C to +85°C
MIC6xxAJ ..... –55°C to +125°C

Electrical Characteristics MIC63x

Unless otherwise specified all limits guaranteed for T_J = 25°C.

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Operating Voltage Range	Voltage at V_{OUT}, –55°C < T_J < +125°C	2.0		16.5	V
	Startup Voltage	Voltage at V_{OUT}				
		T_A = +25°C	1.5			V
		–55°C < T_J < +125°C	1.8			V
I_S	Supply Current	LX off, –55°C < T_J < +125°C				
		V_{OUT} = 3.3V, MIC631-3.3		100	200	µA
		V_{OUT} = +5V, MIC631		120	250	µA
		V_{OUT} = +12V, MIC632		250	500	µA
		V_{OUT} = +15V, MIC633		300	600	µA
	Reference Voltage (Internal)	T_A = +25°C	1.263	1.275	1.287	V
		–55°C < T_J < +125°C	1.250	1.275	1.300	V
	V_{OUT} Voltage	No Load, FB = Gnd, –55°C < T_J < +125°C				
		MIC631-3.3	3.16	3.3	3.47	V
		MIC631	4.80	5.0	5.20	V
		MIC632	11.52	12.0	12.48	V
		MIC633	14.40	15.0	15.60	V
	Line Regulation	0.5V_{OUT} < +V_{SOURCE}, V_{OUT}		0.08		%V_{OUT}
	Load Regulation	V_S = 0.5V_{OUT}, P_{OUT} = 0mW to 150mW		0.2		%V_{OUT}
f_O	Oscillator Frequency	V_{OUT} = +3.3V, MIC631-3.3	46	50	54	kHz
		V_{OUT} = +5V, MIC631	46	50	54	kHz
		V_{OUT} = +12V, MIC632	46	50	54	kHz
		V_{OUT} = 15V, MIC633	46	50	54	kHz
	Oscillator Frequency Temperature Coefficient			–20		Hz/°C
	Oscillator Duty Cycle	MIC631-3.3, V_{OUT} = +3.3V	40	50	60	%
		MIC631, V_{OUT} = +5V	40	50	60	%
		MIC632, V_{OUT} = +12V	40	50	60	%
		MIC633, V_{OUT} = +15V	40	50	60	%
R_{ON}	LX On Resistance	I_X = 100mA, V_{OUT} = +5V		5	12	Ω
		V_{OUT} = +15V		3	7	Ω
I_{LX}	LX Leakage Current	V_4 = +16.5V, T_A = +25°C		0.1	1.0	µA
		V_4 = +16.5V, –55°C < T_J < +125°C			30	µA
V_F	Diode Forward Voltage	I_F = 100mA		0.8	1.0	V
	CP On Resistance	V_{OUT} = +5V, I_{OUT} = ±10mA (All Devices)		70	140	Ω
		V_{OUT} = +15V, I_{OUT} = ±30mA (All Devices)		30	60	Ω
I_{FB}	FB Input Bias Current			10	25	nA
V_{LBI}	Low Battery Input Threshold		1.250	1.275	1.300	V
I_{LBI}	Low Battery Input Bias Current			10	25	nA

I_{LBO}	Low Battery Output Current	V_2 = +0.4V, V_1 = +1.1V, V_{OUT} = 5V −55°C < T_J < +125°C	 300	600		µA µA
I_{LBOL}	Low Battery Output Leakage Current	V_2 = +16.5V, V_1 = +1.4V		0.01	3.0	µA

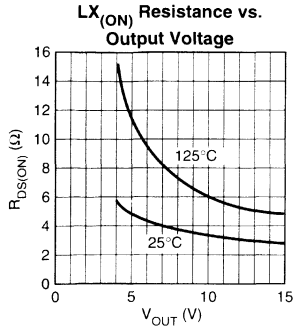
Electrical Characteristics MIC64x

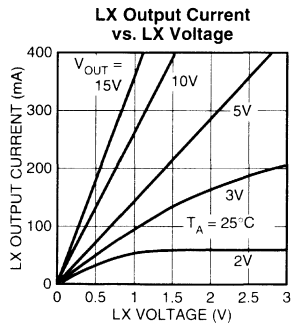
Unless otherwise specified all limits guaranteed for T_J = 25°C.

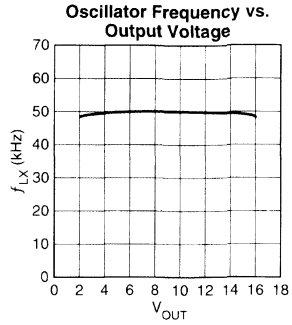
Symbol	Parameter	Condition	Min	Typ	Max	Units
	Operating Voltage Range	Voltage at V_{OUT}, −55°C < T_J < +125°C	2.0		16.5	V
	Startup Voltage	Voltage at V_{OUT} T_A = +25°C −55°C < T_J < +125°C	 1.5 1.8			 V V
I_S	Supply Current	LX off, −55°C < TJ < +125°C VOUT = 3.3V, MIC641-3.3 V_{OUT} = +5V, MIC641 V_{OUT} = +12V, MIC642 V_{OUT} = +15V, MIC643		 100 120 250 300	 200 250 500 600	 µA µA µA µA
	Reference Voltage (Internal)	T_A = +25°C −55°C < T_J < +125°C	1.264 1.250	1.275 1.275	1.287 1.300	V V
	V_{OUT} Voltage	No Load, FB = Gnd, −55°C < T_J < +125°C MIC641-3.3 MIC641 MIC642 MIC643	 3.16 4.80 11.52 14.40	 3.3 5.0 12.0 15.0	 3.47 5.20 12.48 15.60	 V V V V
	Line Regulation	0.5V_{OUT} < +V_{SOURCE} , V_{OUT}		0.08		%V_{OUT}
	Load Regulation	V_S = 0.5V_{OUT}, P_{OUT} = 0mW to 150mW		0.2		%V_{OUT}
f_O	Oscillator Frequency	V_{OUT} = +3.3V, MIC641-3.3 V_{OUT} = +5V, MIC641 V_{OUT} = +12V, MIC642 V_{OUT} = 15V, MIC643	46 46 46 46	50 50 50 50	54 54 54 54	kHz kHz kHz kHz
	Oscillator Frequency Temperature Coefficient			−20		Hz/°C
	Oscillator Duty Cycle	MIC641-3.3, V_{OUT} = +3.3V MIC641, V_{OUT} = +5V MIC642, V_{OUT} = +12V MIC643, V_{OUT} = +15V	40 40 40 40	50 50 50 50	6 0 60 60 60	% % % %
	EXT Output Resistance	V_{OUT} = +5V, I_{OUT} = ±10mA V_{OUT} = +15V, I_{OUT} = ±10mA		70 30	140 60	Ω Ω
t_{ON}, t_{OFF}	EXT Switching Time	C_L = 330pF, V_{OUT} = +5V C_L = 330pF, V_{OUT} = +15V		160 125		ns ns
R_{ON}	LX On Resistance	I_X = 100mA, V_{OUT} = +5V V_{OUT} = +15V		5 3	12 7	Ω Ω
I_{LX}	LX Leakage Current	V_4 = +16.5V, T_A = +25°C V_4 = +16.5V, −55°C < T_J < +125°C		0.1	1.0 30	µA µA
V_F	Diode Forward Voltage	I_F = 100mA		0.8	1.0	V
I_{FB}	FB Input Bias Current			10	25	nA
V_{LBI}	Low Battery Input Threshold		1.250	1.275	1.300	V
I_{LBI}	Low Battery Input Bias Current			10	25	nA
I_{LBO}	Low Battery Output Current	V_2 = +0.4V, V_1 = +1.1V, V_{OUT} = 5V −55°C < T_J < +125°C	 300	600		µA µA
I_{LBOL}	Low Battery Output Leakage Current	V_2 = +16.5V, V_1 = +1.4V		0.01	3.0	µA

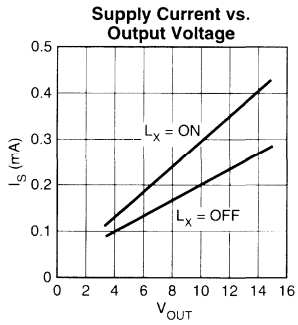
7

Typical Characteristics









Switching Waveforms

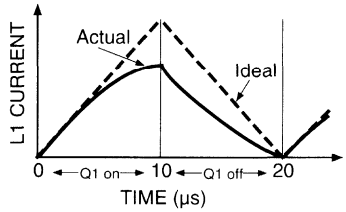


Figure 1. Inductor Current

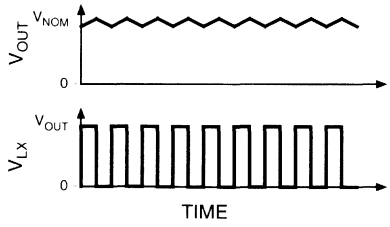


Figure 2a. Full Load / Low Input

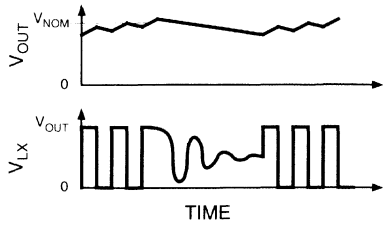


Figure 2b. Nominal Load / Nominal Input

Applications Information

Theory of Operation

Micrel's MIC63x/64x family of step-up controllers maintain a constant output voltage V_{OUT} by comparing a fraction of this voltage to an internal reference and gating an internal N-channel MOSFET ON for a fixed duty cycle (50%) if the output is low. Conversely, if the output is high the MOSFET is not gated ON. The MIC63x/64x is different than controllers called Pulse Width Modulators (PWMs) which provide a variable duty cycle gating signal to keep the output in regulation. The mode of operation of the MIC63x/64x is called 'hysteretic' referring to the difference of voltage which must occur on the output in order to force a change of state of the error comparator output.

Internal Power and Startup

The MIC63x/64x does not have a dedicated supply voltage pin. Internal circuit power is provided by the output voltage which is developed across the filter capacitor C1. Internal operation begins after V_{IN} ($\geq$ 2V) charges C1 (external) through L1 (external) and D1 (internal).

Circuit Operation

Since pin 7 (FB) is grounded, the offset comparator U1 (and inverter) direct the analog switches to route a fraction of V_{OUT} which is dropped across R2 to appear at the inverting input of U2. Assuming V_{OUT} is low (for example, < 5.0V if using the MIC631) U2's output will be high, gating Q1 ON when the oscillator is low. V_{IN} is then impressed across L1 with D1 reverse biased. L1's current versus time will ideally be a ramp (see figure 1) whose value can be found from equation 1. Because of the non-zero ON resistance of Q1, which is dependent on V_{OUT} plus L1's winding resistance, the actual circuit current may take an exponential form (figure 1).

(1) $i(t) = V_{IN} (1 \times 10^{-5}) / L1$

After 10µs the oscillator goes high, terminating Q1's gate drive, causing its drain voltage to rise. The energy stored in L1 will cause Q1's drain voltage to exceed V_{IN}, forward biasing D1 increasing V_{OUT} proportional to the energy stored. L1's discharge current versus time is given by equation 2 and is shown in figure 1.

(2) $i(t) = (V_{IN} - V_{OUT}) (1 \times 10^{-5}) / L1$

The charging and discharging of L1 continues until the output voltage is high enough that the voltage across R2 exceeds the reference voltage. When this occurs U2 will cease gating Q1 ON. Because the output must provide MIC63x/64x supply current plus load current, the output voltage will eventually drop forcing U2 to change states again gating Q1 ON until the output is within tolerance. This action continues as required to keep V_{OUT} constant.

The MIC63x/64x L_X waveform may take on the appearance shown in figure 2a, completing several cycles until the output is high enough to trip U2 then ceasing switching action until the output voltage causes U2 to gate Q1 ON again. When demanded, such as with full load and/or low V_{IN}, the MIC63x/64x will not skip cycles, but will switch Q1 ON and OFF every oscillator cycle (see figure 2b).

Additional Features

Output Voltage Ripple Reduction

As with all Switch-Mode controllers a certain amount of ripple voltage will always be present at the output. Normally, with a properly selected output capacitor (see component selection), this ripple will be low enough to prevent disturbance to the load. Loads which are more sensitive to output ripple may benefit by the addition of a small value capacitor (C_{COMP}) placed between V_{OUT} and the MIC63x/64x COMP pin. The addition of this capacitor provides a low impedance ac path between the output and the COMP pin. This decreases the apparent hysteresis voltage of U2 by allowing a higher value of the output ripple voltage to appear across R2 than would be possible with only R1 present. The result is a lowered peak to peak output ripple voltage. To determine the optimum value of C_{COMP} begin with a 100pF capacitor and increase this value until the ripple voltage has been minimized.

V_{OUT} Adjustment

Should a value of V_{OUT} be required which is not available from the standard family, a resistive divider should be connected between V_{OUT} and ground with their common node feeding pin 7 (FB). The presence of a voltage on FB greater than 150mV will force U1 to redirect the error voltage from FB rather than pin 8 (COMP). It is recommended that R6 be less than 50kΩ to prevent the input capacitance of FB from creating a dominant pole in the output response. Simply put, if R6 is too large, FB's input capacitance will tend to slow the response of the MIC63x/64x resulting in higher ripple voltages at the output. As mentioned earlier a capacitor from V_{OUT} to FB can reduce this problem if R6 must be a large value. To determine the values of R5 and R6 first choose a value for R6 then determine R5 from equation 3.

(3) $R5 = R6 [(V_{OUT} / 1.275) - 1]$

Low Battery Comparator

The MIC63x/64x contains a low battery comparator U3 which drives an N-channel MOSFET (LBO). LBO and LBI (the non-inverting input of U3) are both pinned out. When LBI is greater than 1.275V LBO will be high signaling housekeeping circuitry that plenty of battery power is left. When the battery voltage causes LBI to fall below 1.275V, LBO will go low alerting the user of a low battery voltage. Equation (3a) is used to calculate R3 after selecting a value for R4.

(3a) $R3 = R4 [(V_{OUT} / 1.275) - 1]$

Charge Pump Output (MIC63x)

A charge pump output (CP) is provided on pin 6 of the MIC63x/64x family. This signal is a buffered and inverted replica of the oscillator output. It can be used for voltage doubling and/or inversion (see figures 3 and 4) for low output current applications.

External Gate Drive (MIC64x)

The MIC64x family uses pin 6 (EXT) to drive an external MOSFET for higher power applications. Q1's gate and the external MOSFET are driven in parallel for higher ouput power. For output voltages higher than 16.5V LX should be disconnected from L1 to prevent applying an overvoltage to Q1 (see figures 5 & 6).

Thermal Shutdown

Abnormal conditionals such as inductor saturation or shorting and excessive ambient temperatures can result in excessive junction temperatures in the MIC63x/64x. To prevent damage, thermal shutdown circuitry is activated when the junction temperature exceeds 150°C. The shutdown circuit forces Q1 OFF and prevents it from restarting until the junction temperature has dropped by 10°C.

Component Selection

Inductor L1

The inductor must store an adequate amount of energy each oscillator period to maintain output regulation under the worst case conditions of minimum input voltage V_{IN} and maximum output current I_{OUT}. To arrive at the required value of L1 first solve equation 4 to determine the peak current which must flow in L1 to produce the required output current.

(4) $I_{PK} = (V_{IN} - K) / (2\ R_{DS(ON)})$

Where:

$K = \sqrt{V_{IN}^2 - 16\ R_{DS(ON)}\ I_{OUT}\ (V_{OUT} + V_{D1} - V_{IN})}$

I_{PK} = peak inductor current

V_{IN} = minimum input voltage

V_{OUT} = required output voltage

$R_{DS(ON)}$ = Q1's ON resistance
(see graph "LX Resistance vs. Output Voltage")

I_{OUT} = output load current

V_{D1} = D1 forward drop (use 0.8V)

If I_{PK} is greater than Q1's absolute maximum rating (450mA) use a MIC64x device and an external FET which can safely and efficiently pass this current. Next solve equation 5 for L1's value.

(5) $L1 = V_{IN}\ (1\times10^{-5}) / I_{PK}$

Where:

V_{IN} = minimum input voltage

Practical Example

Let:

V_{IN} = 5V (4.75V minimum)

V_{OUT} = 12V (12.48V maximum)

I_{OUT} = 10mA

$R_{DS(ON)}$ = 4Ω(maximum)

V_{D1} = 0.8V

Then:

$I_{PK} = (4.75 - 4.17) / (2)\ (4) = 77mA$

$L1 = (4.75)\ (1\times10^{-5}) / 0.077 = 625\mu H$

Choose a standard off-the-shelf inductor for L1 whose value is less than that calculated such as 560µH to allow for a lower I_{PK} caused by the resistance of Q1 and the inductor's winding resistance. Table 1 contains a partial list of inductor vendors. L1 can be purchased in various forms such as toroid, pot-core, or rod to meet printed circuit board restrictions. If size is not a constraint, powdered iron is a good choice for the core material although ferrite or Molyperm material can result in smaller size inductors.

C1 Capacitor

The peak to peak magnitude of the output ripple voltage is a complex function of I_{PK}, I_{OUT}, C1's capacitance and ESR (equivalent series resistance). During Q1's OFF time the output ripple is the sum of two components: the product of I_{PK} and C1's ESR plus the total charge into C1 from L1 discharging it's current from I_{PK} to zero. In most cases, the contribution of ripple due to C1's ESR value will be much greater than the ripple voltage caused by C1 being charged by L1. This becomes apparent when I_{PK} is multiplied by C1's ESR, which produces a dominant voltage 'peak' when Q1 shuts OFF.

During Q1's ON time the output voltage will fall as I_{OUT} is drawn from C1 through it's ESR. Again the ESR will tend to produce the majority of this 'valley' voltage while the loss in charge of C1 due to I_{OUT} causes only a slight decrease in V_{OUT}. During this interval the drop in output voltage can be approximated from the product of I_{OUT} times C1's ESR. Equation 6 yields an approximate value of the peak to peak output ripple voltage by combining the sum of the effects of C1's ESR during Q1's ON and OFF times.

(6) $V_{P-P} \leq (ESR\ I_{PK}) + (ESR\ I_{OUT})$

Where:

V_{P-P} = output peak to peak ripple voltage

ESR = C1's ESR value at 50kHz

I_{PK} = peak inductor current

I_{OUT} = output load current

To obtain the maximum ESR value given a target V_{P-P} rearrange equation 6 to equation 7.

(7) $ESR \leq (I_{PK} + I_{OUT}) / V_{P-P}$

For the example given earlier assume V_{P-P} less than 200mV. Then:

$ESR = (0.077 + 0.01) / 0.2 \leq 0.435\Omega$

In general, electrolytic capacitors are more suitable for the output capacitor as they are inexpensive, readily available from several vendors and are offered in a modest capacitance to volume ratio. Tantalums can be used, often with a space savings, but are generally more expensive. To reduce wideband noise on the output which is caused by the abrupt switching of Q1, it is recommended that a 0.1µF low ESR capacitor be placed in parallel with C1.

Select an electrolytic family (see table 2 for capacitor vendors) specifically intended for use in switch-mode power supply applications. These will exhibit low ESR values.

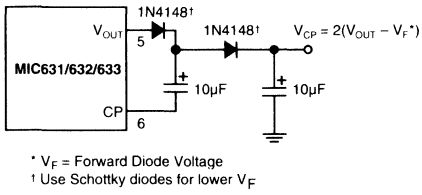


Figure 3. Voltage Doubler

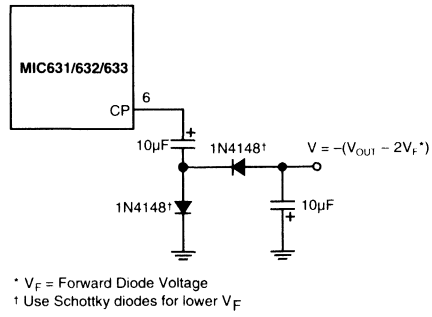


Figure 4. Voltage Inverter

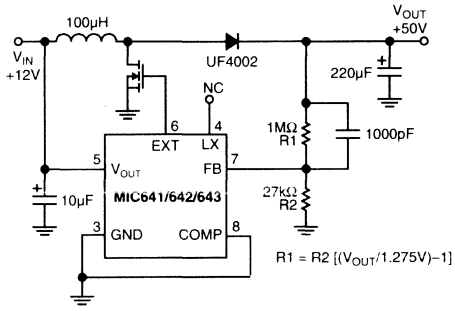


Figure 5. High-Voltage Step-Up Converter

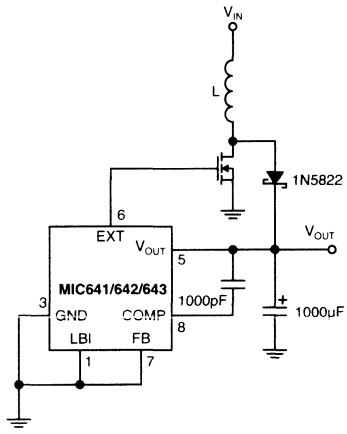


Figure 6. High-Current Step-Up Converter

Component Manufacturers

Caddell-Burns	Mineola, NY (516) 746-2310
Coilcraft	Gary, IL (708) 639-1469
Custom Coils	Alcester, SD (605) 934-2460
Dale	Columbus, NE (402) 564-3131
Gowanda	Gowanda, NY (716) 532-2234
J.W. Miller	Gardena, CA (310) 515-1720
Renco	Deer Park, NY (516) 586-5566
Sumida	Arlington Heights, IL (708) 956-0666

Note: This is only a partial listing of manufacturers.
Micrel does not endorse any one of the above manufacturers.

Table 1. Inductor Manufacturers

Mallory	Indianapolis, IN (317) 856-3731
Marcon	Vernon Hills, IL (312) 913-9980
Nichicon	Schaumburg, IL (708) 843-7500
United Chemi-con	Rosemont, IL (708) 696-2000

Note: This is only a partial listing of manufacturers.
Micrel does not endorse any one of the above manufacturers.

Table 2. Electrolytic Capacitor Manufacturers

Application Hint 11

500kHz 30W Off-line Switching Power Supply

by George Hall

Circuit Description

Line Input

Alternating line voltage is rectified by D1 and filtered by C1 to provide a dc bus voltage for the main transformer T1 and MIC38HC43 controller IC1.

Thermistor RT1 limits the in-rush current to C1, protecting D1, and reducing the chance of an unacceptable momentary voltage drop on the ac input line during turn-on.

PWM Operation

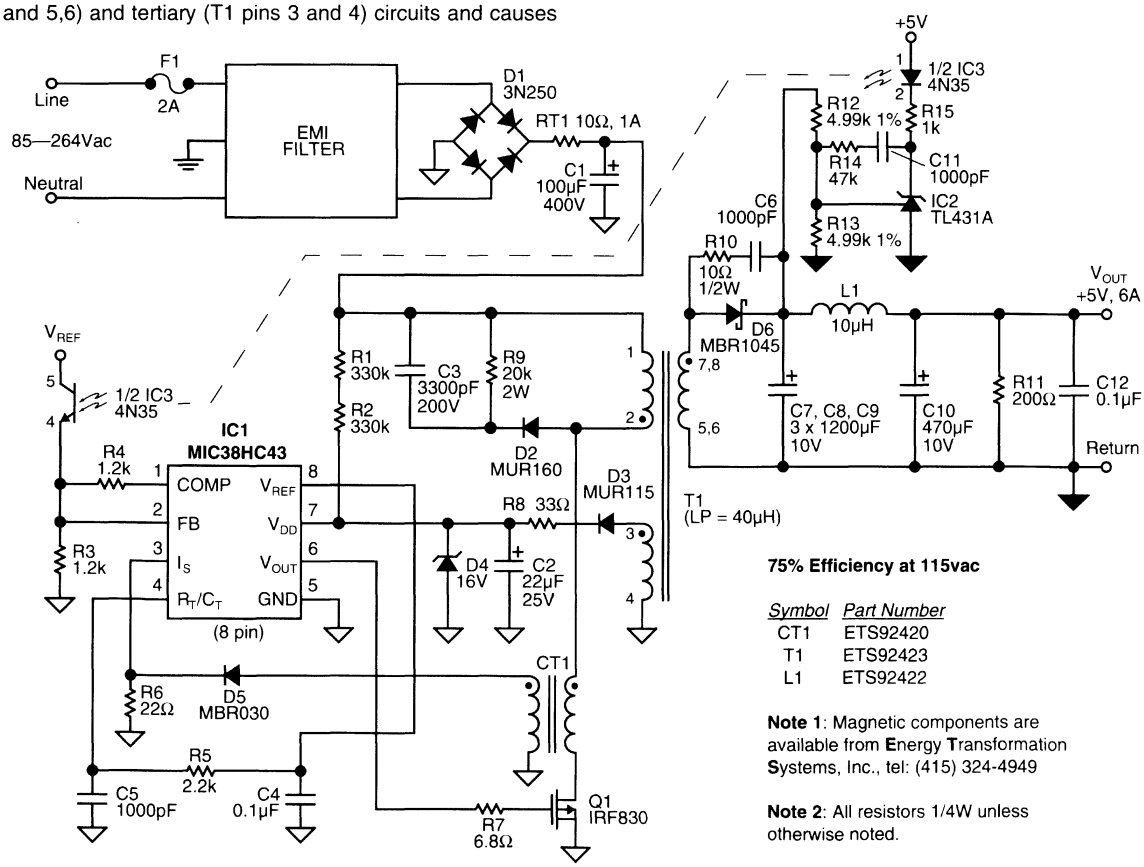
Resistors R1 and R2 charge C2 until its voltage exceeds the UVLO (undervoltage lockout) of IC1 which causes output drive to be applied to Q1. This lowers Q1's drain voltage and charges T1's primary until the current sense voltage at pin 3 of IC1 exceeds 1V. IC1 then removes drive from Q1.

With Q1 off, T1 discharges into both the output (T1 pins 7,8 and 5,6) and tertiary (T1 pins 3 and 4) circuits and causes Q1's drain voltage to rise above C1's voltage. IC1 voltage is now supplied from the low impedance winding of T1 (pins 3 and 4).

The output voltage rises until IC2's reference voltage reaches approximately 2.5V where it begins drawing current through the diode of optocoupler IC3. IC3's detector transistor conducts, raising the voltage on pin 2 of IC1. When the output voltage equals 5V, pin 2 of IC1 will be 2.5V and current mode PWM operation will regulate the output precisely over varying line and load changes. R14 and C11 provide stability compensation for IC2.

Q1 Protection

Components D2, C3, and R9 protect Q1 from avalanche breakdown and possible destruction by clamping the leakage inductance spike to a safe level. C6 and R10 suppress parasitic oscillations from D6.



75% Efficiency at 115vac

Symbol	*Part Number*
CT1	ETS92420
T1	ETS92423
L1	ETS92422

Note 1: Magnetic components are available from **E**nergy **T**ransformation **S**ystems, Inc., tel: (415) 324-4949

Note 2: All resistors 1/4W unless otherwise noted.

EMI Filter

Electromagnetic interference feedback into the ac input line from the operation of switched mode power supplies requires EMI filtering to comply with national and international standards. Use these standards to determine the acceptable levels of line conducted emissions for the specific application and location.

EMI filtering may be simplified by procuring several packaged EMI filters from a reputable source. Select the appropriate filter by EMI measurement. Include the selected filter in the final design or substitute the individual components (from the filter's parts list). Printed circuit board layout and component placement will affect conducted emissions. If you are not qualified in the this area consult an expert.

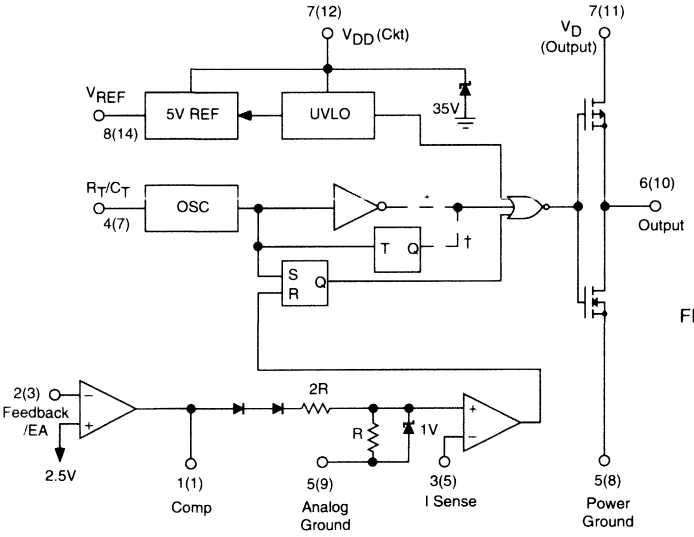
Circuit Layout

Care should be taken when designing high frequency converters to avoid capacitive and inductive coupling of the switching waveform into high impedance circuitry such as the error amplifier, oscillator, and current sense amplifier. Avoid long printed circuit traces and component lead lengths. Locate oscillator and compensation circuitry near the IC. Use high frequency decoupling capacitors on V_{REF} and, if necessary, on V_{DD}. Return high di/dt currents directly to the source and use large area ground planes where possible.

Safety

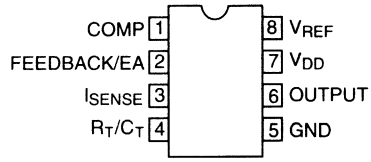
Always proceed with caution when working on off-line supplies as lethal voltages are present. Never work on the supply without someone nearby who is aware of the hazards and can take steps to avoid serious injury to yourself in the event of an accident.

Block Diagram

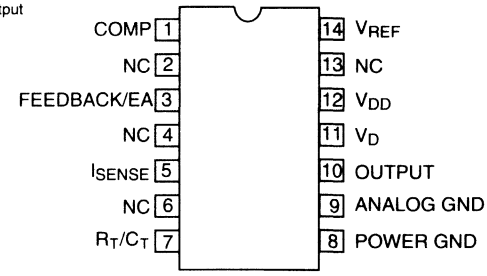


* MICx8C42, 43 / MICx8HC42, 43
† MICx8C44, 45 / MICx8HC44, 45

Pin Configurations



8-pin DIP



14-pin DIP
(suffix -1, full featured parts)

Also available in 8-pin and 14-pin SOIC packages.

7

Application Hint 12

Designing with the MIC3830 Family

by George Hall and Brenda Kovacevic

Introduction

The MIC3830 family is the first-ever family of PWM controllers designed specifically for current-fed topologies. A current-fed topology is a SMPS (switch mode power supply) topology where the transformer center tap is fed by an inductor current instead of a voltage. This applies only to center-tapped applications such as push-pull or multiple output schemes (Figures 1, 2).

Since the transformer's primary sees a current instead of a voltage, overlapping conduction (caused by turning on both sides of the transformer at the same time) cannot create core saturation. (Core saturation can be catastrophic leading to the destruction of not only the transformer itself, but also of surrounding components, such as the power FET switches.)

Prior to the creation of the MIC3830 family, implementing a current-fed topology meant using not only a PWM controller, but a flip-flop and two FET drivers. The designer was also left with the task of ensuring that the transformer drive FETs were one-half (one-fourth) the PWM frequency, and that propagation delays did not affect the synchronization of the system.

The MIC3830 also introduces many features that simplify designs, such as programmable soft start, front edge blanking, choice of voltage or current mode control, cycle-by-cycle current limit (current mode control), overcurrent shutdown (voltage mode control), a maximum duty cycle limiting function, and 1 amp output drive capability.

Practical Considerations

Layout

PWM controllers are very sensitive to layout. This makes the use of the traditional solderless breadboards as a prototyping tool close to impossible!

A copper clad or mesh prototyping board should be used, with large buss bars for a ground plane. All ground wires should be kept as short as possible, and all grounded components emanating from the MIC3830 should have a single-point ground.

Likewise, the switching elements (FETs or power transistors) should be kept very close to the drive outputs. Stray capacitance/inductances can cause undue noise on the switching waveforms. Oscillator and loop compensation components should be kept as close to the pins as possible.

Bypassing

Proper bypassing is essential. In addition to the chosen bootstrap capacitor, a 0.1µF ceramic disc capacitor should be used both between V_{DD} and ground, and V_{REF} and ground. The additional bypassing of V_{REF} ensures less noisy operation of the error amplifier, and gives better regulation as a result.

Component Choice

SMPS systems as a rule are very sensitive to component quality. The oscillator components, C_T and R_T, require careful attention. R.F. capacitors such as silver mica, glass, polystyrene, or COG ceramics are recommended. High K ceramic capacitors should not be used. (These guidelines can also be applied to the soft start and front edge blanking capacitors.)

It is very important to use no less than a 2.2nF capacitor as the oscillator C_T. Values smaller than this have led to "phase jitter" or phase shifting in the oscillator as the timing ramp becomes too sensitive to noise.

Careful attention to the SOA (safe operating area) curves of the chosen power FETs will pay off in increased reliability. It is important to make sure that inductive spikes do not create conditions that exceed the SOA of these devices. If a p-channel FET is used as the main switching element, be sure

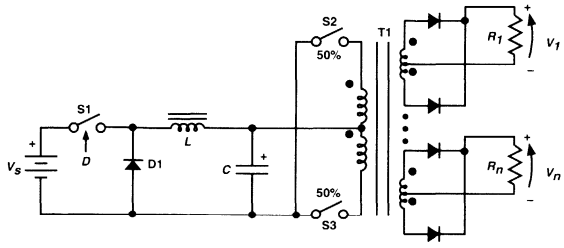


Figure 1. Current-Fed Multiple Output Topology

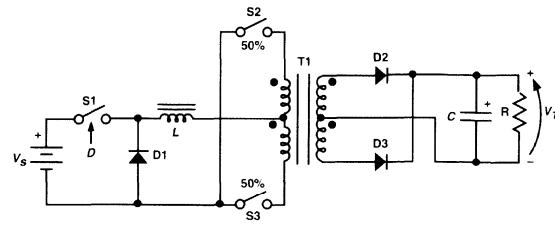


Figure 2. Current-Fed Push-Pull Topology

to accommodate the higher dissipation (due to higher $R_{DS(ON)}$) by using adequate heat sinks.

If fast switching speed N-channel FETs are used, a resistor in series with the gate is sometimes necessary. This low value resistor (10Ω—100Ω) helps to filter the EMI/RFI generated at turn-on and also slows down the turn-on slightly. This noise generated from the Q and $\overline{Q}$ outputs can cause frequency shifting in the oscillator without this resistor if the switching speed is too fast.

Inductors and transformers should be carefully designed following either magnetics texts or manufacturer instructions. Careful attention should be paid to core size so that saturation of the core doesn't occur. Losses should be minimized by using appropriate wire type and size (litz wire or copper foil minimizes skin effects at high frequency) and winding the cores tightly.

If powdered iron cores are used for their low cost, be sure to calculate the thermal characteristics. They can get quite hot and can cause temperature coefficient related parameter shifts in other parts of the circuit.

Gapping of the cores during prototyping should always be done using spacers as hand grinding can be inaccurate and lead to shifts in material properties.

The output capacitor quality is crucial to the stability and output ripple of the completed supply. The critical parameter to be minimized is the ESR (equivalent series resistance).

This can be minimized by paralleling several types of capacitors (all become series resonant at different frequencies), using a special low ESR aluminum electrolytic (available from Nichicon, United Chemicon, and Panasonic), using a very large aluminum electrolytic (ESR varies inversely with size), or using a new polymeric capacitor available from Sanyo; the Oscon series (max. value = 220μF).

Features

Max. Duty Cycle/Soft Start

As this pin provides a double function, both as an input for the max duty cycle limiting voltage and for the soft start capacitor, it must be handled with care. The NPN pull down for soft start or overcurrent shutdown is located on this pin; if turned on it will pull down the output and effectively turn off the part. It will draw several mA in this state. For this reason (and to prevent the max. duty cycle from being 0%!), this pin cannot be allowed to float. It must be tied to a non-zero voltage though a pull-up resistor (5V and up gives 100% max. duty cycle). The main use of this function is to provide a fail-safe to keep a current mode power supply below 50% duty cycle (to prevent the well-known subharmonic oscillation problem from occurring). It is important that a well designed compensation network also be in place as this limiting point will vary quite a bit over temperature.

Soft start prevents damage to the system by starting the MIC3830 slowly after an overcurrent condition has happened. It is **only** operative if the shutdown pin is used; if current mode control is used, both the shutdown and current mode ramp pins should be connected to the external sense resistor. The time constant is set by R_{TH} C, where R_{TH} is the Thevenin equivalent resistance seen by this pin, and C is the capacitor placed from this pin to ground. To prevent interaction effects with the front edge blanking feature, this capacitor should be larger by 1.5× than the front edge blanking capacitor.

Current Limit/Shutdown

If current mode control is used, cycle-by-cycle current limiting is a fringe benefit. It should be noted that the MIC3830 family has a higher threshold than most: 3.5V (1.5V + error amplifier output). If voltage mode control is used, then the shutdown pin is tied to an external sense resistor to provide a one time current shutdown (not cycle-by-cycle). The threshold is 1.0V for current limiting, and 1.25V for a full shutdown. If current mode control is used and no soft start function is desired, then the overcurrent shutdown pin **must** be tied to ground. Letting it float will lead to noise induced shutdowns.

Voltage Reference

The 5V bandgap, trimmed to 2% accuracy, is available as a source to power the soft start/max. duty cycle pin, front edge blanking pin, and positive error amplifier input. Even though the short circuit current is 60mA typical, it is important to keep from pulling down the reference. Larger resistance values (10k and up) should be used for pull-ups and voltage division from this pin.

Error Amplifier

The error amplifier of the MIC3830 is extremely sensitive; all components used should be tied as closely as possible to the error amplifier pins. As it has a very high open loop gain, ~95dB, the compensation network gain should be kept lower. It also has an open loop pole at around 110Hz that should be taken into account in designing any stability network. Bandwidth is around 5MHz.

Headroom is also an important consideration. To maximize headroom, it is wise to divide the reference by two (use two 10k resistors) before supplying the positive input. If common mode range is exceeded, a condition in which the polarity of the inputs are switched can occur.

A good rule of thumb for stability networks is to keep the unity gain crossover point from 1/5 to 1/6 of the switching frequency, and to keep the phase margin above 45°.

Front Edge Blanking

Front edge blanking is a feature that eliminates the need for a filter around the sense resistor. It provides a delay prior to the current limit/shutdown or cycle-by-cycle current limit becoming active. This prevents initial systems transients or spikes from causing systems instabilities in current mode control, or overcurrent shutdowns in voltage mode control.

Duration of the blanking should be as short as possible while still providing adequate spike/transient time delay. The timing is set by placing a capacitor from the F.E.B. pin to ground, and is 0.38RC, where R should be a 10k pull-up resistor to V_{REF}. The capacitor used here should be smaller than the one used on the soft start pin to prevent any interaction effects.

Design Example

100kHz Current Fed Converter

A 5V, 20A max DC to DC converter was designed using the current fed push–pull configuration for increased safety and reduced size/transformer core area.

The input is an unregulated 14V to 32V dc supply, such as is commonly found in aircraft environments. This supply is fed to an MIC2951 low drop out regulator which acts as a housekeeping supply; supplying a steady, well regulated 12V to the MIC3833.

The main PWM switching element is an IRF540, with gate drive provided by transformer T1. The two 50% duty cycle outputs each drive an IRF540 directly, which in turn drive their respective sides of T2's center tapped primary. The 1N6291A is a transzorb used to protect the FETs from spikes generated by the transformer.

Current mode control was chosen to simplify the stability analysis; with the 0.2Ω 5W resistor being used as the sensing element. As the maximum duty cycle at light loads is greater than 50%, the well characterized problem of subharmonic oscillations found when using current mode control was evident. A ramp was introduced at the sensing element to correct this; the 10kΩ and 470kΩ divider from the oscillator (ramp source) to the sensing element provide the proper slope. As a large resistor value was chosen to place on the oscillator pin, no buffering was necessary.

Front edge blanking was used to eliminate the need for a filter network around the sensing element, and reduce the possibility of turn-on transients causing system instabilities.

Four inexpensive capacitors were paralleled to lower ESR to an acceptable level of 80mΩ without adding too much size or cost.

Error amp compensation was performed using a simple lead–lag network. As current mode control was used, there was no need to compensate the LC filter pole.

A voltage of 2.5V derived from the reference was fed to the Max. duty cycle pin to provide a failsafe. This prevents the PWM out from attaining greater than 75% duty cycle.

Soft start was also implemented to allow slow turn-on in the event of a short circuit.

All magnetics were chosen to minimize losses at 100kHz. T2 and L1 were wound using Seimen's new N87 material, and T1 using Magnetics Inc's P–type material. T2 and L1 were made using Seimen's new EFD core and bobbin assemblies, which were designed to reduce the height/form factor of the finished supply. T1 is a simple toroid.

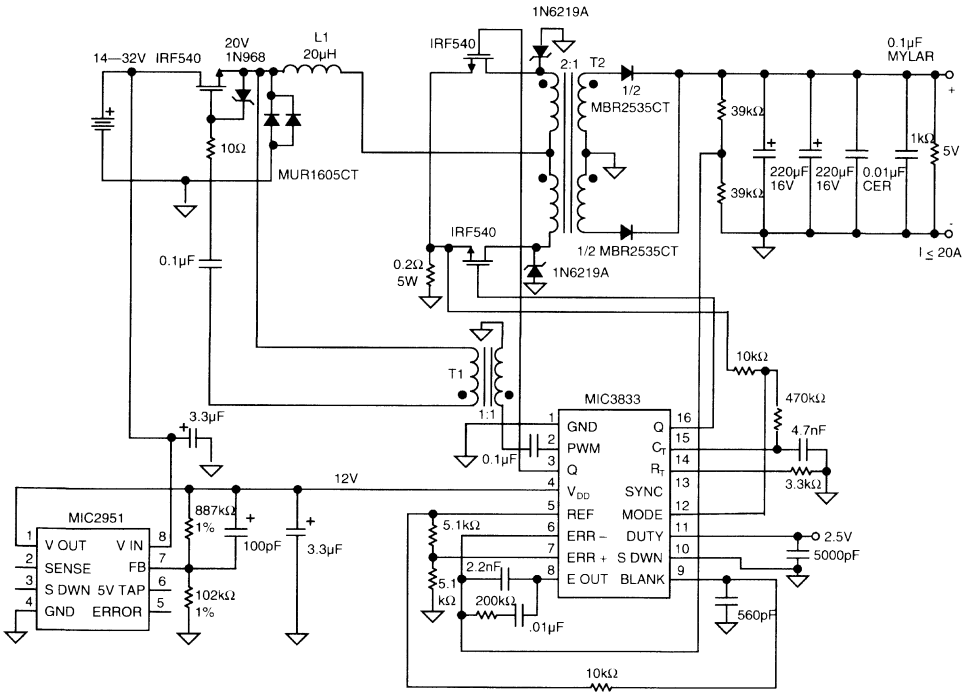


Figure 3. 100W Current Fed Push–Pull DC to DC Converter

Magnetics Design

T1: Magnetics Inc # 41303 – TC, P material, Primary = 26 T 30 gauge wire, Secondary = 26 T 30 gauge wire

T2: Seimen's EFD40, N87 material. Primary = 20 T 20 gauge wire, Secondary = 10 T trifilar wound 20 gauge wire. Both are center tapped.

L1: Seimen's EFD30, N87 material. 13 T 20 gauge wire. Gap for 20 μH

Application Hint 13

A Design Guide for the New BiCMOS LM2575 Family

by George Hall and Brenda Kovacevic

Introduction

BiCMOS technology has given the classic LM2575 switcher many added benefits. Faster rise/fall times, faster response to fault conditions, and improved efficiency at light loads, are a few of the many improvements now offered. The key feature that has led to the popularity of this device, its sheer simplicity, has been improved by these upgrades. In fact, it is now even easier to use!

Basic Operation

The LM2575 switcher is basically a PWM (pulse width modulator) controller IC with a fixed gain error amplifier, a 52kHz oscillator, and internal compensation network. The non-inverting side of the error amplifier is tied to a 1.23V bandgap reference. The improved BiCMOS drive stage (see block diagram) gives the LM2575 its faster rise/fall times.

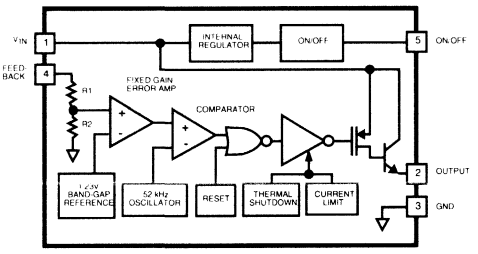


Figure 1. Block Diagram

Design Procedure

Output Voltage

For fixed output requirements a 3.3V 5.0V, 12V, or 15V can be obtained with no additional resistor network.

For the adjustable versions:

$$V_{OUT} = 1.23V\ (1 + R2/R1)$$

For best results, R1 should be between 1kΩ and 10kΩ.

Inductor Selection

Two criteria are used for inductor selection: peak current and continuous/discontinuous mode operation.

To prevent core saturation, the inductor must be able to withstand the peak operating current.

Discontinuous mode operation occurs when the inductor empties itself of all stored flux during each OFF cycle. For efficiency and simplicity reasons, it is preferable to operate in the continuous mode. Discontinuous mode allows the use of a smaller inductor size, which may be preferable in some instances.

Either a standard off-the-shelf inductor can be chosen, or one can be designed to optimize the requirements of each unique application.

If an "off-the-shelf" inductor is preferable, simply calculate the volt-second (V • μs) product:

$$V \bullet t = [(V_{IN} - V_{OUT})\ (V_{OUT} / V_{IN})\ 1000] / 52$$

Match this number to the V • t number on the vertical axis of the graph in Figure 2. The horizontal axis shows your maximum load current; locate the region intersected by these two values. The inductor code given is referenced to the

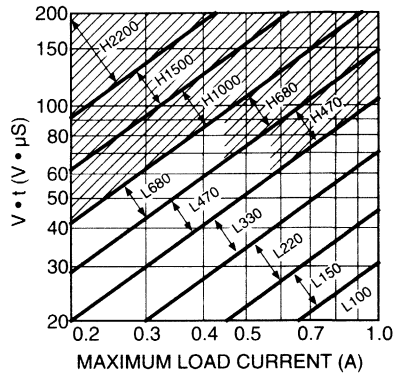


Figure 2. Inductor Code Chart

appropriate part number in Figure 3. Please note that all values result in continuous mode operation. These inductors are conservatively designed and well-guard banded.

Inductor Code	Inductor Value	Custom Coil[1] Part Number	Renco[2] Part Number
	47μH	4926	RL5035
	68μH	4927	RL5036
L100	100μH	4928	RL5037
L150	150μH	4929	RL5024
L220	220μH	4930	RL5028
L330	330μH	4931	RL5029
L470	470μH	4932	RL5030
L680	680μH	4933	RL5031
H150	150μH	4934	RL5038
H220	220μH	4935	RL5043
H330	330μH	4936	RL5044
H470	470μH	4937	RL5045
H680	680μH	4938	RL5039
H1000	1000μH	4939	RL5040
H1500	1500μH	4940	RL5041
H2200	2200μH	4941	RL5042

Figure 3. Inductor Selection and Cross Reference

For applications where the regulator must fit into a small physical space, small inductors (low cost powered iron toroids, optimized premium MPP (Molypermalloy) toroids, and surface mount inductors) are available from Custom Coils and Renco. All offered for 1A peak currents. Figure 4 shows Renco part numbers.

Inductor Value	MPP Toroid (Renco #)[1]	Powered Iron Toroid (Renco #)[1]	Surface Toroid (Renco #)[1]
20µH	RL-5058	RL-5046	RLS-1500-20
48µH	RL-5060	RL-5048	RLS-1500-48
68µH	RL-5062	RL-5050	RLS-1500-68
100µH	RL-5064	RL-5052	RLS-1500-100
220µH	RL-5066	RL-5054	RLS-1500-220
330µH	RL-5068	RL-5056	RLS-1500-330

Figure 4. Small Size Inductors

MPP toroids are more expensive but allow more efficient energy storage hence smaller size. The powered iron cores are the lowest cost, and are self-gapped.

To design an inductor for use with the LM2575, first look at the core manufacturer's data sheets. The minimum core size needed to prevent saturation is:

$$V_e = I_P^2 \bullet L \bullet \mu_e \bullet (0.4\pi) / B_O^2 \bullet 10^{-8}$$

where: I_P = peak current (A)

L = inductance (H)

μ_e = effective relative permeability (of the core)

B_O = maximum operating flux density (Gauss)

V_e = effective core volume (on core data sheets)

B_O can be assumed to be between 2,000 Gauss and 2,500 Gauss for most ferrite materials. At this stage, we can arbitrarily assume an L value (50µH to 1000µH are common values).

If the V_e value you get is too large to be practical, you can adjust the value downwards, or change the μ_e value by adding a gap. The required gap size is given by:

$$g = l_e (\mu / \mu_e - 1) / \mu$$

where: μ = relative permeability (of the material)

l_e = magnetic path length (usually in cm on the data sheet also)

Now, refer to magnetics manufacturer's catalogs to pick the type and size of core desired. To be on the safe side, choose a V_e value of 1.5 × the calculated minimum. Pot cores and toroids are sometimes preferable as the magnetic shielding is better. However, E-cores are very easy to wind and can be purchased in forms that have reduced height (i.e., Siemens' new EFD cores).

To check for continuous mode operation we need to look at the boundary current between continuous and discontinuous mode operation.

$$I_{LB} = [(D / f_S) / 2L] (V_{IN} - V_{OUT})$$

where: D = duty cycle (= V_{OUT}/V_{IN} for a buck regulator)

f_S = 52kHz, switching frequency

L = Inductance (H)

I_{LB} = Average inductor current at the boundary between continuous and discontinuous mode conduction.

If the expected output current at the operating point chosen will be greater than I_{LB}, then the inductance value chosen will be sufficient to keep the supply in continuous mode conduction. If it is smaller than I_{LB}, then the chosen L value must be raised. Another iteration of the core size calculation must be performed to make sure that the higher inductance value doesn't result in saturation.

For light load conditions or when the above inductance values are very high, it may be preferable to operate in the discontinuous mode. Both maximum output power and efficiency are reduced in discontinuous mode.

The number of turns necessary can now be calculated by:

$$N = \sqrt{(2 \bullet l_e) / (\mu e \bullet Ae \bullet 0.4\pi \times 10^{-8})}$$

It is important to use a wire gauge appropriate to the peak currents expected. A better fill factor on the bobbin as well as reduced wire losses can be obtained by paralleling two or more smaller gauge wires instead of using larger gauge wire.

Output Capacitor Selection

The capacitor must satisfy the following requirement for stable operation:

$$C_{OUT} \geq 7.785 [(V_{IN(max)}) / (V_{OUT} \bullet L)]$$

where: L = inductance (µH)

Its maximum voltage rating should be at least 1.25 × the output voltage.

As ESR (equivalent series resistance) is the major contributor to ripple voltage, it is desirable to minimize ESR. This can be done by using a higher value capacitor (ESR goes down as capacitor value goes up), paralleling several standard electrolytic capacitors, or using special low ESR capacitors. Low ESR electrolytic capacitors are available from Panasonic, Nichicon, and United Chemicon. A new polymeric capacitor, the Oscon series, is available from Sanyo. Using one of the above techniques, output ripple can be reduced to 10mVp-to-p to 20mVp-to-p. A small LC filter can be used to provide further reduction in output ripple.

The capacitor's ripple current rating at 52 kHz should be at least 50% higher than the ripple component of the inductor current.

$$I_{RIPPLE(max)} \geq 1.5 \times 0.3 \times I_{LOAD(max)}.$$

Input Capacitor Selection

To maintain stability, the input bypass capacitor must be at least 47µF. Low ESR capacitors are recommended. If the operating temperature range is below –25°C, the value of this capacitor should be increased. Adding a ceramic or solid tantalum capacitor near the input pin will also increase regulator stability at low temperatures. The capacitor's ripple current rating should be greater than $1.2 \times (t_{ON}/T) \times I_{LOAD}$ for maximum operating lifetime.

Catch Diode Selection

Although either a Schottky or a fast recovery diode can be used, a Schottky diode will provide the best performance as the lower voltage drop and faster switching speed will result in higher efficiency.

Also, a fast recovery diode with abrupt turn-off characteristics may cause EMI problems and/or instabilities.

A standard 1N400x series diode **cannot** be used, as it cannot recover fast enough.

The reverse voltage rating of this diode should be at least 1.25 × the maximum input voltage.

Typical Applications

3.3V fixed Output Buck Regulator

Shown in Figure 5 is a 3.3V buck regulator using inexpensive standard components.

The high efficiency (~80%) and low form factor afforded by the use of a new TO-263 surface mount package makes this an ideal candidate for battery operated designs.

If lower ripple voltage is desired, the standard 220µF capacitor can be replaced with a standard 330µF capacitor at the cost of additional size, or an Oscon 105A220M capacitor (220µF, 35mΩ ESR) can be used.

Inverting Buck-Boost

By bootstrapping the regulator's ground pin to the negative output voltage and grounding the feedback pin, the regulator can be made to sense and regulate a negative output voltage. Figure 6 shows a –5V, 0.25A buck-boost circuit that illustrates this.

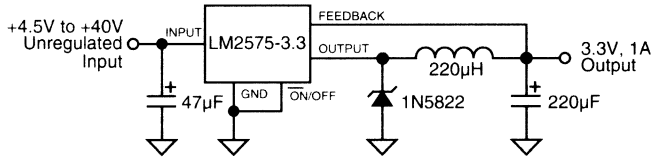


Figure 5. 3.3V Buck Regulator

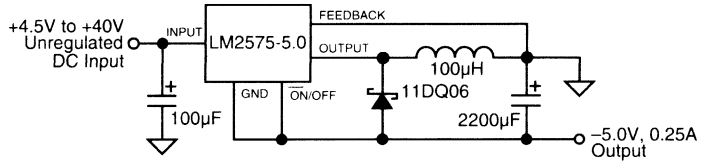


Figure 6. Inverting Boost-Buck Regulator

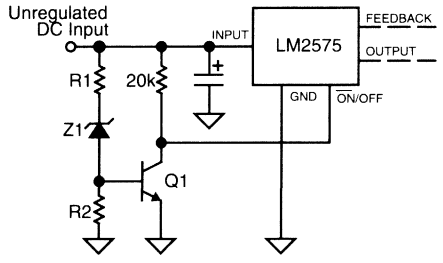


Figure 7. Undervoltage Lockout

24V to 5V Isolated Flyback Regulator

When isolation is desired as in many telecommunications applications, an isolated flyback scheme can be used, as is shown in Figure 8.

A simple 4N35 optoisolator and a 1:1 transformer ensure complete isolation from the input to the load. Feedback is provided via a TL431 shunt regulator to the LM2575's feedback pin.

To prevent the output pin from being taken too far below ground (and forward biasing the substrate diode), a floating ground scheme is used. The Schottky, resistor, and diode combination also serves as a snubber for the flyback transformer.

Note that bypassing is performed to both the pseudo-ground and the system ground to effectively remove noise.

Discontinuous mode operation was chosen to keep the transformer size small, and to remove the right hand plane pole that occurs when you use continuous mode conduction with a flyback topology.

External compensation is now necessary as the additional elements in the feedback loop (optoisolator and shunt regulator) have changed the overall transfer function. A simple RC compensation network was added around the shunt regulator.

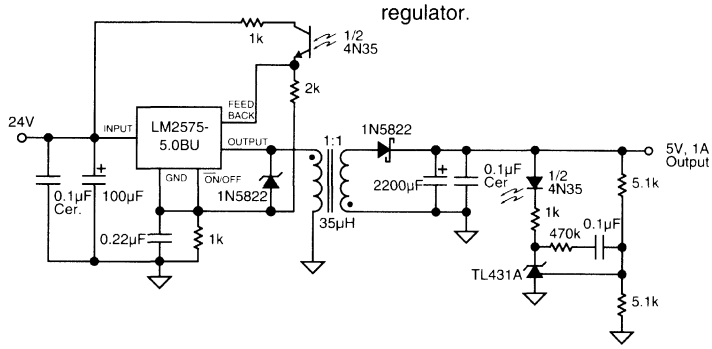


Figure 8. Isolated Flyback DC-DC Converter

Renco Part[1]	Description	
RL5049	48µH 3A	Powdered Iron Toroid
RL5050	68µH 1A	Powdered Iron Toroid
RL5051	68µH 3A	Powdered Iron Toroid
RL5052	100µH 1A	Powdered Iron Toroid
RL5053	100µH 3A	Powdered Iron Toroid
RL5054	220µH 1A	Powdered Iron Toroid
RL5055	220µH 3A	Powdered Iron Toroid
RL5056	330µH 1A	Powdered Iron Toroid
RL5057	330µH 3A	Powdered Iron Toroid
RL5058	20µH 1A	MPP Toroid
RL5059	20µH 3A	MPP Toroid
RL5060	48µH 1A	MPP Toroid
RL5061	48µH 3A	MPP Toroid
RL5062	68µH 1A	MPP Toroid
RL5063	68µH 3A	MPP Toroid
RL5064	100µH 1A	MPP Toroid

Renco Part[1]	Description	
RL5065	100µH 3A	MPP Toroid
RL5066	220µH 1A	MPP Toroid
RL5067	220µH 3A	MPP Toroid
RL5068	330µH 1A	MPP Toroid
RL5069	330µH 3A	MPP Toroid
RL5070	35µH 3A	1:1 Toroid Transformer
RLS-1500-20	20µH 1A	Surface Mount
RLS-1500-48	48µH 1A	Surface Mount
RLS-1500-68	68µH 1A	Surface Mount
RLS-1500-100	100µH 1A	Surface Mount
RLS-1500-220	220µH 1A	Surface Mount
RLS-1500-330	330µH 1A	Surface Mount

Parts also available from Custom Coils[2].

Figure 9. Additional Part Numbers

1. Renco Electronics Inc., Deer Park, New York; tel: (516) 586-5566
2. Custom Coils, Alcester, South Dakota; tel: (605) 934-2460

Application Hint 14

Current-Fed Push-Pull SMPS using the MIC3833

by George Hall and Brenda Kovacevic

Introduction

Most DC-DC and off-line converters have utilized the voltage fed transformer approach to convert input voltages to useful output voltages. Transformer saturation (flux imbalance) in push-pull and bridge type topologies was of concern as it could lead to catastrophic switch failure. Additional circuitry was required to correct transformer flux imbalances by enforcing constant volt-seconds across the transformer primary.

Current mode controllers with their inherent cycle-by-cycle current limiting monitor and compensate for flux imbalances but are still a voltage-fed topology. They remain candidates for switch failure due to the low impedance voltage source. The use of current-fed topologies reduces or eliminates switch failures.

Theory

Figure 1 shows the basic elements of a typical current-fed push-pull topology. Variable duty cycle pulses are applied to S1 forcing a current to be fed to T1. The duty cycle is controlled to provide an average voltage to T1's center tap. S2 and S3 are operating 180° out of phase with each other and at one-half S1's frequency. The average voltage from the primary of T1 is transformed to the secondary voltage required by the output section.

Line and load changes to the output(s) are monitored and used to adjust S1's duty cycle to maintain a steady output voltage. Output inductors are not needed (a cost savings) since filtering is accomplished by the input inductor.

Advantages

Reliability

Current fed topologies deliver current from a high impedance source, inductor L1, to the main transformer T1. The high source impedance makes destruction of the switches unlikely even with a transformer flux imbalance.

Transformer Utilization

The main transformer is 100% utilized (no dead-time) which gives multiple output designs excellent cross regulation from master to slaves. This simplifies or eliminates the need for post regulation schemes.

Reduced Parts Count

Since the buck inductor is in the primary, the output rectifiers do not support inductor current during the dead-time normally associated with voltage-fed designs. This means the inverter switches (S2 and S3) do not experience the high initial current spike required to suppress the output inductor current flowing in the rectifiers. Also since there is no output inductor current flowing in the output rectifiers there is no leakage energy stored in the output winding. This means that snubbers are not required (a cost savings) to protect the output rectifiers.

The Micrel MIC383x Family

Micrel Semiconductor has introduced a family of current-fed controllers which can operate in current or voltage mode. This single IC controller can operate up to 500kHz and supplies 1 amp of drive current on both the $\overline{Q}$ and PWM drive outputs. Cycle-by-cycle current limiting, front edge blanking, soft start, shutdown, maximum duty cycle programming, and external synchronization have been incorporated. All error amplifier connections and a 5V ±2% reference are made available.

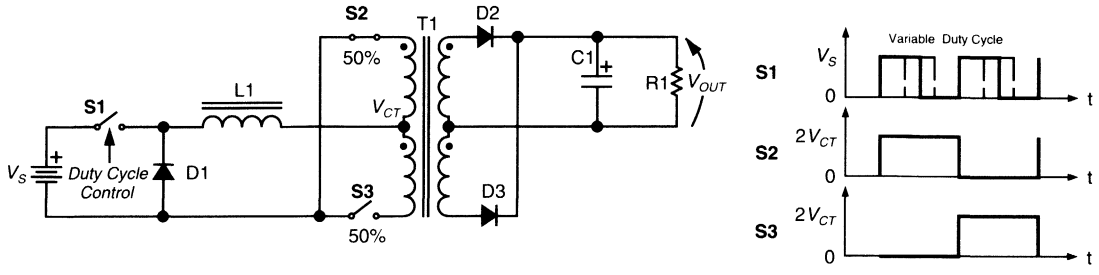


Figure 1. Basic Elements of a Current-Fed Push-Pull Topology

300 Watt Off-Line Current-Fed SMPS

Input and Start-up

Referring to figure 3, AC line voltage is rectified and filtered providing the necessary start-up voltage to the MIC3833 via R6 and R7 charging C9. Once the UVLO limit of the IC is exceeded, pulses from the PWM output are applied to Q2's gate charging L3 and supplying center tap voltage to T3. At the same time, Q and $\overline{Q}$ drive Q3 and Q4 alternately through gate drive transformer T2. T3 transformers T3's center tap voltage and applies it to the output rectifiers. Once the +5V output reaches approximately 5V, current mode PWM operation begins due to the action of U2 sensing the output to be within regulation and sending this information to the inverting input of the MIC3833 through the optocoupler U2.

Maximum Duty Cycle

Maximum duty cycle of the PWM output is held below 50% by dividing V_{REF} with R21 and R23 and applying this voltage to the MDC pin of the MIC3833.

Current Limiting

Cycle-by-cycle current limiting and current mode operation is implemented using the CMR pin of U1 from the current induced voltage across resistors R13 through R15. Current limiting of the individual output is performed by sensing the output current with T4 for the +5V output and T6 for the +12V output. These currents are transformed, rectified, terminated, and diode OR'ed into the shutdown pin of the MIC3833. A voltage greater than 1.25V on this pin will terminate PWM operation of the IC causing the output voltage(s) to drop with increased load beyond the current limit point.

R22 and C17 perform front edge blanking of the PWM output to prevent false termination of this output from the initial spike when Q2 is turned on.

+12V and –12V Outputs

Post regulation of the +12V output is provided to improve its load regulation. Operational amplifier U5 senses the +12V output and corrects it by controlling the voltage drop across T5's primary which in turn adds voltage to the +12V output through T5's secondaries as required to maintain a steady load independent output. The –12V output is provided by a 1 amp 3-terminal regulator U4.

Leakage inductance spikes from the main transformer T3 are suppressed by R10 and C12 while the catch diode D4 is snubbed by D6, C13, and R12. Although a surge limiting thermistor could have been used for in-rush limiting, this function is provided by R3 initially until Q1 is turned on shunting R3 and allowing a low dissipation path for AC current.

Efficiency

At 115VAC in and the output loaded to 300 watts, the circuit efficiency is 68%. Load and line regulation on all outputs is better than ±1%.

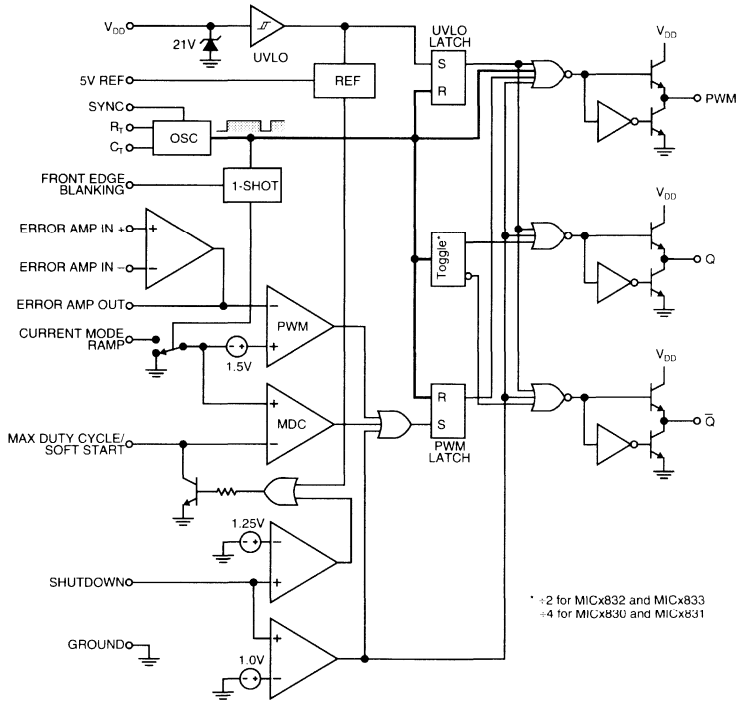


Figure 2. Functional Diagram

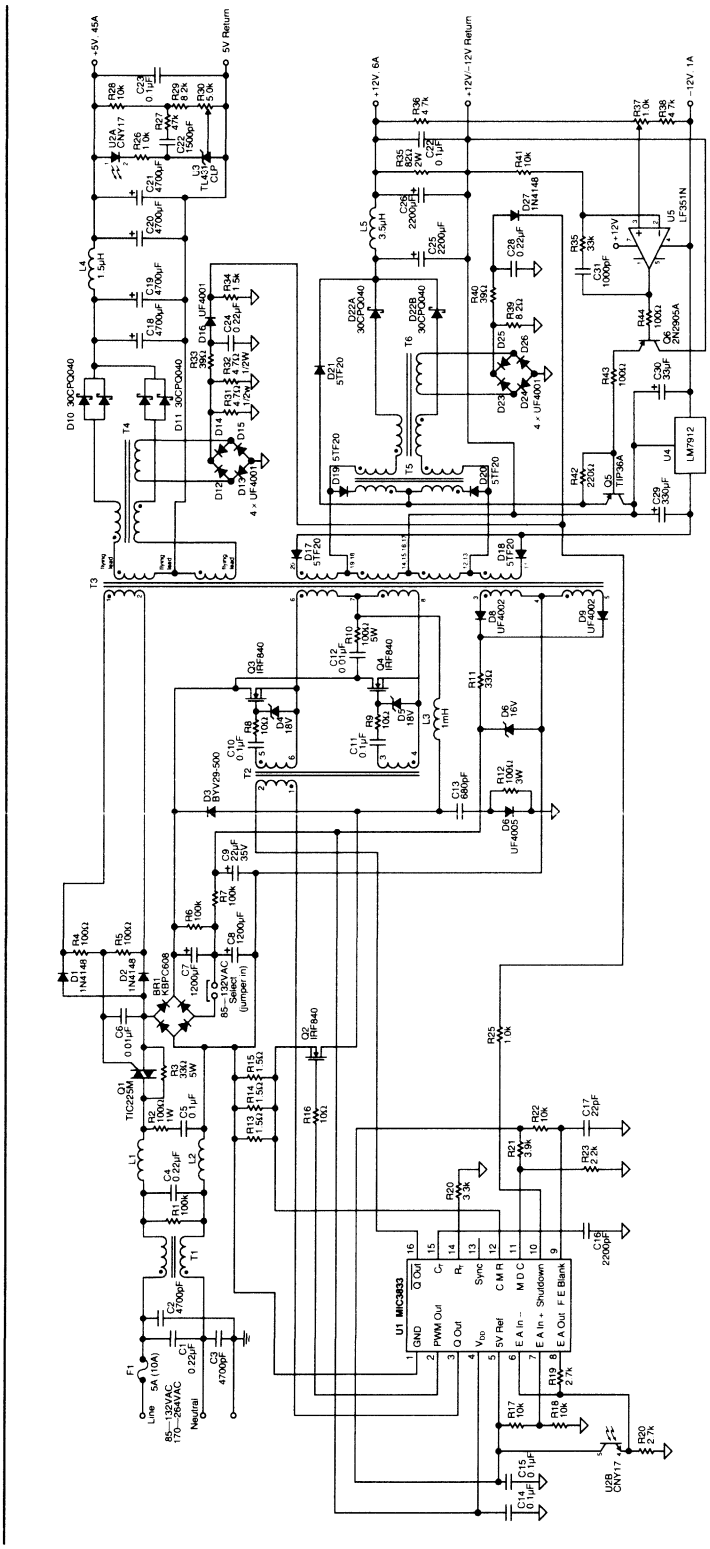


Figure 3. 300W Off-Line Current-Fed Switch Mode Power Supply

SECTION 8 : OPEN DRAIN POWER SWITCHES

Open Drain Power Switch Selection Guide

Device	Function	Logic	Single	Dual	Current	ON Resistance	Package
MIC4401	Open Drain Switch	Inverting	•		6A	1.7Ω	8-pin DIP, SOIC
MIC4402	Open Drain Switch	Non-Inverting	•		6A	1.7Ω	8-pin DIP, SOIC
MIC4403	Floating Load Switch	–	•		1.5A	3Ω	8-pin DIP, SOIC
MIC4604	Open Drain Switch	Inverting		•	1.5A	7Ω	8-pin DIP, SOIC
MIC4605	Open Drain Switch	Non-Inverting		•	1.5A	7Ω	8-pin DIP, SOIC
MIC4606	Open Drain Switch	Inverting		•	3A	3.5Ω	8-pin DIP, SOIC
MIC4607	Open Drain Switch	Non-Inverting		•	3A	3.5Ω	8-pin DIP, SOIC
MIC4608	Open Drain Switch	Inverting	•		9A	1.0Ω	8-pin DIP, SOIC
MIC4609	Open Drain Switch	Non-Inverting	•		9A	1.0Ω	8-pin DIP, SOIC
MIC4610	Open Drain Switch	Inverting	•		12A	1.0Ω	8-pin DIP, SOIC
MIC4611	Open Drain Switch	Non-Inverting	•		12A	1.0Ω	8-pin DIP, SOIC

MIC4401/4402

6A Open Drain Power Switch

Preliminary Information

General Description

The MIC4401/4402 are BiCMOS/DMOS buffer-drivers constructed with complementary MOS outputs, where the drains of the final output totem poles have been left disconnected so individual connections can be made to the pull-up and pull-down sections of the output, thus allowing the user to define the rates of rise and fall times desired for a capacitive load, or a reduced output swing if driving a resistive load, or to limit base current when driving a bipolar transistor. Minimum rise and fall times, with no resistors, will be less than 30ns for a 10,000pF load. There is no upper limit.

These devices are rugged due to extra steps taken to protect them from failures. A modern Bipolar/CMOS/DMOS process guarantees freedom from latchup. Proprietary circuits allow the input to swing negative as much as 5V without damaging the part.

For driving MOSFETs in motor-control applications, where slow-on/fast-off operation is desired, the MIC4401/4402 is superior to the previously-used technique of adding a diode-resistor combination between the driver output and the MOSFET, because it allows accurate control of turn-on, while maintaining fast turn-off and maximum noise immunity for the device being driven.

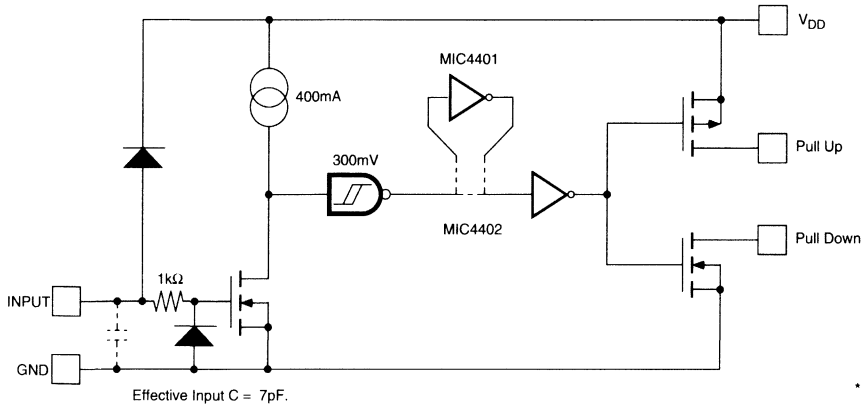
Features

- Independently Programmable Rise and Fall Times
- High Peak Output Current ..... 6A peak
- Low Output Impedance ..... 1.7Ω typ
- High Speed t_R, t_F ..... <20 ns with 2500pF load
- Short Delay Times ..... 25ns Typical
- Wide Operating Range ..... 4.5V to 18V
- Latch-up Protected: Fully Isolated Process is Inherently Immune to any Latchup.
- Input Withstands Negative Swings to –5V
- ESD Protected 2kV

Applications

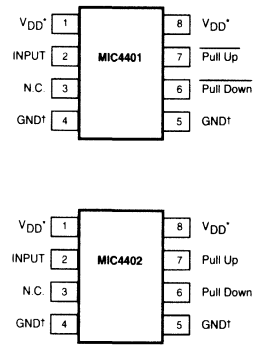
- Motor Controls
- Self-Commutating MOSFET Bridge Driver
- Driving Bipolar Transistors
- Driver for Non-overlapping Totem Poles
- Reach-Up/Reach-Down Driver

Functional Diagram



Effective Input C = 7pF.

Pin Configuration



* Pins 1 and 8 must be externally connected for proper operation.

† Pins 4 & 5 must be externally connected for proper operation.

When used to drive bipolar transistors, this driver maintains high speeds and allows insertion of a base current-limiting resistor, and also provides a separate half-output for fast turn-off. By proper positioning of the resistor, either NPN or PNP transistors can be driven.

For driving many loads in low-power systems, this driver, since it has very low quiescent current (80µA) and eliminates shoot-through current in the output stage, requires significantly less power than other drivers. This can be helpful in meeting low-power budgets.

Due to independent drains, this device can also be used as an open-drain buffer/driver where both drains are available in one device, thus minimizing chip count. An unused pull-down should be returned to the ground; an unused pull-up should be returned to V_{DD}. This is to prevent static damage. Alternatively, in situations requiring greater current-carrying capacity, multiple MIC4608 or MIC4608s may be paralleled.

The MIC4608/4609 will not latch under any conditions within its power and voltage ratings. It is not subject to damage when up to 5V of noise spiking of either polarity occurs on the ground pin. It can accept, without damage or logic upset, up to 1.5 amps of reverse current (of either polarity) being forced back into the outputs.

Absolute Maximum Ratings (Note 1)

Supply Voltage ..... +22V
Logic Input Voltage ..... V_{DD} + 0.3V to GND – 5V
Logic Input Current ($V_{IN} > V_{DD}$) 50mA
Maximum Die Temperature ..... +150°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Power Dissipation, $T_A \leq 25°C$
PDIP 1W
SOIC 500mW
CerDIP 800mW
Package Thermal Resistance
CerDIP θ_{JA} ..... 150°C/W
CerDIP θ_{JC} ..... 55°C/W
PDIP θ_{JA} ..... 125°C/W
PDIP θ_{JC} ..... 45°C/W
SOIC θ_{JA} ..... 160°C/W
SOIC θ_{JC} ..... 75°C/W

Ordering Information

Part Number	Logic	Package	Temperature Range
MIC4401AJ	Inverting	8-pin CerDIP	–55°C to +125°C
MIC4401BN	Inverting	8-pin PDIP	–40°C to +85°C
MIC4401BM	Inverting	8-pin SOIC	–40°C to +85°C
MIC4401CN	Inverting	8-pin PDIP	0°C to +70°C
MIC4402AJ	Non-Inverting	8-pin CerDIP	–55°C to +125°C
MIC4402BN	Non-Inverting	8-pin PDIP	–40°C to +85°C
MIC4402BM	Non-Inverting	8-pin SOIC	–40°C to +85°C
MIC4402CN	Non-Inverting	8-pin PDIP	0°C to +70°C

Note 1: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability. Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields.

Electrical Characteristics

Unless otherwise specified, specifications measured at $T_A = 25°C$ with $4.5V \le V_{DD} \le 18V$.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1 High Input Voltage		2.4		V_{DD} + 0.3	V
V_{IL}	Logic 0 Low Input Voltage		–5		0.8	V
I_{IN}	Input Current	$0V \le V_{IN} \le V_{DD}$	–10		10	µA
Output						
V_{OH}	High Output Voltage		V_{DD} – 0.025			V
V_{OL}	Low Output Voltage				0.025	V
R_O	Output Resistance, Pull-Up	I_{OUT} = 10mA, V_{DD} = 18V		1.5	2.8	Ω
R_O	Output Resistance, Pull-Down	I_{OUT} = 10mA, V_{DD} = 18V		1.7	2.5	Ω
I_{PK}	Peak Output Current			6		A
I_R	Latch-up Protection Withstand Reverse Current		>1500			mA
Switching Time						
t_R	Rise Time	Figure 1, C_L = 2500pF		12	35	ns
t_F	Fall Time	Figure 1, C_L = 2500pF		13	35	ns
t_{D1}	Delay Time	Figure 1, C_L = 2500pF		18	75	ns
t_{D2}	Delay Time	Figure 1, C_L = 2500pF		48	75	ns
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V		0.45	1.5	mA
		V_{IN} = 0V		0.09	0.15	mA

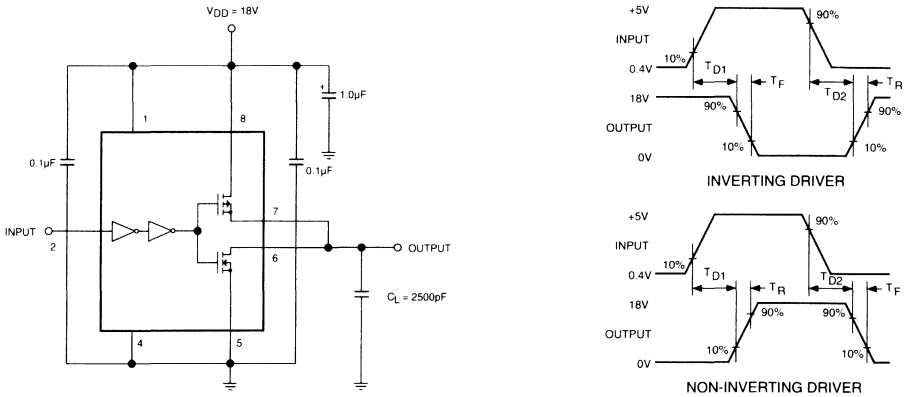


Figure 1. MIC4401/4402 Switching time test circuit.

Electrical Characteristics, continued

Specifications measured **over operating temperature range** with $4.5V \leq V_{DD} \leq 18V$, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1 High Input Voltage		2.4			V
V_{IL}	Logic 0 Low Input Voltage				0.8	V
I_{IN}	Input Current	$0V \leq V_{IN} \leq V_{DD}$	–10		10	µA
Output						
V_{OH}	High Output Voltage		$V_{DD} - 0.025$			V
V_{OL}	Low Output Voltage				0.025	V
R_O	Output Resistance, Pull-Up	$I_{OUT} = 10mA$, $V_{DD} = 18V$		2.2	5	Ω
R_O	Output Resistance, Pull-Down	$I_{OUT} = 10mA$, $V_{DD} = 18V$		3.5	5	Ω
Switching Time						
t_R	Rise Time	Figure 1, $C_L = 2500pF$		16	60	ns
t_F	Fall Time	Figure 1, $C_L = 2500pF$		25	60	ns
t_{D1}	Delay Time	Figure 1, $C_L = 2500pF$		25	100	ns
t_{D2}	Delay Time	Figure 1, $C_L = 2500pF$		70	100	ns
Power Supply						
I_S	Power Supply Current	$V_{IN} = 3V$		0.5	3	mA
		$V_{IN} = 0V$		0.12	0.4	mA

MIC4403

1.5A High Speed Floating Load Switch

Preliminary Information

General Description

The MIC4403 is a modified version of the MIC4425 power MOSFET driver, intended to drive floating or isolated loads requiring high-current pulses. The load is intended to be connected between the outputs without other reference to supply or ground. Only when both logic inputs are high and the V_{DD} supply is energized, is power supplied to the load. This construction allows the implementation of a wide variety of redundant input controllers.

The low off-state output leakage and independence of the two half-circuits permit a wide variety of testing schemes to be utilized to assure functionality. The high peak current capability, short internal delays, and fast output rise and fall times ensure sufficient power will be available to the load when it is needed. The TTL and CMOS compatible inputs allow operation from a wide variety of input devices. The ability to swing the inputs negative without affecting device performance allows negative biases to be placed on the inputs for greater safety. In addition, the capacitive nature of the inputs allows the use of series resistors on the inputs for extra noise suppression.

Input voltage excursions above the supply voltage or below ground are clamped internally without damaging the device. The output stages are power CMOS and DMOS FETs with high speed body diodes to prevent damage to the driver from inductive kickbacks.

Features

- Built Using Contemporary BiCMOS/DMOS Process
- Latch-Up Protected: Fully Isolated Process is Inherently Immune to any Latch-Up
- Low Quiescent Current ..... 300µA Max
- Low Capacitive Inputs With 300mV Hysteresis
- Both Inputs Must Be Driven to Drive Load
- Low Output Leakage
- High Peak Current Capability
- Fast Output Rise Time
- Outputs Individually Testable
- 3A Single Ended (1.5A with Floating Load)

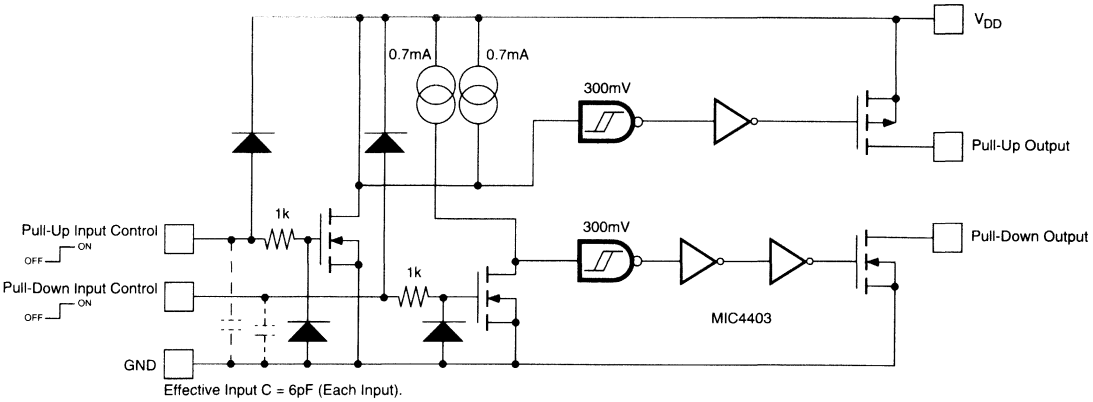
Applications

- Squib Drivers
- Isolated Load Drivers
- Pulsers
- Safety Interlocks

Ordering Information

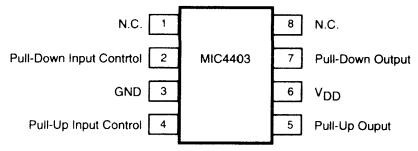
Part Number	Temperature Range	Package
MIC4403AJ	–55°C to +125°C	8-pin CerDIP
MIC4403BM	–40°C to +85°C	8-pin SOIC
MIC4403BN	–40°C to +85°C	8-pin PDIP
MIC4403CN	0°C to +70°C	8-Pin PDIP

Functional Diagram



Effective Input C = 6pF (Each Input).

Pin Configuration



Absolute Maximum Ratings (Note 1)

Supply Voltage ..... +22V
Maximum Die Temperature ..... +150°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

Package Thermal Resistance
CerDIP θ_{JA} ..... 150°C/W
CerDIP θ_{JC} ..... 55°C/W
PDIP θ_{JA} ..... 125°C/W
PDIP θ_{JC} ..... 45°C/W
SOIC θ_{JA} ..... 250°C/W
SOIC θ_{JC} ..... 75°C/W

Note 1: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability. Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields.

Electrical Characteristics

Unless otherwise specified, specifications measured at $T_A = 25°C$ with $4.5V \leq V_{DD} \leq 18V$.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1 High Input Voltage		2.4		$V_{DD} + 0.3$	V
V_{IL}	Logic 0 Low Input Voltage		–5		0.8	V
I_{IN}	Input Current	$0V \leq V_{IN} \leq 5V_{DD}$	–1	±0.01	1	µA
Output						
V_{OH}	High Output Voltage		$V_{DD} - 0.025$			V
V_{OL}	Low Output Voltage				0.025	V
R_O	Output Resistance, Pull-Up	$I_{OUT} = 10mA$, $V_{DD} = 18V$		2.8	5	Ω
R_O	Output Resistance, Pull-Down	$I_{OUT} = 10mA$, $V_{DD} = 18V$		3.5	5	Ω
I_{PK}	Peak Output Current			1.5		A
Switching Time						
t_R	Rise Time	Figure 1, $C_L = 1800pF$		23	35	ns
t_F	Fall Time	Figure 1, $C_L = 1800pF$		25	35	ns
t_{D1}	Delay Time	Figure 1, $C_L = 1800pF$		17	75	ns
t_{D2}	Delay Time	Figure 1, $C_L = 1800pF$		23	75	ns
Power Supply						
I_S	Power Supply Current	$V_{IN} = 3V$ (both inputs)		1.4	2.5	mA
		$V_{IN} = 0V$ (both inputs)		0.17	0.25	mA

Electrical Characteristics, continued

Specifications measured **over operating temperature range** with 4.5V ≤ V_{DD} ≤18V, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1 High Input Voltage		2.4		V_{DD} + 0.3	V
V_{IL}	Logic 0 Low Input Voltage		–5		0.8	V
I_{IN}	Input Current	0V ≤ V_{IN} ≤ V_{DD}	–10	±0.01	10	µA
Output						
V_{OH}	High Output Voltage		V_{DD} – 0.025			V
V_{OL}	Low Output Voltage				0.025	V
R_O	Output Resistance, Pull-Up	I_{OUT} = 10mA, V_{DD} = 18V V_{IN} ≥ 2.4V		3.7	8	Ω
R_O	Output Resistance, Pull-Down	I_{OUT} = –10mA, V_{DD} = 18V V_{IN} ≥ 2.4V		5.5	8	Ω
Switching Time						
t_R	Rise Time	Figure 1, C_L = 1800pF		24	60	ns
t_F	Fall Time	Figure 1, C_L = 1800pF		32	60	ns
t_{D1}	Delay Time	Figure 1, C_L = 1800pF		19	100	ns
t_{D2}	Delay Time	Figure 1, C_L=1800pF		19	100	ns
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V (both inputs)		1.6	3.5	mA
		V_{IN} = 0V (both inputs)		0.25	0.3	mA

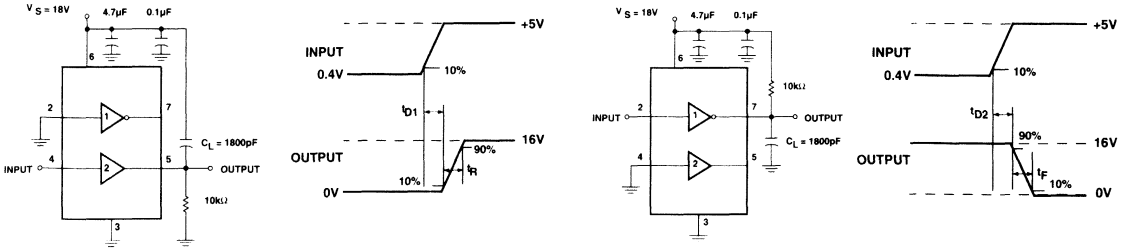


Figure 1. MIC4403 Switching time test circuit.

MIC4604/4605

1.5A Dual Open Drain Power Switch

Preliminary Information

General Description

The MIC4604 and MIC4605 are BiCMOS/DMOS buffer-drivers constructed with complementary MOS outputs, where the drains of the final output totem pole have been left disconnected so individual connections can be made to the pull-up and pull down sections of the output. This allows the insertion of individual drain-current-limiting resistors in the pull up and pull down sections of the output, thus allowing the user to define the rates of rise and fall desired for a capacitive load, or a reduced output swing if driving a resistive load, or to limit base current when driving a bipolar transistor. Minimum rise and fall times, with no resistors, will be less than 20ns for a 1000pF load. There is no upper limit.

These devices are rugged due to extra steps taken to protect them from failures. A modern Bipolar/CMOS/DMOS process guarantees freedom from latchup. Proprietary circuits allow the input to swing negative as much as 5V without damaging the part.

For driving MOSFETs in motor-control applications, where slow on/fast off operation is desired, these devices are superior to the previously used technique of adding a diode resistor combination between the driver output and the MOSFET, because they allow accurate control of turn-ON, while maintaining fast turn-OFF and maximum noise immunity for an OFF device.

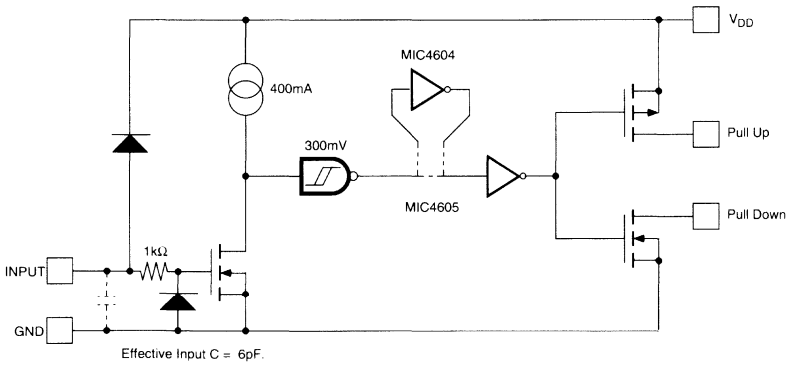
Features

- Independently Programmable Rise and Fall Times
- Low Output Impedance ..... 6Ω Typ
- High Speed t_R, t_F ..... <30ns with 1000pF Load
- Short Delay Times ..... <25ns typ
- Wide Operating Range ..... 4.5V to 18V
- Latch-Up Protection: Fully Isolated Process is Inherently Immune to to Any Latch-up
- Input Withstands Negative Swings to –5V
- ESD Protected 2kV

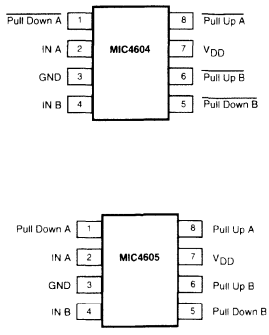
Applications

- Motor Controls
- Self-Commutating MOSFET Bridge Driver
- Driving Bipolar Transistors
- Drive for Nonoverlapping Totem Poles
- Level Shifters
- Power Management

Functional Diagram



Pin Configuration



When used to drive bipolar transistors, this driver maintains high speeds and allows insertion of a base current-limiting resistor, and also provides a separate half-output for fast turn-off. By proper positioning of the resistor, either NPN or PNP transistors can be driven.

These drivers, since they eliminate shoot-through currents in the output stage, require significantly less power at higher frequencies. This can be helpful in meeting low-power budgets.

Due to independent drains, this device can also be used as an open-drain buffer/driver where both drains are available in one device, thus minimizing chip count. An unused pull-down should be returned to the ground; an unused pull-up should be returned to V_{DD}. This is to prevent static damage. Alternatively, in situations requiring greater current-carrying capacity, multiple MIC4604 or MIC4605s may be paralleled.

The MIC4604/4605 will not latch under any conditions within its power and voltage ratings. It is not subject to damage when up to 5V of noise spiking of either polarity occurs on the ground pin. It can accept, without damage or logic upset, up to 1.5 amps of reverse current (of either polarity) being forced back into the outputs.

Absolute Maximum Ratings (Note 1)

Supply Voltage ..... +22V
Maximum Chip Temperature ..... +150°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Package Thermal Resistance
CerDIP θ_{J-A} ..... 150°C/W
CerDIP θ_{J-C} ..... 55°C/W
PDIP θ_{J-A} ..... 125°C/W
PDIP θ_{J-C} ..... 45°C/W
SOIC θ_{J-A} ..... 250°C/W
SOIC θ_{J-C} ..... 75°C/W

8

Ordering Information

Part Number	Logic	Package	Temperature Range
MIC4604AJ	Inverting	8-pin CerDIP	–55°C to +125°C
MIC4604BM	Inverting	8-pin SOIC	–40°C to +85°C
MIC4604BN	Inverting	8-pin PDIP	–40°C to +85°C
MIC4605AJ	Non-Inverting	8-pin CerDIP	–55°C to +125°C
MIC4605BM	Non-Inverting	8-pin SOIC	–40°C to +85°C
MIC4605BN	Non-Inverting	8-pin PDIP	–40°C to +85°C

Note 1: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability. Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields.

Electrical Characteristics

Unless otherwise specified, specifications measured at $T_A = 25°C$ with $4.5V \leq V_{DD} \leq 18V$.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1 High Input Voltage		2.4		V_{DD} + 0.3	V
V_{IL}	Logic 0 Low Input Voltage		–5		0.8	V
I_{IN}	Input Current	$0V \leq V_{IN} \leq V_{DD}$	–1		1	µA
Output						
V_{OH}	High Output Voltage		V_{DD} – 0.025			V
V_{OL}	Low Output Voltage				0.025	V
R_O	Output Resistance, Pull-Up	I_{OUT} = 10mA, V_{DD} = 18V		6	10	Ω
R_O	Output Resistance, Pull-Down	I_{OUT} = 10mA, V_{DD} = 18V		6	10	Ω
I_{PK}	Peak Output Current	Any Drain		1.5		A
I_R	Latch-up Protection	Any Drain Reverse Current	>500			mA
Switching Time						
t_R	Rise Time	Figure 1, C_L = 1000pF		18	30	ns
t_F	Fall Time	Figure 1, C_L = 1000pF		27	35	ns
t_{D1}	Delay Time	Figure 1, C_L = 1000pF		17	30	ns
t_{D2}	Delay Time	Figure 1, C_L = 1000pF		23	50	ns
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V (both inputs)		1.4	2.5	mA
		V_{IN} = 0V (both inputs)		0.18	0.25	mA

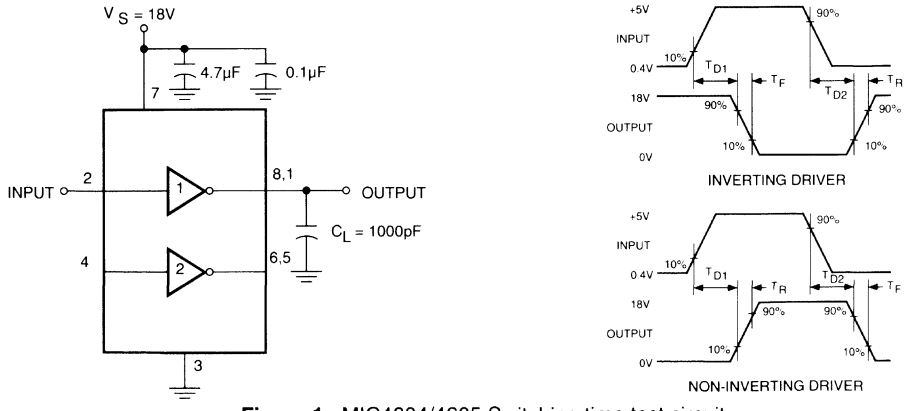


Figure 1. MIC4604/4605 Switching time test circuit.

Electrical Characteristics, continued

Specifications measured **over operating temperature range** with 4.5V ≤ V_{DD} ≤ 18V, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1 High Input Voltage		2.4		V_{DD} + 0.3	V
V_{IL}	Logic 0 Low Input Voltage				0.8	V
I_{IN}	Input Current	0V ≤ V_{IN} ≤ V_{DD}	–10		10	µA
Output						
V_{OH}	High Output Voltage		V_{DD} – 0.025			V
V_{OL}	Low Output Voltage				0.025	V
R_O	Output Resistance, Pull-Up	I_{OUT} = 10mA, V_{DD} = 18V		8	12	Ω
R_O	Output Resistance, Pull-Down	I_{OUT} = 10mA, V_{DD} = 18V		9	12	Ω
I_{PK}	Peak Output Current	Any Drain		1.5		A
I_R	Latch-up Protection	Any Drain Reverse Current	>500			mA
Switching Time						
t_R	Rise Time	Figure 1, C_L = 1000pF		20	40	ns
t_F	Fall Time	Figure 1, C_L = 1000pF		30	40	ns
t_{D1}	Delay Time	Figure 1, C_L = 1000pF		20	40	ns
t_{D2}	Delay Time	Figure 1, C_L = 1000pF		30	60	ns
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V (both inputs)		1.5	3.5	mA
		V_{IN} = 0V (both inputs)		0.2	0.3	mA

8

MIC4606/4607

3A Dual Open Drain Power Switches

Preliminary Information

General Description

The MIC4606 and MIC4607 are BiCMOS/DMOS buffer-drivers constructed with complementary MOS outputs, where the drains of the final output totem pole have been left disconnected so individual connections can be made to the pull-up and pull-down sections of the output. This allows the insertion of individual drain current-limiting resistors in the pull-up and pull-down sections of the outputs, thus allowing the user to define the rates of rise and fall desired for a capacitive load, or to limit base current when driving a bipolar transistor. Minimum rise and fall times, with no resistors, will be less than 25ns for a 1800pF load.

These devices are rugged due to extra steps taken to protect them from failures. A modern Bipolar/CMOS/DMOS process guarantees freedom from latchup. Proprietary circuits allow the input to swing negative as much as 5V without damaging the part.

For driving MOSFETs in motor-control applications, where slow-on/fast-off operation is desired, these devices are superior to the previously-used technique of adding a diode-resistor combination between the driver output and the MOSFET, because they allow accurate control of turn-on, while maintaining fast turn-off and maximum noise immunity for the device being driven.

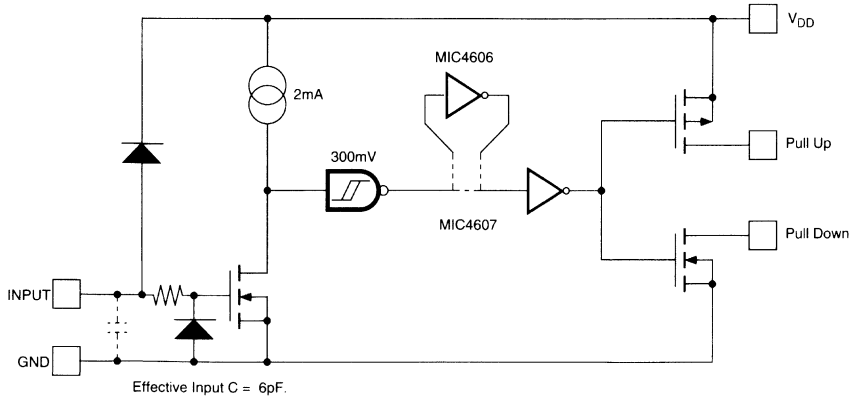
Features

- Independently-Programmable Rise and Fall Times
- Low Output Impedance ..... 3Ω typ.
- High Speed t_R, t_F ..... <25ns with 1800pF Load
- Short Delay Times ..... <25ns typ.
- Wide Operating Range ..... 4.5V to 18V
- Latch-Up Protected: Fully Isolated Process is Inherently Immune to any Latchup
- Input Withstands Negative Swings to –5V
- ESD Protected 2kV

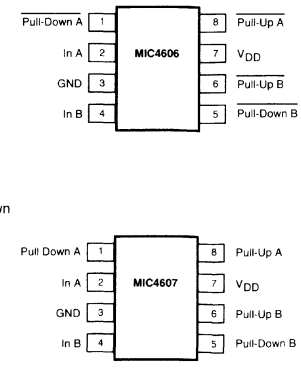
Applications

- Motor Controls
- Self-Commutating MOSFET Bridge Driver
- Driving Bipolar Transistors
- Driver for Nonoverlapping Totem Poles
- Level Shifters
- Power Management

Functional Diagram



Pin Description



When used to drive bipolar transistors, these drivers allow insertion of a base current limiting resistor, while providing a separate half-output for fast turn-off. By proper positioning of the resistor, either NPN or PNP transistors can be driven.

These drivers, since they have very low quiescent current (<250μA) and eliminate shoot-through currents in the output stage, require significantly less power than similar drivers. This can be helpful in meeting low-power budgets.

Due to independent drains, this device can also be used as an open-drain buffer/driver where both drains are available in one device, thus minimizing chip count. An unused pull-down should be returned to the ground; an unused pull-up should be returned to V_{DD}. This is to prevent static damage. Alternatively, in situations requiring greater current-carrying capacity, multiple MIC4606 or MIC4607s may be paralleled.

The MIC4606/4407 will not latch under any conditions within its power and voltage ratings. It is not subject to damage when up to 5V of noise spiking of either polarity occurs on the ground pin. It can accept, without damage or logic upset, up to 500mA of reverse current (of either polarity) being forced back into the outputs All terminals are fully protected against up to 2kV of electrostatic discharge.

Absolute Maximum Ratings (Note 1)

Supply Voltage ..... +22V
Maximum Die Temperature ..... +150°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Package Thermal Resistance
CerDIP θ_{JA} ..... 150°C/W
CerDIP θ_{JC} ..... 55°C/W
PDIP θ_{JA} ..... 125°C/W
PDIP θ_{JC} ..... 45°C/W
SOIC θ_{JA} ..... 250°C/W
SOIC θ_{JC} ..... 75°C/W

Ordering Information

Part Number	Logic	Package	Temperature Range
MIC4606AJ	Inverting	8-pin CerDIP	–55°C to +125°C
MIC4606BN	Inverting	8-pin PDIP	–40°C to +85°C
MIC4606BM	Inverting	8-pin SOIC	–40°C to +85°C
MIC4607AJ	Noninverting	8-pin CerDIP	–55°C to +125°C
MIC4607BN	Noninverting	8-pin PDIP	–40°C to +85°C
MIC4607BM	Noninverting	8-pin SOIC	–40°C to +85°C

8

Note 1: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability. Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields.

Electrical Characteristics

Unless otherwise specified, specifications measured at $T_A = 25°C$ with $4.5V \leq V_{DD} \leq 18V$.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1 High Input Voltage		2.4		V_{DD} + 0.3	V
V_{IL}	Logic 0 Low Input Voltage		–5		0.8	V
I_{IN}	Input Current	$0V \leq V_{IN} \leq V_{DD}$	–1		1	µA
Output						
V_{OH}	High Output Voltage		V_{DD} – 0.025			V
V_{OL}	Low Output Voltage				0.025	V
R_O	Output Resistance, Pull-Up	I_{OUT} = 10mA, V_{DD} = 18V		2.8	5	Ω
R_O	Output Resistance, Pull-Down	I_{OUT} = 10mA, V_{DD} = 18V		5.5	5	Ω
I_{PK}	Peak Output Current	Any Drain		3		A
I_R	Latch-up Protection Withstand Reverse Current	Any Drain	>500			mA
Switching Time						
t_R	Rise Time	Figure 1, C_L = 1800pF		23	35	ns
t_F	Fall Time	Figure 1, C_L = 1800pF		25	35	ns
t_{D1}	Delay Time	Figure 1, C_L = 1800pF		17	75	ns
t_{D2}	Delay Time	Figure 1, C_L = 1800pF		23	75	ns
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V (both inputs)		1.4	2.5	mA
		V_{IN} = 0V (both inputs)		0.17	0.25	mA

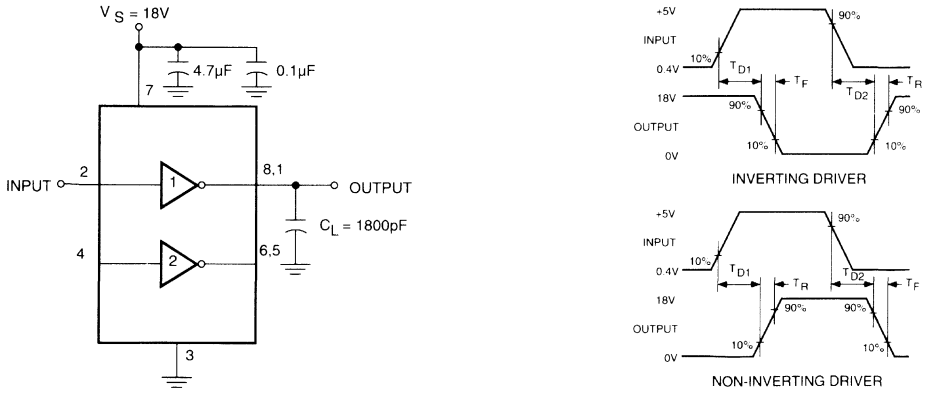


Figure 1. MIC4606/4607 Switching time test circuit.

Electrical Characteristics (continued)

Specifications measured **over operating temperature range** with $4.5V \leq V_{DD} \leq 18V$, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1 High Input Voltage		2.4		V_{DD} + 0.3	V
V_{IL}	Logic 0 Low Input Voltage		–5		0.8	V
I_{IN}	Input Current	$0V \leq V_{IN} \leq V_{DD}$	–10		10	µA
Output						
V_{OH}	High Output Voltage		V_{DD} – 0.025			V
V_{OL}	Low Output Voltage				0.025	V
R_O	Output Resistance, Pull-Up	I_{OUT} = 10mA, V_{DD} = 18V		3.7	8	Ω
R_O	Output Resistance, Pull-Down	I_{OUT} = 10mA, V_{DD} = 18V		5.5	8	Ω
I_{PK}	Peak Output Current	Any Drain		3		A
I_R	Latch-up Protection Withstand	Any Drain Reverse Current	>500			mA
Switching Time						
t_R	Rise Time	Figure 1, C_L = 1800pF		24	60	ns
t_F	Fall Time	Figure 1, C_L = 1800pF		32	60	ns
t_{D1}	Delay Time	Figure 1, C_L = 1800pF		19	100	ns
t_{D2}	Delay Time	Figure 1, C_L=1800pF		27	100	ns
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V (both inputs)		1.6	3.5	mA
		V_{IN} = 0V (both inputs)		0.25	0.3	mA

MIC4608/4609

9A Open Drain Power Switch

Preliminary Information

General Description

The MIC4608/4609 are BiCMOS/DMOS buffer-drivers constructed with complementary MOS outputs, where the drains of the final output totem poles have been left disconnected so individual connections can be made to the pull-up and pull-down sections of the output, thus allowing the user to define the rates of rise and fall times desired for a capacitive load, or a reduced output swing if driving a resistive load, or to limit base current when driving a bipolar transistor. Minimum rise and fall times, with no resistors, will be less than 30ns for a 10,000pF load. There is no upper limit.

These devices are rugged due to extra steps taken to protect them from failures. A modern Bipolar/CMOS/DMOS process guarantees freedom from latchup. Proprietary circuits allow the input to swing negative as much as 5V without damaging the part.

For driving MOSFETs in motor-control applications, where slow-on/fast-off operation is desired, the MIC4608/4609 is superior to the previously-used technique of adding a diode-resistor combination between the driver output and the MOSFET, because it allows accurate control of turn-on, while maintaining fast turn-off and maximum noise immunity for the device being driven.

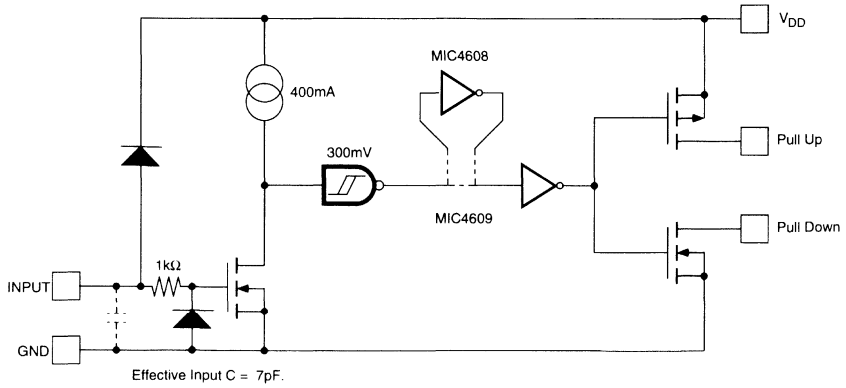
Features

- Independently Programmable Rise and Fall Times
- High Peak Output Current ..... 9A peak
- Low Output Impedance ..... 1Ω typ.
- High Speed t_R, t_F ..... <30ns with 10,000pF
- Short Delay Times ..... <30ns typ.
- Wide Operating Range ..... 4.5V to 18V
- Latch-up Protected: Fully Isolated Process is Inherently Immune to Any Latch-Up.
- Input Withstands Negative Swings to –5V
- ESD Protected 2kV

Applications

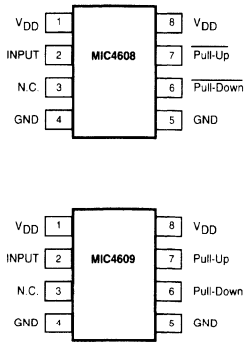
- Power Switch
- Motor Controls
- Self-Commutating MOSFET Bridge Driver
- Driving Bipolar Transistors
- Driver for Nonoverlapping Totem Poles
- Pulse Generator
- Line Driver
- Power Management
- Level Shifters

Functional Diagram



Effective Input C = 7pF.

Pin Configuration



When used to drive bipolar transistors, this driver maintains high speeds and allows insertion of a base current-limiting resistor, and also provides a separate half-output for fast turn-off. By proper positioning of the resistor, either NPN or PNP transistors can be driven.

For driving many loads in low-power systems, this driver, because it has very low quiescent current (<80μA) and eliminates shoot-through current in the output stage, requires significantly less power than similar drivers and can be helpful in meeting low-power budgets.

Due to independent drains, this device can also be used as an open-drain buffer/driver where both drains are available in one device, thus minimizing chip count. An unused pull-down should be returned to the ground; an unused pull-up should be returned to V_{DD}. This is to prevent static damage. Alternatively, in situations requiring greater current-carrying capacity, multiple MIC4608 or MIC4609s may be paralleled.

The MIC4608/4609 will not latch under any conditions within its power and voltage ratings. It is not subject to damage when up to 5V of noise spiking of either polarity occurs on the ground pin. It can accept, without damage or logic upset, up to 1.5 amps of reverse current (of either polarity) being forced back into the outputs.

Absolute Maximum Ratings (Note 1)

Supply Voltage ..... +22V
Maximum Die Temperature ..... +150°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Package Thermal Resistance
CerDIP θ_{JA} ..... 150°C/W
CerDIP θ_{JC} ..... 55°C/W
PDIP θ_{JA} ..... 125°C/W
PDIP θ_{JC} ..... 45°C/W
SOIC θ_{JA} ..... 250°C/W
SOIC θ_{JC} ..... 75°C/W

8

Ordering Information

Part Number	Logic	Package	Temperature Range
MIC4608AJ	Inverting	8-pin CerDIP	–55°C to +125°C
MIC4608BN	Inverting	8-pin PDIP	–40°C to +85°C
MIC4608BM	Inverting	8-pin SOIC	–40°C to +85°C
MIC4609AJ	Non-inverting	8-pin CerDIP	–55°C to +125°C
MIC4609BN	Non-inverting	8-pin PDIP	–40°C to +85°C
MIC4609BM	Non-inverting	8-pin SOIC	–40°C to +85°C

Note 1: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability. Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields.

Electrical Characteristics

Unless otherwise specified, specifications measured at T_A = 25°C with 4.5V ≤ V_{DD} ≤ 18V.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1 High Input Voltage		2.4		V_{DD} + 0.3	V
V_{IL}	Logic 0 Low Input Voltage		–5		0.8	V
I_{IN}	Input Current	0V ≤ V_{IN} ≤ V_{DD}	–10		10	µA
Output						
V_{OH}	High Output Voltage		V_{DD} – 0.025			V
V_{OL}	Low Output Voltage				0.025	V
R_O	Output Resistance, Pull-Up	I_{OUT} = 10mA, V_{DD} = 18V		0.9	1.7	Ω
R_O	Output Resistance, Pull-Down	I_{OUT} = 10mA, V_{DD} = 18V		1.0	2.5	Ω
I_{PK}	Peak Output Current			9		A
I_R	Latch-up Protection Withstand Reverse Current	t < 300µs, Duty Cycle ≤ 2%	>1500			mA
Switching Time						
t_R	Rise Time	Figure 1, C_L = 10,000pF		25	60	ns
t_F	Fall Time	Figure 1, C_L = 10,000pF		25	60	ns
t_{D1}	Delay Time	Figure 1, C_L = 10,000pF		30	60	ns
t_{D2}	Delay Time	Figure 1, C_L = 10,000pF		33	60	ns
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V		0.4	1.5	mA
		V_{IN} = 0V		0.08	0.15	mA

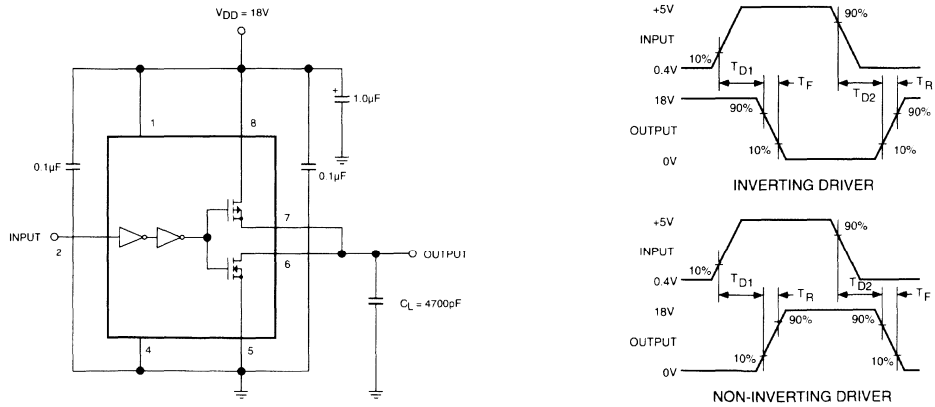


Figure 1. MIC4608/4609 Switching time test circuit.

Electrical Characteristics, continued

Specifications measured **over operating temperature range** with $4.5V \leq V_{DD} \leq 18V$, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1 High Input Voltage		2.4		V_{DD} + 0.3	V
V_{IL}	Logic 0 Low Input Voltage		–5		0.8	V
I_{IN}	Input Current	$0V \leq V_{IN} \leq V_{DD}$	–10		10	µA
Output						
V_{OH}	High Output Voltage		V_{DD} – 0.025			V
V_{OL}	Low Output Voltage				0.025	V
R_O	Output Resistance, Pull-Up	I_{OUT} = 10mA, V_{DD} = 18V		1.4	5	Ω
R_O	Output Resistance, Pull-Down	I_{OUT} = 10mA, V_{DD} = 18V		1.5	5	Ω
Switching Time (Note 1)						
t_R	Rise Time	Figure 1, C_L = 10,000pF		30	80	ns
t_F	Fall Time	Figure 1, C_L = 10,000pF		40	80	ns
t_{D1}	Delay Time	Figure 1, C_L = 10,000pF		30	80	ns
t_{D2}	Delay Time	Figure 1, C_L=10,000pF		40	80	ns
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V		0.6	3	mA
		V_{IN} = 0V		0.1	0.2	mA

8

MIC4610/4611

12A Open Drain Power Switch

Preliminary Information

General Description

The MIC4610/4611 are CMOS buffer-drivers constructed with complementary MOS outputs, where the drains of the final output totem poles have been left disconnected so individual connections can be made to the pull-up and pull-down sections of the output, thus allowing the user to define the rates of rise and fall times desired for a capacitive load, or a reduced output swing if driving a resistive load, or to limit base current when driving a bipolar transistor. Minimum rise and fall times, with no resistors, is 40ns for a 15,000pF load. There is no upper limit.

These devices are rugged due to extra steps taken to protect them from failures. A modern Bipolar/CMOS/DMOS process guarantees freedom from latchup. Proprietary circuits allow the input to swing negative as much as 5V without damaging the part.

For driving MOSFETs in motor-control applications, where slow-on/fast-off operation is desired, the MIC4610/4611 is superior to the previously-used technique of adding a diode-resistor combination between the driver output and the MOSFET, because it allows accurate control of turn-on, while maintaining fast turn-off and maximum noise immunity for the device being driven.

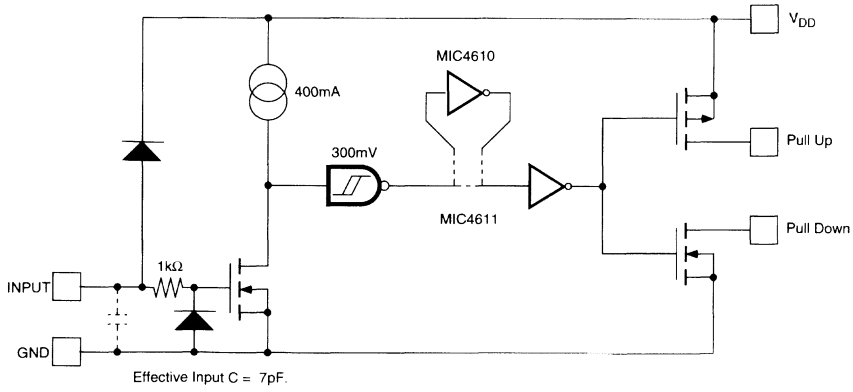
Features

- Independently - Programmable Rise and Fall Times
- High Peak Output Current ..... 12A peak
- Low Output Impedance ..... 1Ω Typ
- High Speed t_R, t_F ..... <40 ns with 15,000pF load
- Short Delay Times ..... 30ns Typical
- Wide Operating Range ..... 4.5V to 18V
- Latch-up Protected: Fully Isolated Process is Inherently Immune to Any Latch-Up.
- Input Withstands Negative Swings to –5V
- ESD Protected 2kV

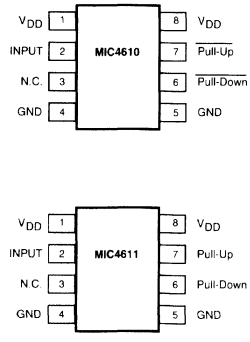
Applications

- Power Switch
- Motor Controls
- Self-Commutating MOSFET Bridge Driver
- Driving Bipolar Transistors
- Driver for Nonoverlapping Totem Poles
- Pulse Generator
- Line Driver
- Power Management
- Level Shifters

Functional Diagram



Pin Configuration



When used to drive bipolar transistors, this driver maintains high speeds and allows insertion of a base current-limiting resistor, and also provides a separate half-output for fast turn-off. By proper positioning of the resistor, either NPN or PNP transistors can be driven.

For driving many loads in low-power systems, this driver, since it has very low quiescent current (<80μA) and eliminates shoot-through current in the output stage, requires significantly less power than similar drivers. This can be helpful in meeting low-power budgets.

Due to independent drains, this device can also be used as an open-drain buffer/driver where both drains are available in one device, thus minimizing chip count. An unused pull-down should be returned to the ground; an unused pull-up should be returned to V_{DD}. This is to prevent static damage. Alternatively, in situations requiring greater current-carrying capacity, multiple MIC4610 or MIC4611s may be paralleled.

The MIC4610/4611 will not latch under any conditions within its power and voltage ratings. It is not subject to damage when up to 5V of noise spiking of either polarity occurs on the ground pin. It can accept, without damage or logic upset, up to 1.5 amps of reverse current (of either polarity) being forced back into the outputs.

Absolute Maximum Ratings

Supply Voltage ..... +22V
Maximum Die Temperature ..... +150°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Package Thermal Resistance
CerDIP θ_{JA} ..... 150°C/W
CerDIP θ_{JC} ..... 55°C/W
PDIP θ_{JA} ..... 125°C/W
PDIP θ_{JC} ..... 45°C/W
SOIC θ_{JA} ..... 250°C/W
SOIC θ_{JC} ..... 75°C/W

8

Ordering Information

Part Number	Logic	Package	Temperature Range
MIC4610AJ	Inverting	8-pin CERDIP	–55°C to +125°C
MIC4610BN	Inverting	8-pin PDIP	–40°C to +85°C
MIC4610BM	Inverting	8-pin SOIC	–40°C to +85°C
MIC4611AJ	Non-inverting	8-pin CERDIP	–55°C to +125°C
MIC4611BN	Non-inverting	8-pin PDIP	–40°C to +85°C
MIC4611BM	Non-inverting	8-pin SOIC	–40°C to +85°C

Note 1: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability. Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields.

Electrical Characteristics

Unless otherwise specified, specifications measured at $T_A = 25°C$ with $4.5V \leq V_{DD} \leq 18V$.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1 High Input Voltage		2.4		V_{DD} + 0.3	V
V_{IL}	Logic 0 Low Input Voltage		–5		0.8	V
I_{IN}	Input Current	$0V \leq V_{IN} \leq V_{DD}$	–10		10	µA
Output						
V_{OH}	High Output Voltage		V_{DD} – 0.025			V
V_{OL}	Low Output Voltage				0.025	V
R_O	Output Resistance, Pull-Up	I_{OUT} = 10mA, V_{DD} = 18V		1.0	1.5	Ω
R_O	Output Resistance, Pull-Down	I_{OUT} = 10mA, V_{DD} = 18V		0.9	1.5	Ω
I_{PK}	Peak Output Current			12		A
I_R	Latch-up Protection Withstand Reverse Current	t < 300µs, Duty Cycle ≤ 2%	>1500			mA
Switching Time						
t_R	Rise Time	Figure 1, C_L = 15,000pF		40	60	ns
t_F	Fall Time	Figure 1, C_L = 15,000pF		40	60	ns
t_{D1}	Delay Time	Figure 1, C_L = 15,000pF		30	60	ns
t_{D2}	Delay Time	Figure 1, C_L = 15,000pF		33	60	ns
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V		0.4	1.5	mA
		V_{IN} = 0V		0.08	0.15	mA

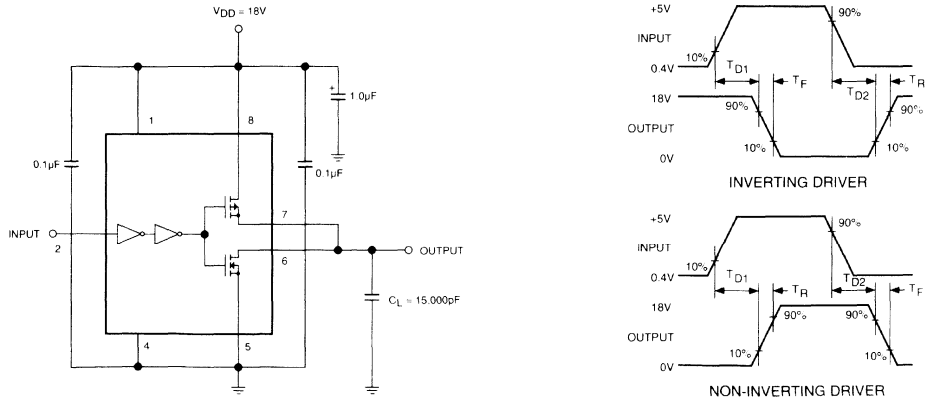


Figure 1. MIC4610/4611 Switching time test circuit.

Electrical Characteristics, continued

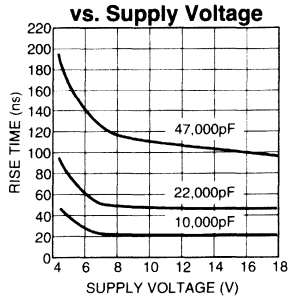
Specifications measured **over operating temperature range** with $4.5V \leq V_{DD} \leq 18V$, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1 High Input Voltage		2.4		V_{DD} + 0.3	V
V_{IL}	Logic 0 Low Input Voltage		–5		0.8	V
I_{IN}	Input Current	$0V \leq V_{IN} \leq V_{DD}$	–10		10	µA
Output						
V_{OH}	High Output Voltage		V_{DD} – 0.025			V
V_{OL}	Low Output Voltage				0.025	V
R_O	Output Resistance, Pull-Up	I_{OUT} = 10mA, V_{DD} = 18V		1.5	2.2	Ω
R_O	Output Resistance, Pull-Down	I_{OUT} = 10mA, V_{DD} = 18V		1.4	2.2	Ω
Switching Time (Note 1)						
t_R	Rise Time	Figure 1, C_L = 15,000pF		60	100	ns
t_F	Fall Time	Figure 1, C_L = 15,000pF		60	100	ns
t_{D1}	Delay Time	Figure 1, C_L = 15,000pF		45	80	ns
t_{D2}	Delay Time	Figure 1, C_L=15,000pF		45	80	ns
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V		0.6	3	mA
		V_{IN} = 0V		0.1	0.2	mA

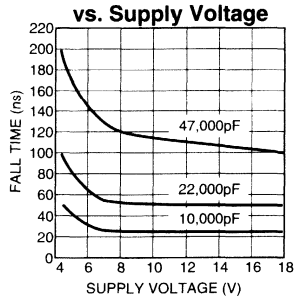
8

Typical Performance Characteristics

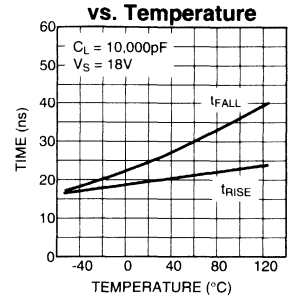
Rise Time vs. Supply Voltage



Fall Time vs. Supply Voltage

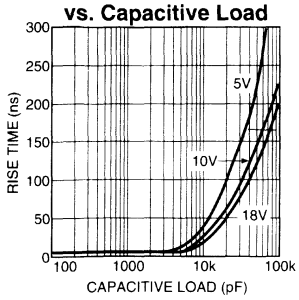


Rise and Fall Times vs. Temperature

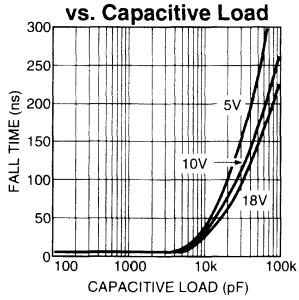


Typical Performance Characteristics, continued

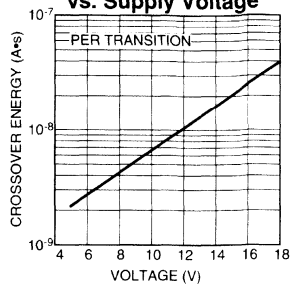
Rise Time vs. Capacitive Load



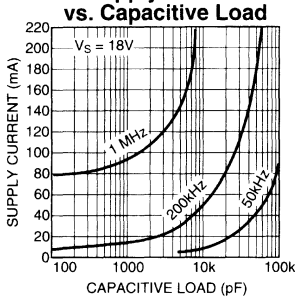
Fall Time vs. Capacitive Load



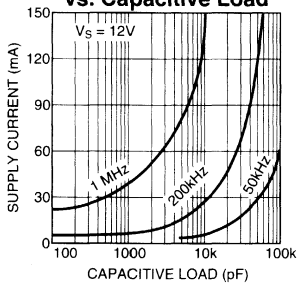
Crossover Energy vs. Supply Voltage



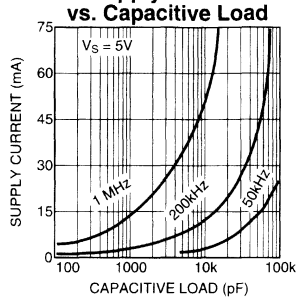
Supply Current vs. Capacitive Load



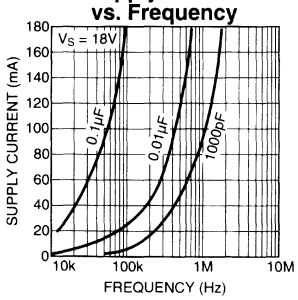
Supply Current vs. Capacitive Load



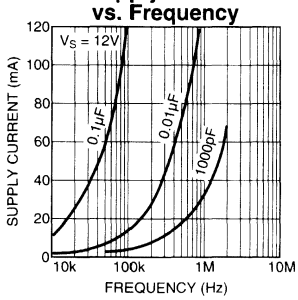
Supply Current vs. Capacitive Load



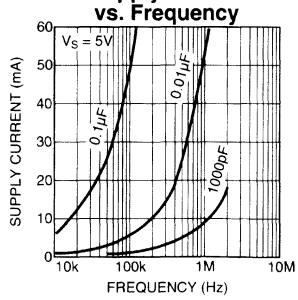
Supply Current vs. Frequency



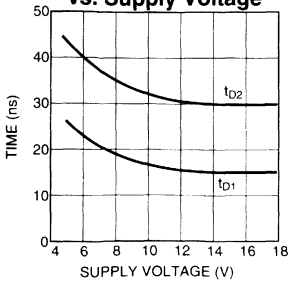
Supply Current vs. Frequency



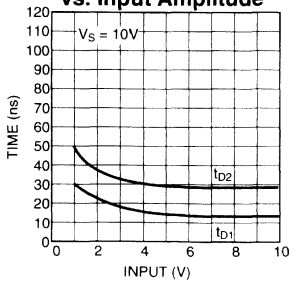
Supply Current vs. Frequency



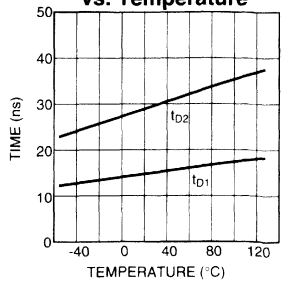
Propagation Delay vs. Supply Voltage



Propagation Delay vs. Input Amplitude

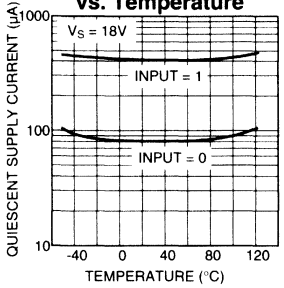


Propagation Delay vs. Temperature

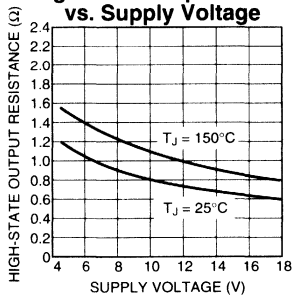


Typical Performance Characteristics, continued

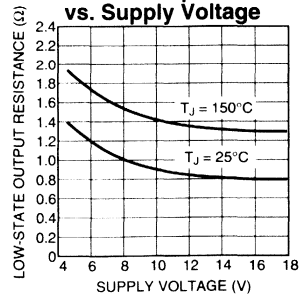
Quiescent Supply Current vs. Temperature



High-State Output Resist. vs. Supply Voltage



Low-State Output Resist. vs. Supply Voltage



8

SECTION 9: COMPUTER PERIPHERALS

MIC2557

PCMCIA Card Socket V_{PP} Switching Matrix

General Description

The MIC2557 switches the four voltages required by PCMCIA (Personal Computer Memory Card International Association) card V_{PP} Pins. The MIC2557 provides selectable 0V, 3.3V, 5.0V, or 12.0V (±5%) from the system power supply to V_{PP1} or V_{PP2}. Output voltage is selected by two digital inputs. Output current ranges up to 120mA. Four control states, V_{PP}, V_{CC}, high impedance, and active logic low are available. An auxiliary control input determines whether the high impedance (open) state or low logic state is asserted.

In either quiescent mode or full operation, the device draws very little current, typically less than 1µA.

The MIC2557 is available in an 8-pin SOIC and an 8-pin plastic DIP.

Applications

- PCMCIA V_{PP} Pin Voltage Switch
- Power Supply Management
- Power Analog Switch

Features

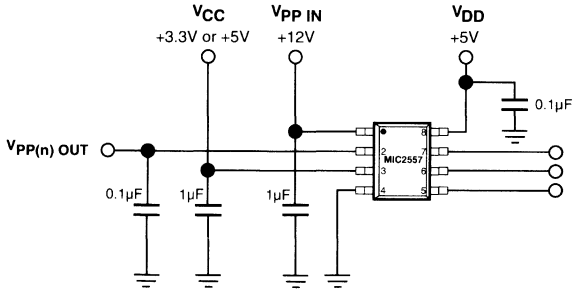
- Complete PCMCIA V_{PP} Switch Matrix in a Single IC
- No External Components Required
- Digital Selection of 0V, V_{CC}, V_{PP}, or High Impedance Output
- No $V_{PP\ OUT}$ Overshoot or Switching Transients
- Break-Before-Make Switching
- Low Power Consumption
- 120mA V_{PP} (12V) Output Current
- Optional Active Source Clamp for Zero Volt Condition
- 3.3V or 5V Supply Operation
- 8-Pin SOIC Package

Ordering Information

Part Number	Temperature Range	Package
MIC2557BM	–40°C to +85°C	8-pin SOIC
MIC2557BM T&R	–40°C to +85°C	8-SOIC Tape & Reel*
MIC2557BN	–40°C to +85°C	8-pin Plastic DIP

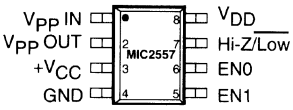
* 2,500 Parts per reel.

Typical Application



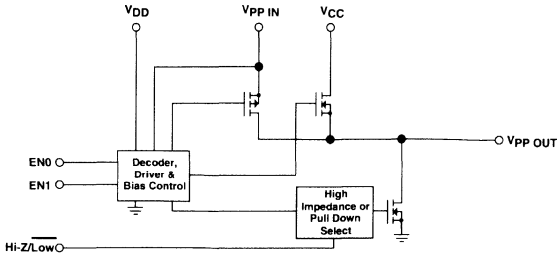
EN1	EN0	Hi-Z/Low	$V_{PP\ OUT}$
0	0	0	0V, (Sink current)
0	0	1	Hi-Z (No Connect)
0	1	x	V_{CC} (3.3V or 5.0V)
1	0	x	V_{PP}
1	1	x	Hi-Z (No Connect)

Pin Configuration



S.O. and DIP Packages

Simplified Block Diagram

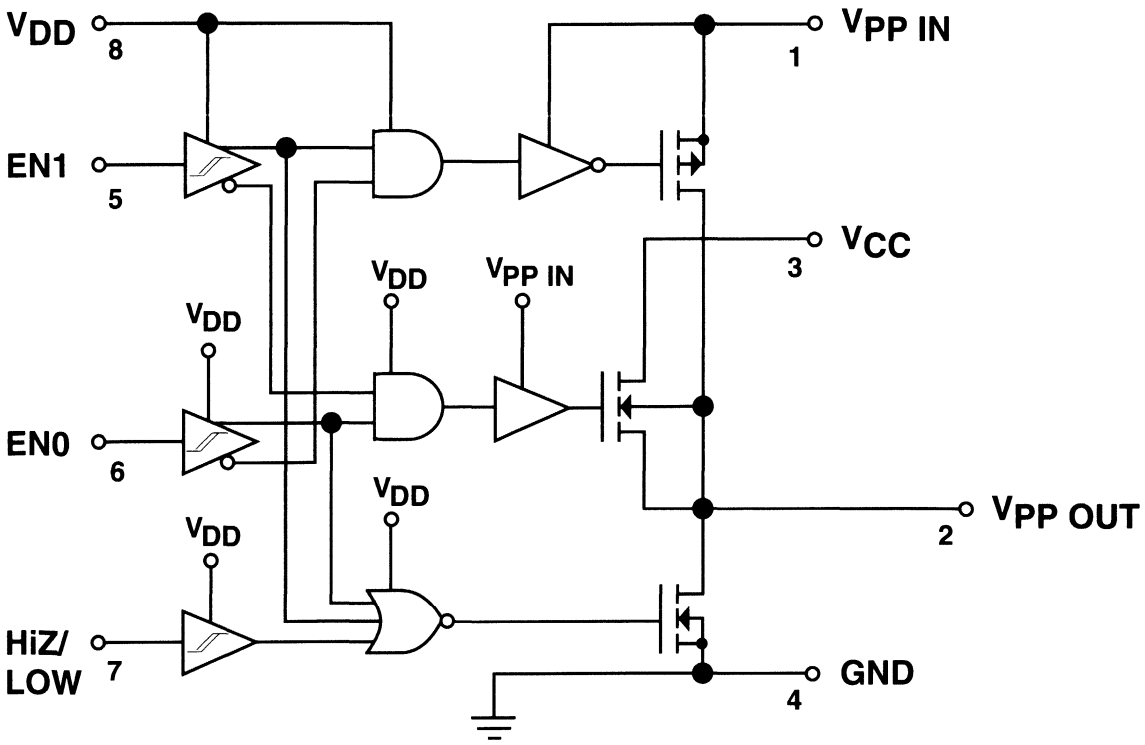


For a dual PCMCIA Card Socket V_{PP} Switching Matrix, see the MIC2558.
For a V_{PP} and V_{CC} Switching Matrix, see the MIC2560.

Absolute Maximum Ratings (Notes 1 and 2)

Power Dissipation, $T_{AMBIENT} \leq 25°C$	
PDIP	1W
SOIC	800 mW
Derating Factors (To Ambient)	
PDIP	8 mW/°C
SOIC	4 mW/°C
Storage Temperature	–65°C to +150°C
Operating Temperature (Die)	125°C
Operating Temperature (Ambient)	–40°C to +85°C
Lead Temperature (10 sec)	300°C
Supply Voltage, $V_{PP\ IN}$	15V
V_{CC}	7.5V
V_{DD}	7.5V
Logic Input Voltages	–5V to V_{DD}
Output Current	
$V_{PP\ OUT} = 12V$	600mA
$V_{PP\ OUT} = V_{CC}$	250mA

Logic Block Diagram



Electrical Characteristics: (Over operating temperature range with $V_{DD} = V_{CC} = 5V$, $V_{PP\ IN} = 12$ V unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
INPUT						
V_{IH}	Logic 1 Input Voltage	V_{DD} = 3.3V or 5.0V	2.2			V
V_{IL}	Logic 0 Input Voltage	V_{DD} = 3.3V or 5.0V			0.8	V
V_{IN} (Max)	Input Voltage Range		–5		V_{DD}	V
I_{IN}	Input Current	$0\ V < V_{IN} < V_{DD}$			±1	µA
OUTPUT						
V_{OL}	Clamp Low Output Voltage	EN0 = EN1 = HiZ = 0, I_{SINK} = 1.6mA			0.4	V
I_{OUT}, Hi-Z	High Impedance Output Leakage Current	EN0 = EN1 = 0, HiZ = 1 $0 \le V_{PP\ OUT} \le 12V$		1	10	µA
R_{OC}	Clamp Low Output Resistance	Resistance to Ground. I_{SINK} = 2mA EN0 = EN1 =0,HiZ=0		130	250	Ω
R_O	Switch Resistance, $V_{PP\ OUT} = V_{CC}$	$I_{PP\ OUT}$ = –10 mA (Sourcing)		2.5	5	Ω
R_O	Switch Resistance, $V_{PP\ OUT} = V_{PP\ IN}$	$I_{PP\ OUT}$ = –100 mA (Sourcing)		0.5	1	Ω
SWITCHING TIME (See Figure 1)						
t_1	Delay + Rise Time	$V_{PP\ OUT}$ = 0V to 5V (Notes 3, 5)		15	50	µs
t_2	Delay + Rise Time	$V_{PP\ OUT}$ = 5V to 12V (Notes 3, 5)		12	50	µs
t_3	Delay + Fall Time	$V_{PP\ OUT}$ = 12V to 5V (Notes 3, 5)		25	75	µs
t_4	Delay + Fall Time	$V_{PP\ OUT}$ = 5V to 0V (Notes 3, 5)		45	100	µs
t_5	Output Turn-On Delay	$V_{PP\ OUT}$ = Hi-Z to 5V (Notes 4, 5)		10	50	µs
t_6	Output Turn-Off Delay	$V_{PP\ OUT}$ = 5V to Hi-Z (Notes 4, 5)		75	200	ns
POWER SUPPLY						
I_{DD}	V_{DD} Supply Current			–	1	µA
I_{CC}	V_{CC} Supply Current	$I_{PP\ OUT}$ = 0		–	1	µA
I_{PP}	I_{PP} Supply Current	$V_{PP\ OUT}$ = 0 V or V_{PP} . I_{PPOUT} = 0.		–	10	µA
		$V_{PP\ OUT1} = V_{PPOUT2} = V_{CC}$		10	40	µA

Electrical Characteristics, (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
POWER SUPPLY, continued						
V_{CC}	Operating Input Voltage				6	V
V_{DD}	Operating Input Voltage		2.8		6	V
$V_{PP\ IN}$	Operating Input Voltage		8.0		14.5	V

NOTE 1: Functional operation above the absolute maximum stress ratings is not implied.
NOTE 2: Static-sensitive device. Store only in conductive containers. Handling personnel and equipment should be grounded to prevent damage from static discharge.
NOTE 3: With R_L = 2.9kΩ and $C_{(...)}$ = 0.1µF on $V_{(...)}$.
NOTE 4: R_L = 2.9kΩ. R_L is connected to V_{CC} during t_5 , and is connected to ground during t_6.
NOTE 5: Rise and fall times are measured to 90% of the difference between initial and final values.

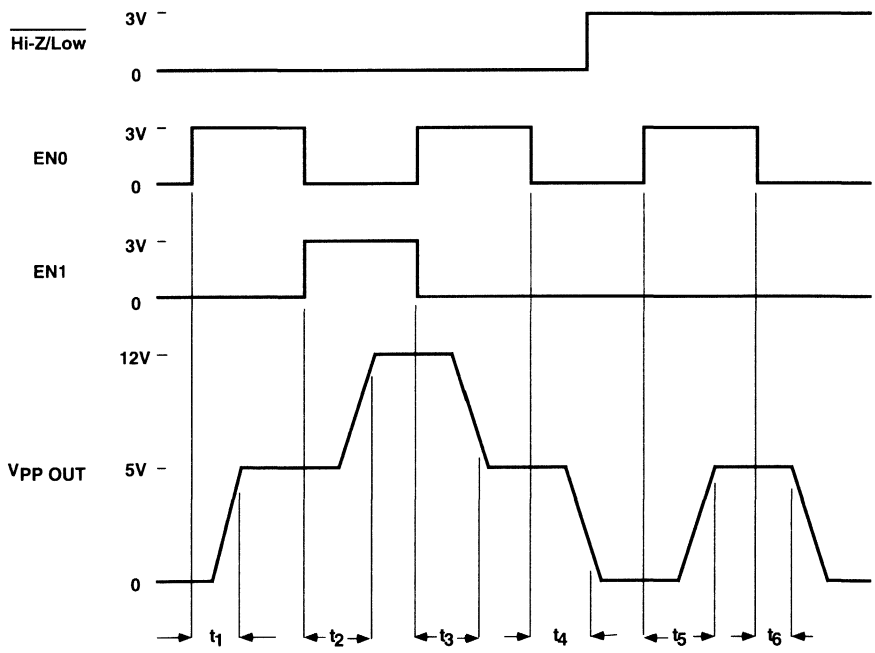


Figure 1. Timing Diagram

Applications Information

PCMCIA V_{PP} control is easily accomplished using the MIC2557 voltage selector/switch IC. Two control bits determine output voltage and standby/operate mode condition. Output voltages of 0V (defined as less than 0.4V), V_{CC} (3.3V or 5V), V_{PP}, or a high impedance state, are available. When either the high impedance or low voltage conditions are selected, the device switches into "sleep" mode, and draws only nanoamperes of leakage current.

The MIC2557 is a low-resistance power MOSFET switching matrix that operates from the computer system main power supply. Device power is obtained from V_{DD}, which may be either 3.3V or 5V, and FET drive is obtained from $V_{PP\ IN}$ (usually +12V). Internal break-before-make switches determine the output voltage and device mode.

Supply Bypassing

For best results, bypass V_{CC} and $V_{PP\ IN}$ at their inputs with 1µF capacitors. $V_{PP\ OUT}$ should have a 0.01µF to 0.1µF capacitor for noise reduction and electrostatic discharge (ESD) damage prevention. Larger values of output capacitor will create large current spikes during transitions, requiring larger bypass capacitors on the V_{CC} and $V_{PP\ IN}$ pins.

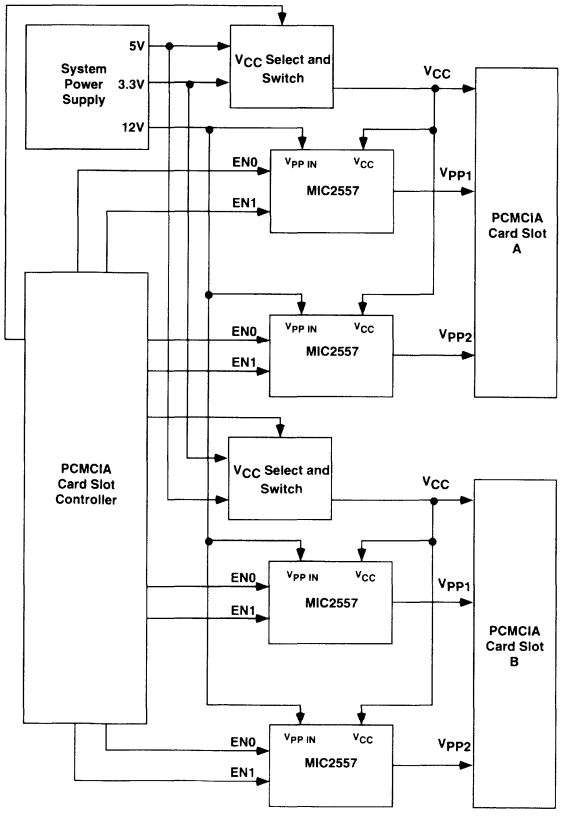


Figure 2. MIC2557 Typical two slot PCMCIA application with dual V_{cc} (5.0V or 3.3V).

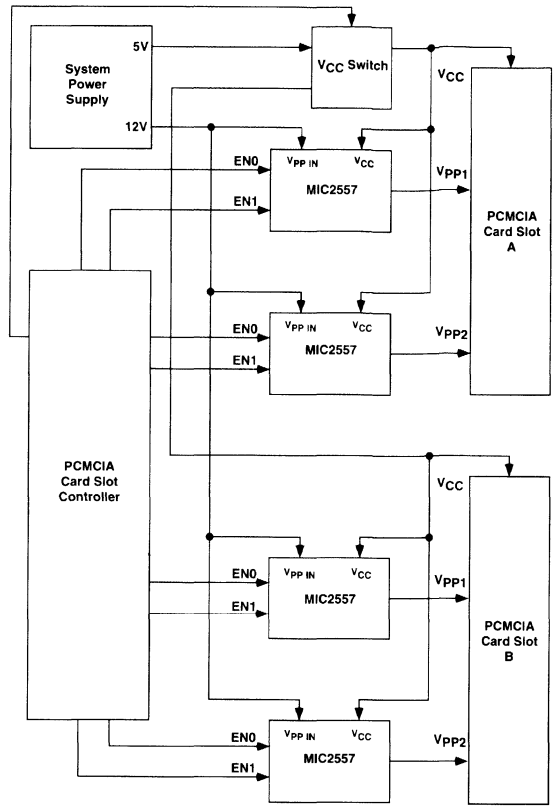


Figure 3. MIC2557 Typical two slot PCMCIA application with single 5.0V V_{CC}.

PCMCIA Implementation

The Personal Computer Memory Card International Association (PCMCIA) specification requires two V_{PP} supply pins per PCMCIA slot. V_{PP} is primarily used for programming Flash (EEPROM) memory cards. The two V_{PP} supply pins may be programmed to different voltages. Fully implementing PCMCIA specifications requires two MIC2557, and a controller. Figure 2 shows this full configuration, supporting both 5.0V and 3.3V V_{CC} operation. Figure 3 is a simplified design with fixed V_{CC} = 5V. Palmtop computers, where size and battery life are tantamount, can sometimes use a compromise implementation, with V_{PP1} tied to V_{PP2} (see Figure 4).

When a memory card is initially inserted, it should receive V_{CC}, usually 5.0V ±5%. The card sends a handshaking data stream to the controller, which then determines whether or not this card requires V_{PP} and if the card is designed for 5.0V or 3.3V V_{CC}. If the card uses 3.3V V_{CC}, the controller commands this change, which is reflected on the V_{CC} pins of both the PCMCIA slot and the MIC2557.

During Flash memory programming, the PCMCIA controller outputs a (1,0) to the MIC2557, which connects $V_{PP\ IN}$ to

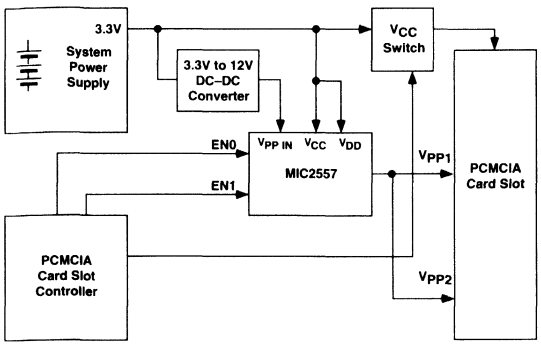


Figure 4. MIC2557 Palmtop application. Note that the V_{PP1} and V_{PP2} pins are combined. Although this does not fully satisfy PCMCIA specifications, it simplifies the circuitry and is acceptable in certain applications.

$V_{PP\ OUT}$. The low ON resistance of the MIC2557 switch requires only a small bypass capacitor on $V_{PP\ OUT}$, with the main filtering action performed by a large filter capacitor on $V_{PP\ IN}$. The $V_{PP\ OUT}$ transition from V_{CC} to 12.0V typically takes 25µS. After programming is completed, the controller outputs a (0,1) to the MIC2557, which then reduces $V_{PP\ OUT}$ to the V_{CC} level. Break-before-make switching action reduces switching transients and lowers maximum current spikes through the switch from the output capacitor.

If no card is inserted, or the system is in sleep mode, the controller outputs either a (0,0) or a (1,1) to the MIC2557. Either input places the switch into its shutdown mode, where only a small leakage current flows.

The HiZ/Low input controls the optional logic low output clamp. With HiZ/Low in the high state and ENO = EN1 = 0, $V_{PP\ OUT}$ enters a high impedance (open) state. With HiZ/Low in the low state and EN0 = EN1 = 0, $V_{PP\ OUT}$ is clamped to ground, providing a logic low signal. The clamp does not require DC bias current for operation.

MOSFET drive and bias voltage is derived from $V_{PP\ IN}$. Internal device control logic is powered from V_{DD}, which should be connected to the same supply voltage as the PCMCIA controller (normally either 3.3V or 5V).

Output Current

MIC2557 output switches are capable of far more current than usually needed in PCMCIA applications. PCMCIA V_{PP} output current is limited primarily by switch resistance voltage drop (**I x R**) and the requirement that $V_{PP\ OUT}$ cannot drop more than 5% below nominal. $V_{PP\ OUT}$ will survive output short circuits to ground if $V_{PP\ IN}$ and V_{CC} are current limited by the regulator that supplies these voltages.

9

MIC2558

PCMCIA Dual Card Socket V_{PP} Switching Matrix

General Description

The MIC2558 Dual V_{PP} Matrix switches the four voltages required by PCMCIA (Personal Computer Memory Card International Association) card V_{PP1} and V_{PP2} Pins. The MIC2558 provides selectable 0V, 3.3V, 5.0V, or 12.0V (±5%) from the system power supply to V_{PP1} and V_{PP2}. Output voltage is selected by two digital inputs per V_{PP} pin. Output current ranges up to 120mA. Four output states, V_{PP}, V_{CC}, high impedance, and active logic low are available, and V_{PP1} is independent of V_{PP2}. An auxiliary control input determines whether the high impedance (open) state or low logic state is asserted.

In standby mode or full operation, the device draws very little quiescent current, typically less than 1µA.

The MIC2558 is available in a 14-pin SOIC and a 14-pin plastic DIP.

Applications

- PCMCIA V_{PP} Pin Voltage Switch
- Power Supply Management

Features

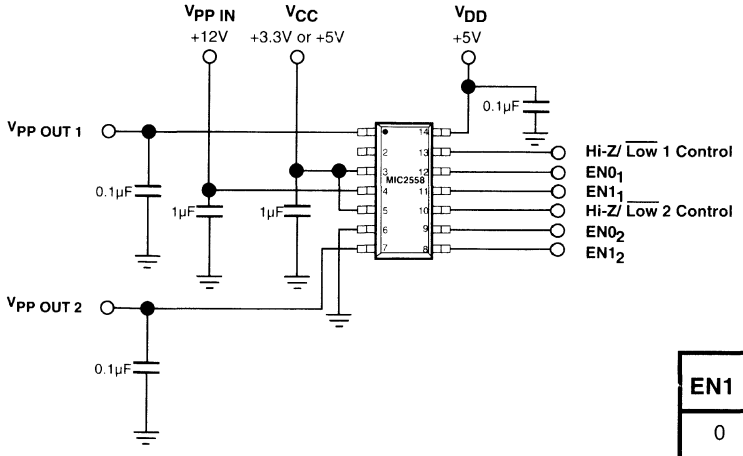
- Complete PCMCIA V_{PP} Switch Matrix in a Single IC
- Dual Matrix allows independent V_{PP1} and V_{PP2}
- Digital Selection of 0V, V_{CC}, V_{PP}, or High Impedance Output
- No V_{PPOUT} Overshoot or Switching Transients
- Break-Before-Make Switching
- Ultra Low Power Consumption
- 120mA V_{PP} (12V) Output Current
- Optional Active Source Clamp for Zero Volt Condition
- 3.3V or 5V Supply Operation
- 14-Pin SOIC Package

Ordering Information

Part Number	Temperature Range	Package
MIC2558BM	–40°C to +85°C	14-pin SOIC
MIC2558BM T&R	–40°C to +85°C	14-SO Tape & Reel*
MIC2558BN	–40°C to +85°C	14-pin Plastic DIP

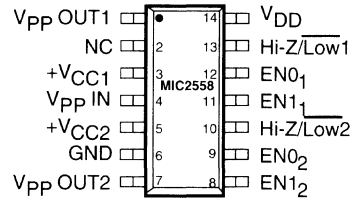
* 2,500 Parts per reel.

Typical Application



For a PCMCIA V_{PP} and V_{CC} Switching Matrix, see the MIC2560.

Pin Configuration



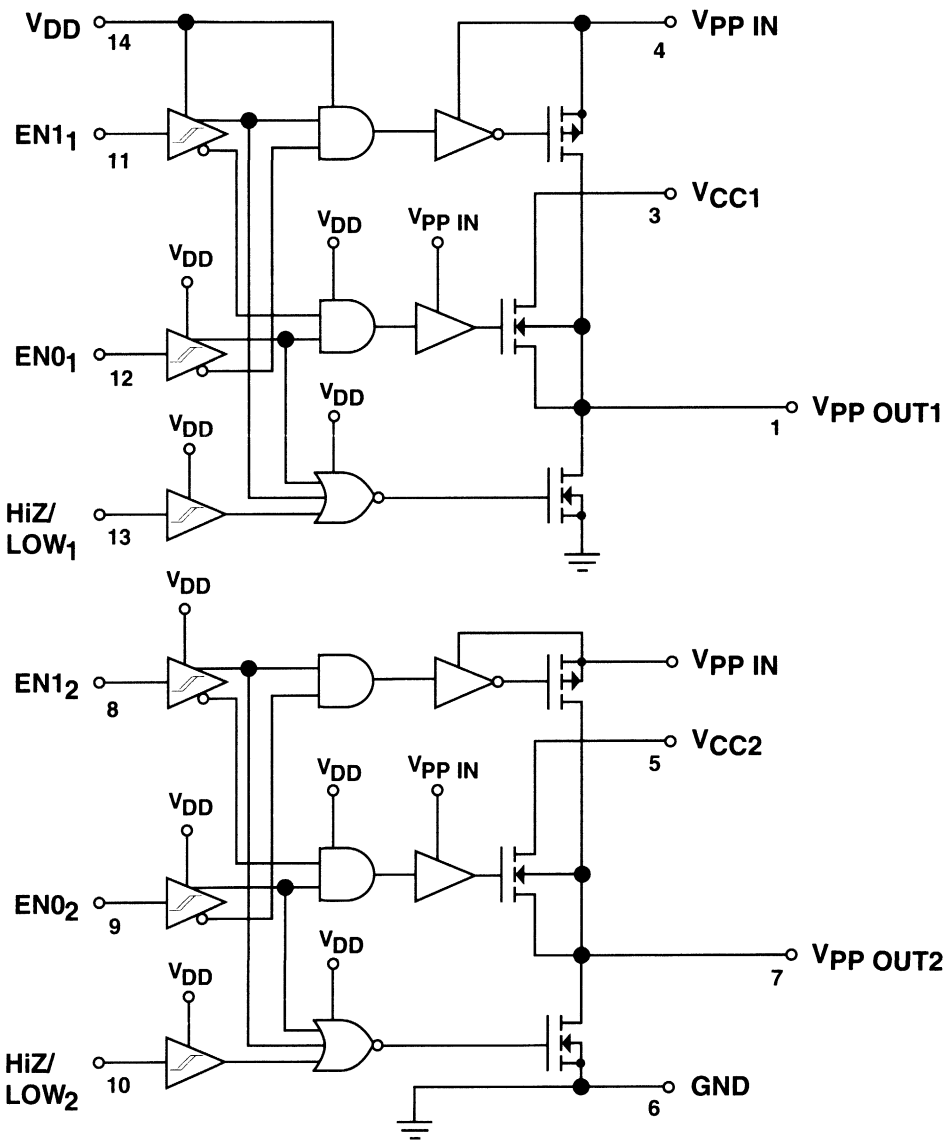
S.O. and DIP Packages

EN1	EN0	Hi-Z/Low	$V_{PP\ OUT}$
0	0	0	0V, (Sink current)
0	0	1	Hi-Z (No Connect)
0	1	x	V_{CC} (3.3V or 5.0V)
1	0	x	V_{PP}
1	1	x	Hi-Z (No Connect)

Absolute Maximum Ratings (Notes 1 and 2)

Power Dissipation, $T_{AMBIENT} \leq 25°C$	
PDIP	1W
SOIC	800 mW
Derating Factors (To Ambient)	
PDIP	8 mW/°C
SOIC	4 mW/°C
Storage Temperature	–65°C to +150°C
Operating Temperature (Die)	125°C
Operating Temperature (Ambient)	–40°C to +85°C
Lead Temperature (10 sec)	300°C
Supply Voltage, $V_{PP\ IN}$	15V
V_{CC}	7.5V
V_{DD}	7.5V
Logic Input Voltages	–5V to V_{DD}
Output Current (each Output)	
$V_{PP\ OUT} = 12V$	600mA
$V_{PP\ OUT} = V_{CC}$	250mA

Logic Block Diagram



9

Electrical Characteristics: (Over operating temperature range with $V_{DD} = V_{CC} = 5V$, $V_{PP\ IN} = 12$ V unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
INPUT						
V_{IH}	Logic 1 Input Voltage		2.2			V
V_{IL}	Logic 0 Input Voltage				0.8	V
V_{IN} (Max)	Input Voltage Range		–5		V_{DD}	V
I_{IN}	Input Current	$0\ V < V_{IN} < V_{DD}$			±1	µA
EACH OUTPUT						
V_{OL}	Clamp Low Output Voltage	EN0 = EN1 = HiZ = 0, I_{SINK} = 1.6mA			0.4	V
I_{OUT}, Hi-Z	High Impedance Output Leakage Current	EN0 = EN1 = 0, HiZ = 1. $0 \le V_{PP\ OUT} \le 12V$		1	10	µA
R_{OC}	Clamp Low Output Resistance	Resistance to Ground. I_{SINK} = 2mA EN0 = EN1 = 0, HiZ = 0.		130	250	Ω
R_O	Switch Resistance, $V_{PP\ OUT} = V_{CC}$	$I_{PP\ OUT}$ = –10 mA (Sourcing)		2.5	5	Ω
R_O	Switch Resistance, $V_{PP\ OUT} = V_{PP\ IN}$	$I_{PP\ OUT}$ = –100 mA (Sourcing)		0.5	1	Ω
SWITCHING TIME (See Figure 1)						
t_1	Delay + Rise Time	$V_{PP\ OUT}$ = 0V to 5V (Notes 3, 5)		15	50	µs
t_2	Delay + Rise Time	$V_{PP\ OUT}$ = 5V to 12V (Notes 3, 5)		12	50	µs
t_3	Delay + Fall Time	$V_{PP\ OUT}$ = 12V to 5V (Notes 3, 5)		25	75	µs
t_4	Delay + Fall Time	$V_{PP\ OUT}$ = 5V to 0V (Notes 3, 5)		45	100	µs
t_5	Output Turn-On Delay	$V_{PP\ OUT}$ = Hi-Z to 5V (Notes 4, 5)		10	50	µs
t_6	Output Turn-Off Delay	$V_{PP\ OUT}$ = 5V to Hi-Z (Notes 4, 5)		75	200	ns
POWER SUPPLY						
I_{DD}	V_{DD} Supply Current			–	1	µA
I_{CC}	V_{CC} Supply Current	$I_{PP\ OUT}$ = 0		–	1	µA
I_{PP}	I_{PP} Supply Current	$V_{PP\ OUT1} = V_{PPOUT2}$ = 0 V or V_{PP} I_{PPOUT} = 0.		–	10	µA
		$V_{PP\ OUT1} = V_{PPOUT2} = V_{CC}$		20	80	µA

Electrical Characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
POWER SUPPLY, continued						
V_{CC}	Operating Input Voltage				6	V
V_{DD}	Operating Input Voltage		2.8		6	V
$V_{PP\ IN}$	Operating Input Voltage		8.0		14.5	V

NOTE 1: Functional operation above the absolute maximum stress ratings is not implied.
NOTE 2: Static-sensitive device. Store only in conductive containers. Handling personnel and equipment should be grounded to prevent damage from static discharge.
NOTE 3: With $R_L = 2.9k\Omega$ and $C_{OUT} = 0.1\mu F$ on $V_{PP\ OUT}$.
NOTE 4: $R_L = 2.9k\Omega$. R_L is connected to V_{CC} during t_5, and is connected to ground during t_6.
NOTE 5: Rise and fall times are measured to 90% of the difference of initial and final values.

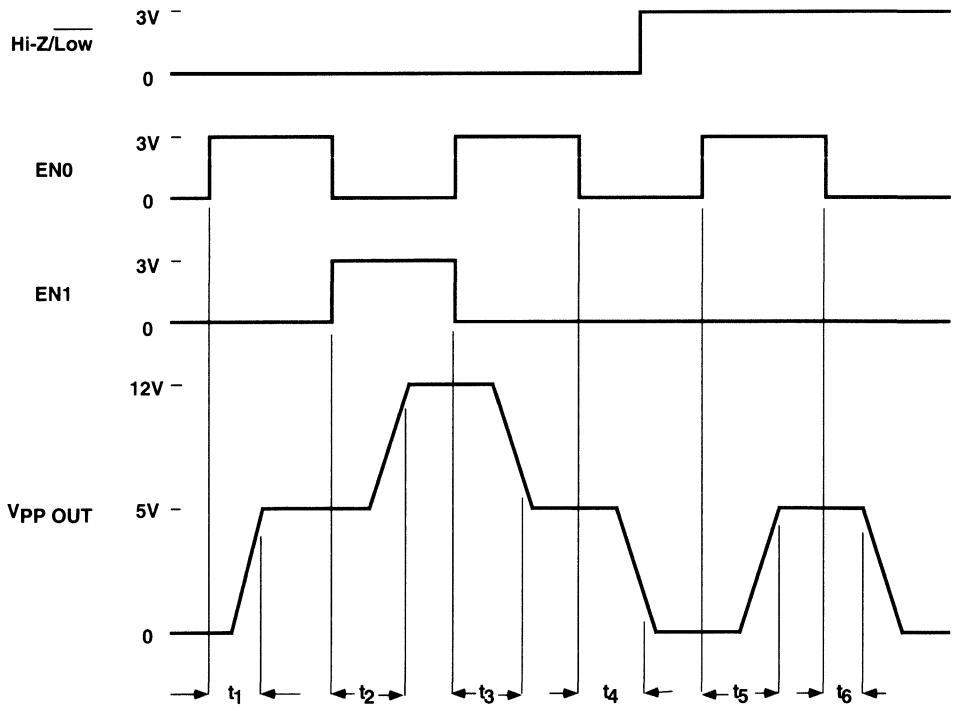


Figure 1. Timing Diagram.

Applications Information

PCMCIA V_{PP_1} and V_{PP_2} control is easily accomplished using the MIC2558 voltage selector/switch IC. Two control bits per $V_{PP\ OUT}$ pin determine output voltage and standby/operate mode condition. Output voltages of 0V (defined as less than 0.4V), V_{CC} (3.3V or 5V), V_{PP}, or a high impedance state, are available. When either the high impedance or low voltage conditions are selected, the device switches into "sleep" mode and draws only nanoamperes of leakage current.

The MIC2558 is a dual low-resistance power MOSFET switching matrix that operates from the computer system main power supply. Device power is obtained from V_{DD}, which may be either 3.3V or 5V, and FET drive is obtained from $V_{PP\ IN}$ (usually +12V). Internal break-before-make switches determine the output voltage and device mode. V_{PP1} and V_{PP2} are completely indepenent from each other.

Supply Bypassing

For best results, bypass V_{CC} and $V_{PP\ IN}$ inputs with 1µF capacitors. Both $V_{PP\ OUT}$ pins should have a 0.01µF to 0.1µF capacitor for noise reduction and electrostatic discharge (ESD) damage prevention. Larger values of output capacitor will create large current spikes during transitions, requiring larger bypass capacitors on the V_{CC} and $V_{PP\ IN}$ pins.

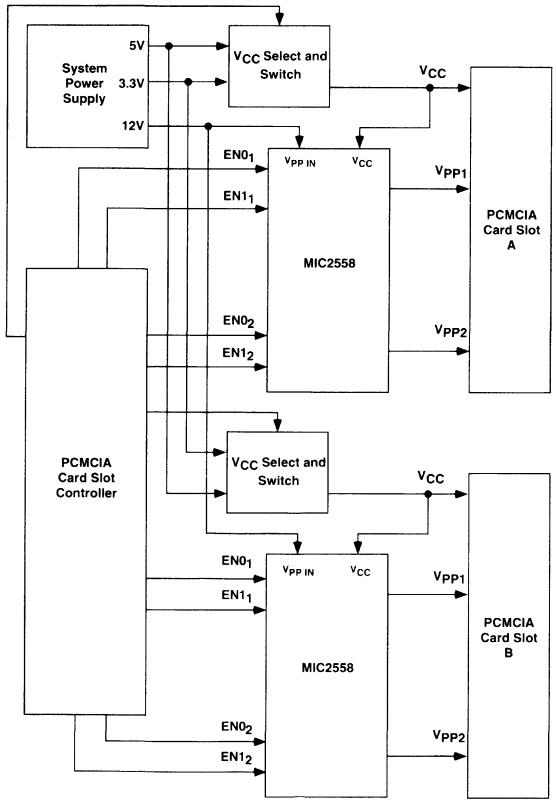


Figure 2. MIC2558 Typical two slot PCMCIA application with dual V_{CC} (5.0V or 3.3V).

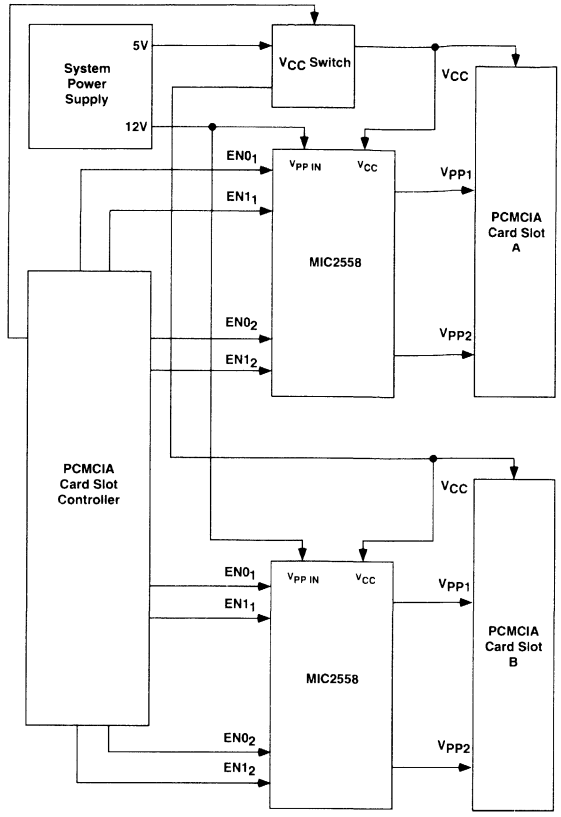


Figure 3. MIC2558 Typical two slot PCMCIA application with single 5.0V V_{CC}.

PCMCIA Implementation

The Personal Computer Memory Card International Association (PCMCIA) specification requires two V_{PP} supply pins per PCMCIA slot. V_{PP} is primarily used for programming Flash (EEPROM) memory cards. The two V_{PP} supply pins may be programmed to different voltages. Fully implementing PCMCIA specifications requires a MIC2558 and a controller. Figure 2 shows this full configuration, supporting both 5.0V and 3.3V V_{CC} operation. Figure 3 is a simplified design with fixed V_{CC} = 5V.

When a memory card is initially inserted, it should receive V_{CC} — usually 5.0V ±5%. The card sends a handshaking data stream to the controller, which then determines whether or not this card requires V_{PP} and if the card is designed for 5.0V or 3.3V V_{CC}. If the card uses 3.3V V_{CC}, the controller commands this change, which is reflected on the V_{CC} pins of both the PCMCIA slot and the MIC2558.

During Flash memory programming, the PCMCIA controller outputs a (1,0) to one or both halves of the MIC2558, which connects $V_{PP\ IN}$ to $V_{PP\ OUT1}$ and/or $V_{PP\ OUT2}$. The low ON resistance of the MIC2558 switch requires only a small bypass capacitor on the $V_{PP\ OUT}$ pins, with the main filtering

action performed by a large filter capacitor on $V_{PP\ IN}$. The $V_{PP\ OUT}$ transition from V_{CC} to 12.0V typically takes 25µS. After programming is completed, the controller outputs a (0,1) to the MIC2558, which then reduces $V_{PP\ OUT}$ to the V_{CC} level. Break-before-make switching action reduces switching transients and lowers maximum current spikes through the switch from the output capacitor.

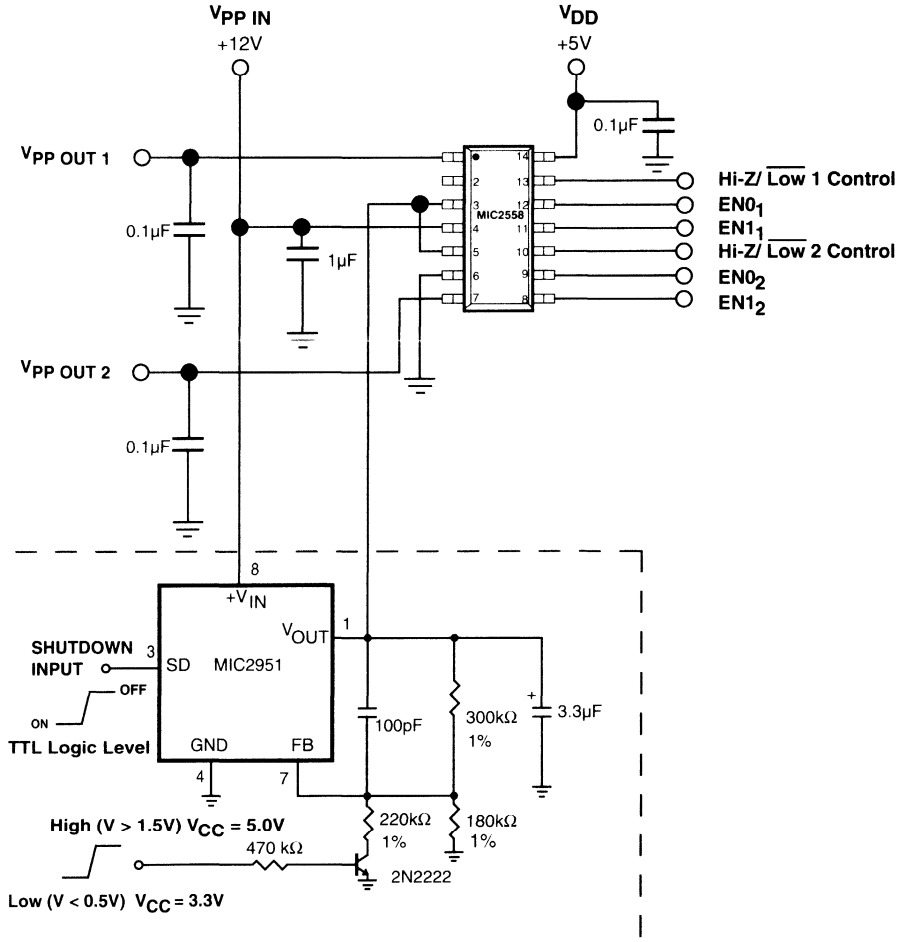
If no card is inserted, or the system is in sleep mode, the controller outputs either a (0,0) or a (1,1) to the MIC2558. Either input places the switch into shutdown mode, where current consumption drops even further.

The HiZ/Low input controls the optional logic low output clamp. With HiZ/Low in the high state and EN0 = EN1 = 0, $V_{PP\ OUT}$ enters a high impedance (open) state. With HiZ/Low in the low state and EN0 = EN1 = 0, $V_{PP\ OUT}$ is clamped to ground, providing a logic low signal. The clamp does not require any DC bias current for operation.

MOSFET drive and bias voltage is derived from $V_{PP\ IN}$. Internal device control logic is powered from V_{DD}, which should be connected to the same supply voltage as the PCMCIA controller (normally either 3.3V or 5V).

Output Current

MIC2558 output switches are capable of far more current than usually needed in PCMCIA applications. PCMCIA V_{PP} output current is limited primarily by switch resistance voltage drop (**I** x **R**) and the requirement that $V_{PP\ OUT}$ cannot drop more than 5% below nominal. $V_{PP\ OUT}$ will survive output short circuits to ground if $V_{PP\ IN}$ or V_{CC} are current limited by the regulator that supplies these voltages.



V_{CC} Switching and Control Block

Figure 3. Full PCMCIA Implementation of V_{PP} and V_{CC} switching using MIC2558 and MIC2951 voltage regulator.

MIC2560

PCMCIA Card Socket V_{CC} & V_{PP} Switching Matrix

Preliminary Information–Production Q2 '94

General Description

The MIC2560 V_{CC} & V_{PP} Matrix controls PCMCIA (Personal Computer Memory Card International Association) memory card power supply pins, both V_{CC} and V_{PP}. The MIC2560 switches voltages from the system power supply to V_{CC} and V_{PP}. The MIC2560 switches between the three V_{CC} voltages (OFF, 3.3V and 5.0V) and the V_{PP} voltages (OFF, 0V, 3.3V, 5V, or 12.0V) required by PCMCIA cards. Output voltage is selected by two digital inputs for each output and output current ranges up to 1A for V_{CC} and 200mA for V_{PP}.

The MIC2560 provides power management capability under the control of the PC Card controller and features over-current and thermal protection of the power outputs, zero current "sleep" mode, suspend mode, low power dynamic mode, and ON/OFF control of the PCMCIA socket power.

The MIC2560 is designed for efficient operation. In standby ("sleep") mode the device draws very little quiescent current, typically 0.01μA. The device and PCMCIA port is protected by current limiting and over-temperature shutdown. Full cross-conduction lockout protects the system power supply.

Ordering Information

Part Number	Temperature Range	Package
MIC2560-0BWM	–40°C to +70°C	16-pin Wide SOIC
MIC2560-0BN	–40°C to +70°C	16-pin Plastic DIP
MIC2560-1BWM	–40°C to +70°C	16-pin Wide SOIC

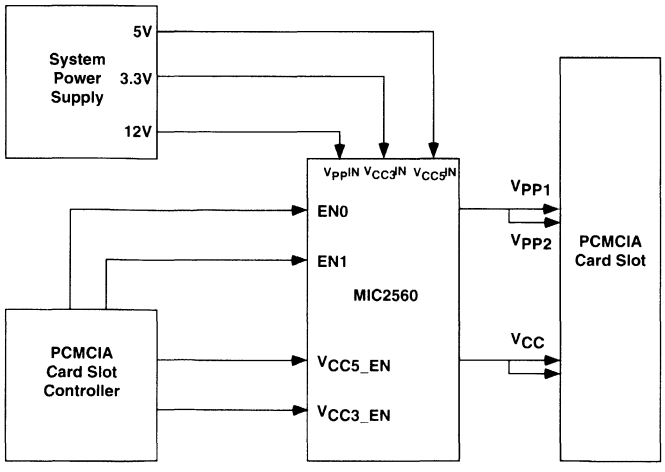
Applications

- PCMCIA Power Supply Pin Voltage Switch
- Font Cards for Printers and Scanners
- Data Collection Systems
- Machine Control Data Input Systems
- Wireless Communications
- Bar Code Data Collection Systems
- Instrumentation Configuration/Datalogging
- Docking Stations (portable and desktop)
- Power Supply Management
- Power Analog Switching

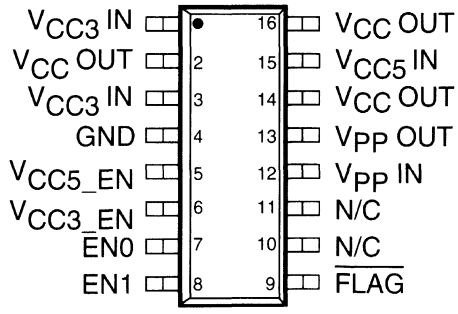
Features

- Complete PCMCIA V_{CC} and V_{PP} Switch Matrix in a Single IC
- No External Components Required
- Logic Compatible with Industry Standard PCMCIA Controllers
- No Voltage Overshoot or Switching Transients
- Break-Before-Make Switching
- Output Current Limit and Over-Temperature Shutdown
- Digital Flag for Error Condition Indication
- Ultra Low Power Consumption
- Digital Selection of V_{CC} and V_{PP} Voltages
- Over 1A V_{CC} Output Current
- 200mA V_{PP} (12V) Output Current
- Options for Direct Compatibility With Industry Standard PCMCIA Controllers
- 16-Pin SOIC Package

Typical Application



Pin Configuration



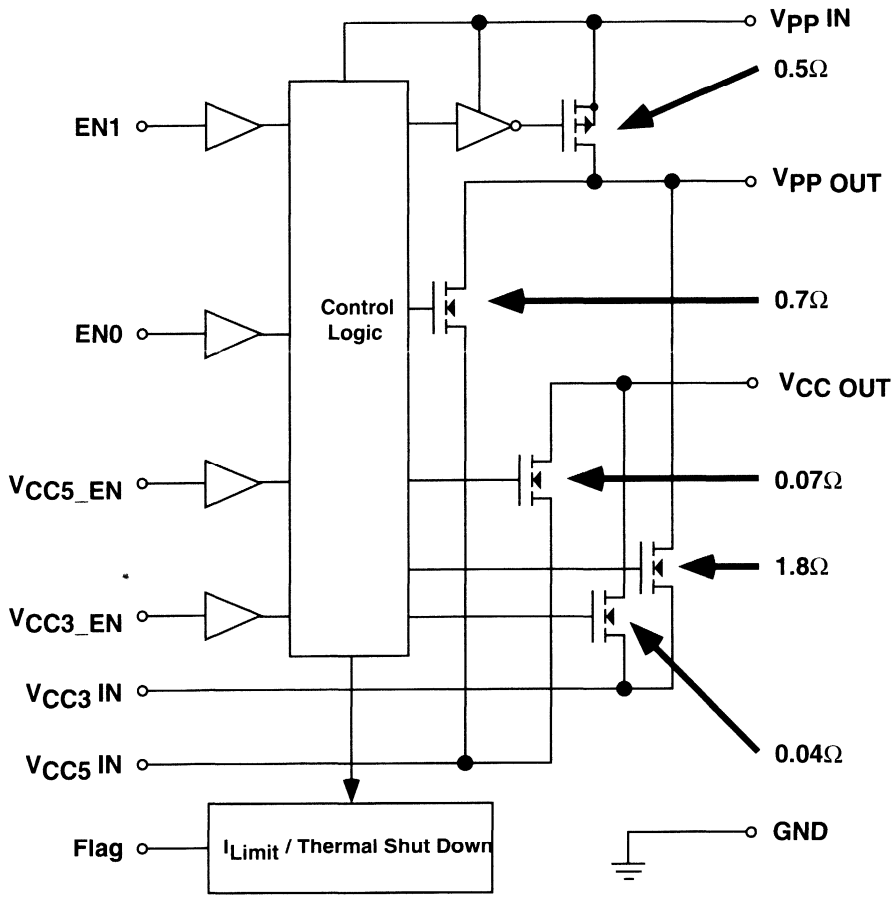
S.O. and DIP Packages

Note: both V_{CC3} IN pins must be connected. All three V_{CC} OUT pins must be connected.

Absolute Maximum Ratings (Notes 1 and 2)

Power Dissipation, $T_{AMBIENT} \leq 25°C$	*Internally Limited*
PDIP	1W
SOIC	800 mW
Derating Factors (To Ambient)	
PDIP	8 mW/°C
SOIC	4 mW/°C
Storage Temperature	–65°C to +150°C
Operating Temperature (Die)	125°C
Operating Temperature (Ambient)	–40°C to +70°C
Lead Temperature (10 sec)	300°C
Supply Voltage, $V_{PP\ IN}$	15V
V_{CC3} IN	7.5V
V_{CC5} IN	7.5V
Logic Input Voltages	–0.3V to +15V
Output Current (each Output)	
$V_{PP\ OUT}$	*>200mA, Internally Limited*
$V_{CC\ OUT}$	*>1A, Internally Limited*
$V_{CC\ OUT}$, Suspend Mode	600mA

Logic Block Diagram



9

Electrical Characteristics: (Over operating temperature range with V_{CC3} IN = 3.3V, V_{CC5} IN = 5.0V, V_{PP} IN = 12V unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
INPUT						
V_{IH}	Logic 1 Input Voltage		2.2		15	V
V_{IL}	Logic 0 Input Voltage		–0.3		0.8	V
I_{IN}	Input Current	0 V < V_{IN} < 5.5V			±1	µA
V_{PP} OUTPUT						
$I_{PP\ OUT}$ Hi-Z	High Impedance Output Leakage Current	Shutdown Mode 0 ≤ $V_{PP\ OUT}$ ≤ 12V		1		µA
I_{PPSC}	Short Circuit Current Limit	$V_{PP\ OUT}$ = 0		0.2		A
R_O	Switch Resistance, $I_{PP\ OUT}$ = –10mA (Sourcing)	Select $V_{PP\ OUT}$ = 5V Select $V_{PP\ OUT}$ = 3.3V		0.7 1.8	1 3	Ω
R_O	Switch Resistance, $V_{PP\ OUT}$ = $V_{PP\ IN}$	$I_{PP\ OUT}$ = –100 mA (Sourcing)		0.55	1	Ω
V_{PP} SWITCHING TIME (See Figure 1)						
t_1	Output Turn-On Rise Time	$V_{PP\ OUT}$ = Hi-Z to 5V		50		µs
t_2	Output Turn-On Rise Time	$V_{PP\ OUT}$ = Hi-Z to 3.3V		40		µs
t_3	Output Turn-On Rise Time	$V_{PP\ OUT}$ = Hi-Z to 12V		300		µs
t_4	Output Rise Time	$V_{PP\ OUT}$ = 3.3V or 5V to 12V		300		µs
V_{CC} OUTPUT						
$I_{CC\ OUT}$ Hi-Z	High Impedance Output Leakage Current	V_{CC3_EN} = V_{CC5_EN} = 0 (or High) 0 ≤ $V_{CC\ OUT}$ ≤ 5V		1		µA
I_{CCSC}	Short Circuit Current Limit	$V_{CC\ OUT}$ = 0		2		A
R_O	Switch Resistance, $V_{CC\ OUT}$ = 5.0V	$I_{CC\ OUT}$ = –1000 mA (Sourcing)		70	100	mΩ
R_O	Switch Resistance, $V_{CC\ OUT}$ = 3.3V	$I_{CC\ OUT}$ = –1000 mA (Sourcing)		40	66	mΩ

Electrical Characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{CC} SWITCHING TIME (See Figure 2)						
t_1	Delay + Rise Time	$V_{CC\ OUT}$ = 0V to 3.3V		600		µs
t_2	Delay + Rise Time	$V_{CC\ OUT}$ = 3.3V to 5.0V		500		µs
t_3	Delay + Fall Time	$V_{CC\ OUT}$ = 5.0V to 3.3V		300		µs
t_4	Rise Time	$V_{CC\ OUT}$ = Hi-Z to 5V		400		µs
POWER SUPPLY						
I_{CC5}	V_{CC5} IN Supply Current (5V)	$I_{CC\ OUT}$ = 0		0.011		µA
I_{CC3}	V_{CC3} IN Supply Current (3.3V)	$V_{CC\ OUT}$ = 5V or 3.3V, $I_{CC\ OUT}$ = 0 $V_{CC\ OUT}$ = Hi-Z (Sleep Mode)		30 0.01		µA
I_{PP} IN	V_{PP} IN Supply Current (12V)	Active $I_{PP\ OUT}$ = 0. $V_{PP\ OUT}$ = Hi-Z, 0 or V_{PP}		15 0.01		µA
V_{CC5} IN	Operating Input Voltage (5V)	V_{CC5} IN ≥ V_{CC3} IN	2.8	5.0	6	V
V_{CC3} IN	Operating Input Voltage (3.3V)	V_{CC3} IN ≤ V_{CC5} IN	2.8	3.3	6	V
$V_{PP\ IN}$	Operating Input Voltage (12V)		8.0	12.0	14.5	V
SUSPEND MODE (NOTE 6)						
I_{CC3}	Active Mode Current	$V_{PP\ IN}$ = 0V, V_{CC5} = V_{CC3} = 3.3V V_{CC3} = Enabled V_{PP} = Disabled (Hi-Z or 0V)		30		µA
R_{ON} V_{CC}	$V_{CC\ OUT}$ R_{ON}	$V_{PP\ IN}$ = 0V, V_{CC5} = V_{CC3} = 3.3V V_{CC3} = Enabled V_{PP} = Disabled (Hi-Z or 0V)		4.5		Ω

NOTE 1: Functional operation above the absolute maximum stress ratings is not implied.

NOTE 2: Static-sensitive device. Store only in conductive containers. Handling personnel and equipment should be grounded to prevent damage from static discharge.

NOTE 6: Suspend mode is a pseudo power-down mode the MIC2560 automatically allows when $V_{PP\ IN}$ = 0V, V_{PP} OUT is deselected, and V_{CC} OUT = 3.3V is selected. Under these conditions, the MIC2560 functions in a reduced capacity mode where V_{CC} output of 3.3V is allowed, but at lower current levels (higher switch ON resistance).

MIC2560-0 Control Logic Table

Pin 5 V_{CC5_EN}	Pin 6 V_{CC3_EN}	Pin 8 EN1	Pin 7 EN0	Pins 2 & 14 $V_{CC\ OUT}$	Pin 13 $V_{PP\ OUT}$
0	0	0	0	High Z	High Z
0	0	0	1	High Z	High Z
0	0	1	0	High Z	High Z
0	0	1	1	High Z	Clamped to Ground
0	1	0	0	3.3	High Z
0	1	0	1	3.3	3.3
0	1	1	0	3.3	12
0	1	1	1	3.3	Clamped to Ground
1	0	0	0	5	High Z
1	0	0	1	5	5
1	0	1	0	5	12
1	0	1	1	5	Clamped to Ground
1	1	0	0	3.3	High Z
1	1	0	1	3.3	3.3
1	1	1	0	3.3	5
1	1	1	1	3.3	Clamped to Ground

MIC2560-1 Logic (Compatible with Cirrus Logic CL-PD6710 & CL-PD6720 Controllers)

Pin 5 V_{CC5_EN}	Pin 6 V_{CC3_EN}	Pin 8 V_{PP_PGM}	Pin 7 V_{PP_VCC}	Pins 2 & 14 $V_{CC\ OUT}$	Pin 13 $V_{PP\ OUT}$
0	0	0	0	High Z	Clamped to Ground
0	0	0	1	High Z	High Z
0	0	1	0	High Z	High Z
0	0	1	1	High Z	High Z
0	1	0	0	5	Clamped to Ground
0	1	0	1	5	5
0	1	1	0	5	12
0	1	1	1	5	High Z
1	0	0	0	3.3	Clamped to Ground
1	0	0	1	3.3	3.3
1	0	1	0	3.3	12
1	0	1	1	3.3	High Z
1	1	0	0	High Z	Clamped to Ground
1	1	0	1	High Z	High Z
1	1	1	0	High Z	High Z
1	1	1	1	High Z	High Z

Note: other control logic patterns are available. Please contact Micrel for details.

Applications Information

PCMCIA V_{CC} and V_{PP} control is easily accomplished using the MIC2560 voltage selector/switch IC. Four control bits determine $V_{CC\ OUT}$ and $V_{PP\ OUT}$ voltage and standby/operate mode condition. $V_{PP\ OUT}$ output voltages of V_{CC} (3.3V or 5V), V_{PP}, or a high impedance state are available. When the V_{CC} high impedance condition is selected, the device switches into "sleep" mode and draws only nanoamperes of leakage current. An error flag falls low if the output is improper, because of overtemperature or overcurrent faults. Full protection from hot switching is provided which prevents feedback from the $V_{PP\ OUT}$ to the V_{CC} inputs (from 12V to 5V, for example) by locking out the low voltage switch until $V_{PP\ OUT}$ drops below V_{CC}. The V_{CC} output is similarly protected against 5V to 3.3V shoot through.

The MIC2560 is a low-resistance power MOSFET switching matrix that operates from the computer system main power supply. Device logic power is obtained from V_{CC3} and internal MOSFET drive is obtained from the V_{PP} IN pin (usually +12V) during normal operation. If +12V is not available, the MIC2560 automatically switches into "suspend" mode, where $V_{CC\ OUT}$ can be switched to 3.3V, but at higher switch resistance. Internal break-before-make switches determine the output voltage and device mode.

Supply Bypassing

External capacitors are not required for operation. The MIC2560 is a switch and has no stability problems. For best results however, bypass V_{CC3} IN, V_{CC5} IN, and V_{PP} IN inputs with filter capacitors to improve output ripple. As all internal device logic and voltage/current comparison functions are powered from the V_{CC3} IN line, supply bypass of this line is the most critical, and may be necessary in some cases. In the most stubborn layouts, up to 0.47µF may be necessary. Both $V_{CC\ OUT}$ and $V_{PP\ OUT}$ pins may have 0.01µF to 0.1µF capacitors for noise reduction and electrostatic discharge (ESD) damage prevention. Larger values of output capacitor might create current spikes during transitions, requiring larger bypass capacitors on the V_{CC3} IN, V_{CC5} IN, and V_{PP} IN pins.

PCMCIA Implementation

The Personal Computer Memory Card International Association (PCMCIA) specification requires two V_{PP} supply pins per PCMCIA slot. V_{PP} is primarily used for programming Flash (EEPROM) memory cards. The two V_{PP} supply pins may be programmed to different voltages. Fully implementing PCMCIA specifications requires a MIC2560, a MIC2557 PCMCIA V_{PP} Switching Matrix, and a controller. Figure 3 shows this full configuration, supporting both 5.0V and 3.3V V_{CC} operation.

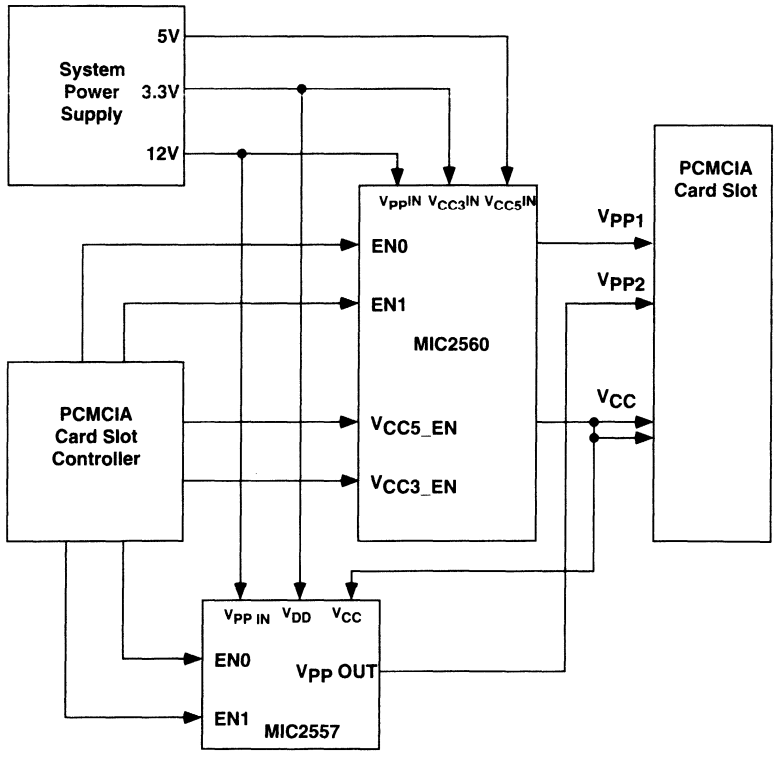


Figure 3. MIC2560 Typical PCMCIA memory card application with dual V_{CC} (5.0V or 3.3V) and separate V_{PP1} and V_{PP2}.

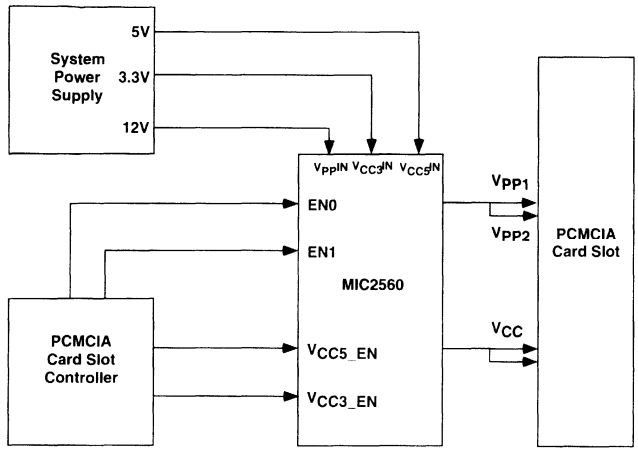


Figure 4. MIC2560 Typical PCMCIA memory card application with dual V_{CC} (5.0V or 3.3V). Note that V_{PP1} and V_{PP2} are driven together.

However, many cost sensitive designs (especially notebook/ palmtop computers) connect V_{PP1} to V_{PP2} and the MIC2557 is not required. This circuit is shown in Figure 4.

When a memory card is initially inserted, it should receive V_{CC} — usually 5.0V ±5%. The card sends a handshaking data stream to the controller, which then determines whether or not this card requires V_{PP} and if the card is designed for 5.0V or 3.3V V_{CC}. If the card uses 3.3V V_{CC}, the controller commands this change, which is reflected on the $V_{CC\ OUT}$ pin of the MIC2560. ***The PCMCIA is presently changing this procedure. Please refer to the latest PCMCIA specification for details.***

During Flash memory programming with standard (+12V) Flash memories, the PCMCIA controller outputs a (1,0) to the EN0, EN1 control pins of the MIC2560, which connects V_{PP} IN to $V_{PP\ OUT}$. The low ON resistance of the MIC2560 switches allow using small bypass capacitors (in some cases, none at all) on the $V_{CC\ OUT}$ and $V_{PP\ OUT}$ pins, with the main filtering action performed by a large filter capacitor on the input supply voltage to V_{PP} IN (usually the main power supply filter capacitor is sufficient). The $V_{PP\ OUT}$ transition from V_{CC} to 12.0V typically takes 250µs. After programming is completed, the controller outputs a (EN1, EN0) = (0,1) to the MIC2560, which then reduces $V_{PP\ OUT}$ to the V_{CC} level for read verification. Break-before-make switching action reduces switching transients and lowers maximum current spikes through the switch from the output capacitor. The flag comparator prevents having high voltage on the $V_{PP\ OUT}$ capacitor from contaminating the V_{CC} inputs, by disabling the low voltage V_{PP} switches until $V_{PP\ OUT}$ drops below the V_{CC} level selected. The lockout delay time varies with the load current and the capacitor on $V_{PP\ OUT}$. With a 0.1µF capacitor and nominal $I_{PP\ OUT}$, the delay is approximately 250µs.

If no card is inserted or the system is in sleep mode, the controller outputs a (V_{CC3} IN, V_{CC5} IN) = (0,0) to the MIC2560, which shuts down V_{CC}. This also places the switch into a high impedance output shutdown (sleep) mode, where current consumption drops to nearly zero, with only tiny CMOS leakage currents flowing.

Internal drive and bias voltage is derived from V_{PP} IN. Internal device control logic is powered from V_{CC3} IN. Input logic threshold voltages are compatible with common PCMCIA controllers using either 3.3V or 5V supplies. No pull-up resistors are required at the control inputs of the MIC2560.

Output Current

MIC2560 output switches are capable of more current than needed in PCMCIA applications and meet or exceed all PCMCIA specifications. For system and card protection, output currents are internally limited. For full system protection, long term (millisecond or longer) output short circuits invoke over-temperature shutdown, protecting the MIC2560, the system power supplies, the card socket pins, and the memory card.

Suspend Mode

An additional feature in the MIC2560 is a pseudo power-down mode, Suspend Mode, which allows operation without a V_{PP} IN supply. In Suspend Mode, the MIC2560 supplies 3.3V to V_{CC} OUT whenever a V_{CC} output of 3.3V is enabled by the PCMCIA controller. This mode allows the system designer the ability to turn OFF the V_{PP} supply generator to save power when it is not specifically required. The PCMCIA card receives V_{CC} at reduced capacity during Suspend Mode, as the switch resistance rises to approximately 4.5Ω.

High Current V_{CC} Operation Without a +12V Supply

Figure 5 Shows the MIC2560 with V_{CC} switch bias provided by a simple charge pump. This enables the system designer to achieve full V_{CC} performance without a +12V supply, which is often helpful in battery powered systems that only provide +12V when it is needed. These on-demand +12V supplies generally have a quiescent current draw of a few

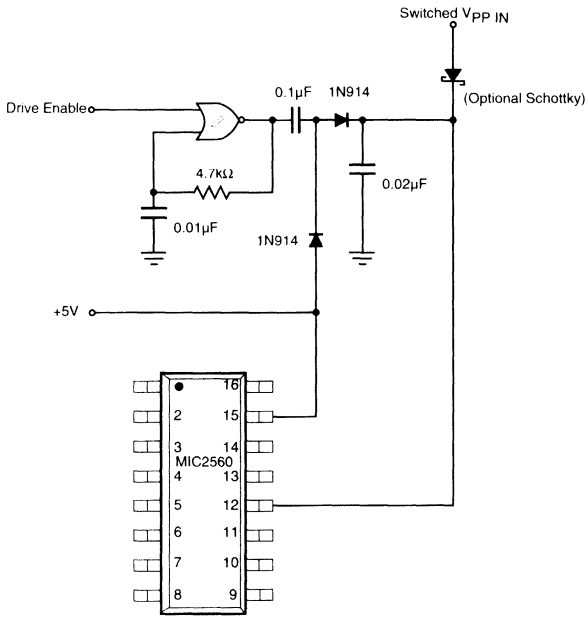


Figure 5. Circuit for generating bias drive for the V_{CC} switches when +12V is not readily available.

milliamperes, which is far more than the microamperes used by the MIC2560. The charge pump of figure 5 provides this low current, using about 100µA when enabled. When $V_{PP\ OUT}$ = 12V is selected, however, the on-demand V_{PP} generator must be used, as this charge pump cannot deliver the current required for Flash memory programming. The Schottky diode may not be necessary, depending on the configuration of the on-demand +12V generator and whether any other loads are on this line.

9

MIC5204

SCSI-II Active Terminator

Preliminary Information–Production Q1 '94

General Description

The MIC5204 is an active terminator designed to comply with SCSI-II specifications. The MIC5204 is enabled by a CMOS or TTL compatible logic signal. When disabled, power consumption drops nearly to zero and the output goes into a high impedance state. Key MIC5204 features include protection against reversed battery, current limiting, and over-temperature shutdown.

Features

- ± 1% Output voltage accuracy
- Guaranteed 1A output
- Low quiescent current
- Low dropout voltage
- Extremely tight load and line regulation
- Very low temperature coefficient
- Current and thermal limiting
- Zero OFF mode current
- Logic-controlled electronic shutdown
- Available in SO-8 and SOT-223 packages

Applications

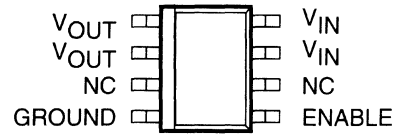
- SCSI–II Active Terminator
- Desktop, Laptop, Notebook, and Palmtop Computers
- Intelligent Instrumentation
- Printers
- Disk Drives
- Voltage Reference

Ordering Information

Part Number	Temperature Range*	Package
MIC5204BM	–40°C to +125°C	SO-8
MIC5204BS	–40°C to +125°C	SOT-223

** Junction Temperature*

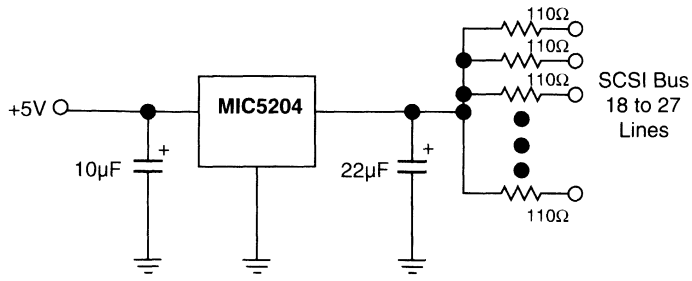
Pin Configuration

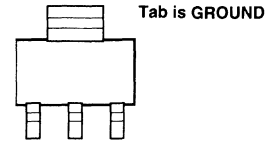


MIC5204BM

Both V_{IN} and both V_{OUT} pins must be tied together. ENABLE must be pulled high for operation.

Typical Application





MIC5204BS

Absolute Maximum Ratings

Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Electrical specifications do not apply when operating the device beyond its specified **Operating Ratings.**

Power Dissipation	Internally Limited
Lead Temperature (Soldering, 5 seconds)	260°C
Operating Junction Temperature Range	–40°C to +125°C
Input Supply Voltage	–20V to +20V
ENABLE Input Voltage	–0.3V to +20V
ESD Rating	> 2000V

Recommended Operating Conditions

Input Voltage	3V to 6V
Operating Junction Temperature Range	–40°C to +125°C
ENABLE Input Voltage	–0.3V to V_{CC}

Electrical Characteristics

Limits in standard typeface are for T_J = 25°C and limits in **boldface** apply over the junction temperature range of –40°C to +125°C. Unless otherwise specified, $V_{IN} = V_{OUT} + 1V$, I_L = 1mA, C_L = 3.3µF, and $V_{ENABLE} \geq 2.0V$

Symbol	Parameter	Conditions	Min	Typical	Max	Units
V_O	Output Voltage Accuracy		2.8215 **2.793**		2.8785 **2.907**	V
$\frac{\Delta V_O}{\Delta T}$	Output Voltage Temperature Coef.	(Note 2)		**20**	**100**	ppm/°C
$\frac{\Delta V_O}{V_{IN}}$	Line Regulation	$V_{IN} = V_{OUT}$ + 1 V to 6V		0.004	0.10 **0.40**	%
$\frac{\Delta V_O}{I_L}$	Load Regulation	I_L = 0.1mA to 100mA (Note 3)		0.04	0.16 **0.30**	%
$V_{IN} - V_O$	Dropout Voltage (Note 4)	I_L = 100µA I_L = 50mA I_L = 100mA I_L = 750mA I_L = 1000mA		30 **75** 190 **240** 210 **350** 600 **1000** 750 **1200**		mV
I_Q	Quiescent Current	$V_{ENABLE} \leq 0.7V$ (Shutdown)		0.01		µA
I_{GND}	Ground Pin Current	$V_{ENABLE} \geq 2.0V$, I_L = 100µA I_L = 20mA I_L = 30mA I_L = 50mA I_L = 100mA		130 240 300 450 900		µA
PSRR	Ripple Rejection			70		dB
I_{GNDDO}	Ground Pin Current at Dropout	V_{IN} = 0.5V less than designed V_{OUT} I_L = 100µA (Note 5)		270	**330**	µA
I_{LIMIT}	Current Limit	V_{OUT} = 0V		**1.5**		A
$\frac{\Delta V_O}{\Delta P_D}$	Thermal Regulation	(Note 6)		0.05		%/W
e_n	Output Noise			30		µV

ENABLE Input

V_{IL}	Input Voltage Level Logic Low Logic High	 OFF ON	 **2.0**		**0.7**	V
I_{IL} I_{IH}	ENABLE Input Current	$V_{IL} \leq 0.7V$ $V_{IH} \geq 2.0V$		0.01 15	 **50**	µA

Note 1: Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device outside of its rated operating conditions. The maximum allowable power dissipation is a function of the maximum junction temperature, $T_{J\,(MAX)}$, the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using: $P_{(MAX)} = (T_{J(MAX)} - T_A)\,\theta_{JA}$. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the regulator will go into thermal shutdown. The θ_{JC} of the MIC5204BS is 15°C/W and θ_{JA} for the MIC5204BM is 160°C/W mounted on a PC board (see "Thermal Considerations" section for further details).

Note 2: Output voltage temperature coefficient is defined as the worst case voltage change divided by the total temperature range.

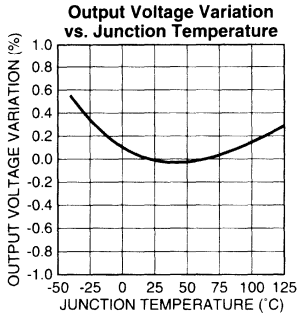
Note 3: Regulation is measured at constant junction temperature using low duty cycle pulse testing. Parts are tested for load regulation in the load range from 0.1mA to 100mA. Changes in output voltage due to heating effects are covered by the thermal regulation specification.

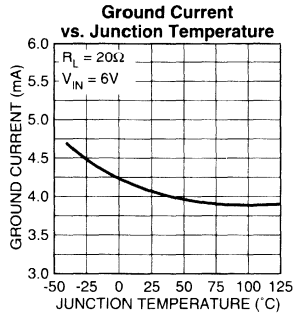
Note 4: Dropout Voltage is defined as the input to output differential at which the output voltage drops 2% below its nominal value measured at 1V differential.

Note 5: Ground pin current is the regulator quiescent current plus pass transistor base current. The total current drawn from the supply is the sum of the load current plus the ground pin current.

Note 6: Thermal regulation is defined as the change in output voltage at a time T after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for a 1A load pulse at V_{IN} = 6V for T = 10ms.

Typical Characteristics





Applications Information

External Capacitors

A 2.2µF capacitor is recommended between the MIC5204 output and ground to prevent oscillations due to instability. Larger values serve to improve the regulator's transient response. Most types of tantalum or aluminum electrolytics will be adequate; film types will work. Many aluminum electrolytics have electrolytes that freeze at about –30°C, so solid tantalums are recommended for operation below –25°C. The important parameters of the capacitor are an effective series resistance of about 5Ω or less and a resonant frequency above 500kHz. The value of this capacitor may be increased without limit.

A 1µF capacitor should be placed from the MIC5204 input to ground if there is more than 10 inches of wire between the input and the AC filter capacitor or if a battery is used as the input.

The MIC5204 will remain stable and in regulation with no load in addition to the internal voltage divider.

Thermal Considerations

Part I. Layout

The MIC5204BM (8-pin surface mount package) has the following thermal characteristics when mounted on a single layer copper-clad printed circuit board.

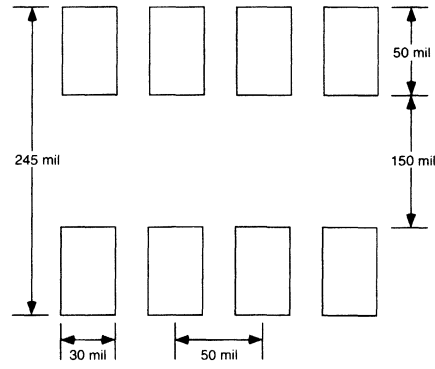
PC Board Dielectric	θ_{JA}
FR4	160°C/W
Ceramic	120°C/W

Multi-layer boards having a ground plane, wide traces near the pads, and large supply bus lines provide better thermal conductivity. The "worst case" value of 160°C/W assumes no ground plane, minimum trace widths, and a FR4 material board.

Part II. Nominal Power Dissipation and Die Temperature

The MIC5204BM at a 25°C ambient temperature will operate reliably at up to 625mW power dissipation when mounted in the "worst case" manner described above. At an ambient temperature of 55°C, the device may safely dissipate 440mW. These power levels are equivalent to a die temperature of 125°C, the recommended maximum temperature for non-military grade silicon integrated circuits. In normal SCSI terminator applications, the average power dissipation is very small and this minimum geometry heat sink is suitable. The total dissipation does not approact the 400mW to 625mW range described above.

For MIC5204BS (SOT-223 package) heat sink characteristics, please refer to Micrel Application Hint 17, "P.C. Board Heat Sinking". As with the SO-8, average power dissipation in SCSI terminator applications is low and a minimum pad size is generally adequate.



Minimum recommended board pad size, SO-8.

Application Note 8

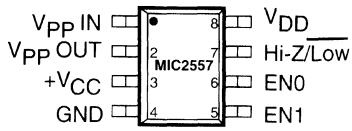
Interfacing the MIC2557/8 to PCMCIA Controllers

by Bob Wolbert

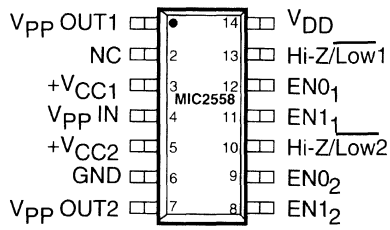
General Description

The MIC2557 and MIC2558 provide "Programming and Peripheral" voltage (V_{PP}) switching for PCMCIA card sockets. They have simple logic compatible inputs and easily interface with industry standard PCMCIA controllers. This note gives circuit examples for several PCMCIA controllers. For controllers supporting dual V_{CC} (3.3V and 5.0V), two simple high current V_{CC} switch matrices are shown.

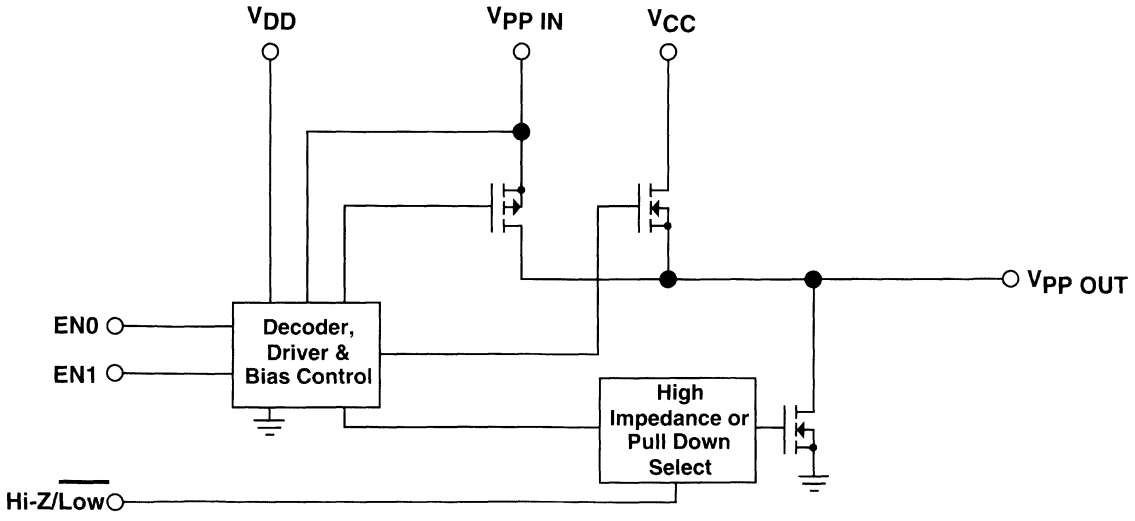
Pin Configuration



PCMCIA
PC Card
MEMBER COMPANY



MIC2557 (½ MIC2558) Block Diagram



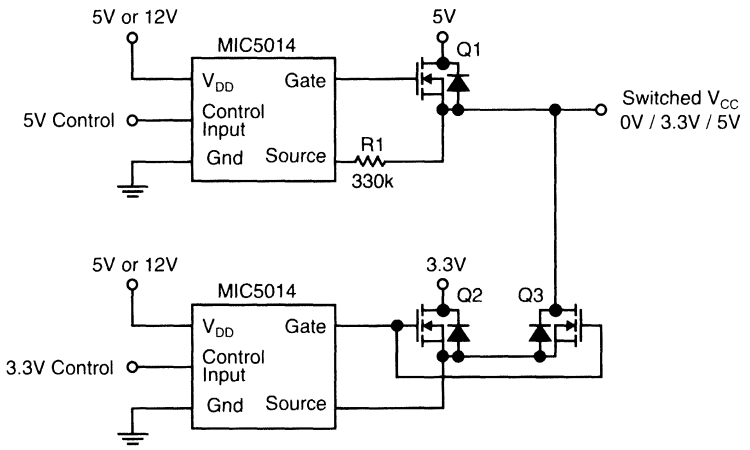


Figure 1. PCMCIA Compatible Dual V_{CC} Switch Matrix. This circuit uses power MOSFETs driven by two MIC5014 high side MOSFET drivers to select between 3.3V and 5V V_{CC}. MOSFET "body diodes" are shown for information.

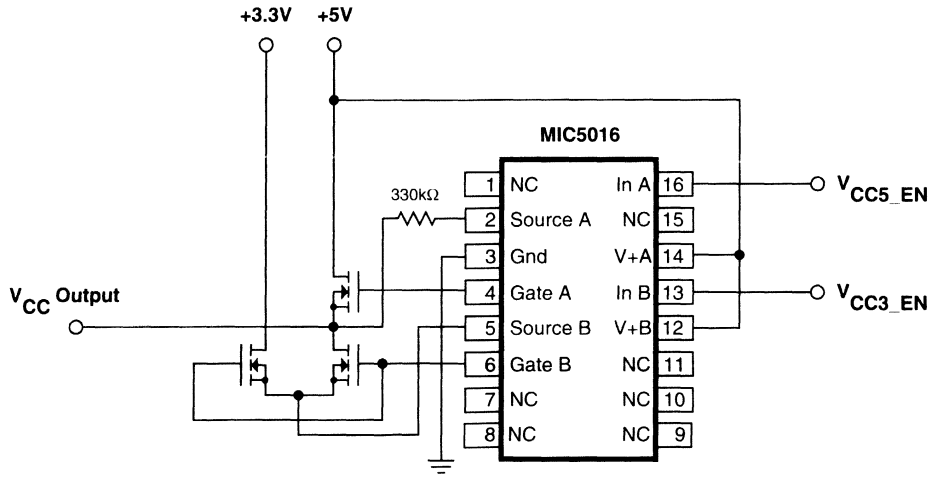


Figure 2. PCMCIA Compatible Dual V_{CC} Switch Matrix. This circuit uses power MOSFETs driven by a single MIC5016 high side MOSFET drivers to select between 3.3V and 5V V_{CC}.

V_{CC} Switching

Figures 1 and 2 show the MIC5014 and MIC5016 high side power MOSFET drivers configured as a V_{CC} select matrix. Both circuits operate identically; the MIC5016 is a dual MIC5014. For convenience, we will discuss the circuit operation referring to Figure 1. Initially, both MOSFET drivers are OFF and the MOSFET gates are clamped low, placing the V_{CC} output in the high impedance condition. A TTL High level on V_{CC5_EN} enables Q1, and 5V appears on $V_{CC\ OUT}$. Likewise, when V_{CC3_EN} is High, Q2 and Q3 are ON and 3.3V appears on the output. V_{CC5_EN} and V_{CC3_EN} are mutually exclusive: circuit damage might occur if both switches are commanded ON simultaneously.

The inherent "body diode" of the power MOSFET, shown in Figure 1, creates circuit problems that are dealt with by adding another MOSFET, Q3, connected in the reverse direction. Without Q3, whenever the 5V supply is enabled, current would flow from $V_{CC\ OUT}$ through the body diode of Q2 into the 3.3V supply, thereby contaminating the low voltage supply. Q3's reverse direction connects its body diode anode

to anode with Q2 and eliminates reverse current. When V_{CC3_EN} is High and the MIC5014 enhances the MOSFET gates, both Q2 and Q3 are ON, and 3.3V appears on $V_{CC\ OUT}$. The enhanced channel shorts out the body diodes, so no diode forward voltage drop is evident. The ON resistance of Q3 is slightly higher in its reverse direction than in normal operation, but with reasonably sized MOSFETs, the voltage drop is small. Although a Schottky diode would provide the required protection, its forward voltage drop is much too large and would prevent the 3.3V switch from meeting its ±5% accuracy requirement.

Cirrus Logic CL-PD6710

The Cirrus Logic CL-PD6710 provides support for a single PCMCIA socket. Key features include full support for dual V_{CC} voltages (3.3V and 5.0V). The CL-PD6710 assumes V_{PP1} is tied to V_{PP2}. The MIC2557, in a small 8-pin surface mount package, provides V_{PP} power control for this single socket. V_{CC} switching is accomplished using the circuit of (either) Figure 1 or Figure 2. Note that no additional components are required, although filter capacitors are recommended for best performance.

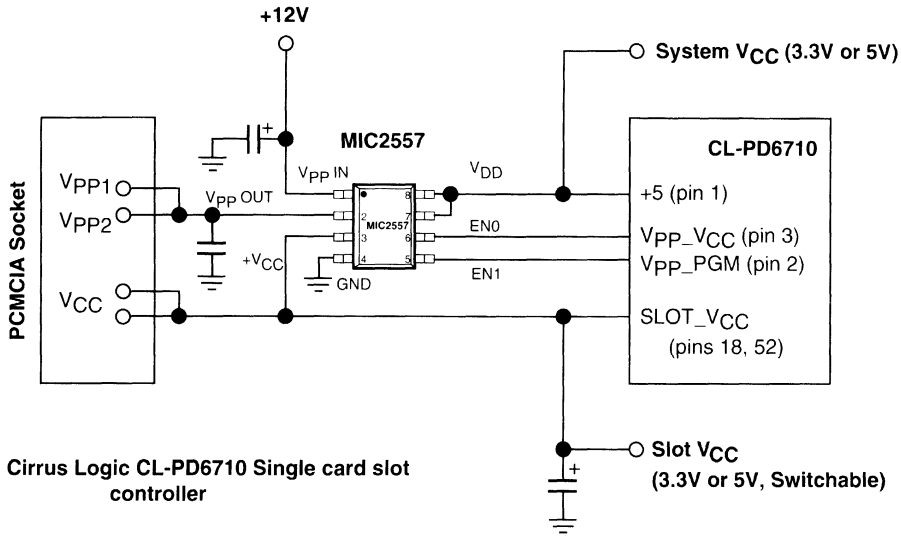


Figure 3. Cirrus Logic CL-PD6710 Single card slot controller

CL-PD6710 & CL-PD6720 Control Logic

V_{CC5_EN}	V_{CC3_EN}	V_{PP_PGM} (EN1)	V_{PP_VCC} (EN0)	$V_{CC\ OUT}$	$V_{PP\ OUT}$
0	0	0	0	High Z	Clamped to Ground
0	0	0	1	High Z	High Z
0	0	1	0	High Z	High Z
0	0	1	1	High Z	High Z
0	1	0	0	5	Clamped to Ground
0	1	0	1	5	5
0	1	1	0	5	12
0	1	1	1	5	High Z
1	0	0	0	3.3	Clamped to Ground
1	0	0	1	3.3	3.3
1	0	1	0	3.3	12
1	0	1	1	3.3	High Z
1	1	0	0	High Z	Clamped to Ground
1	1	0	1	High Z	High Z
1	1	1	0	High Z	High Z
1	1	1	1	High Z	High Z

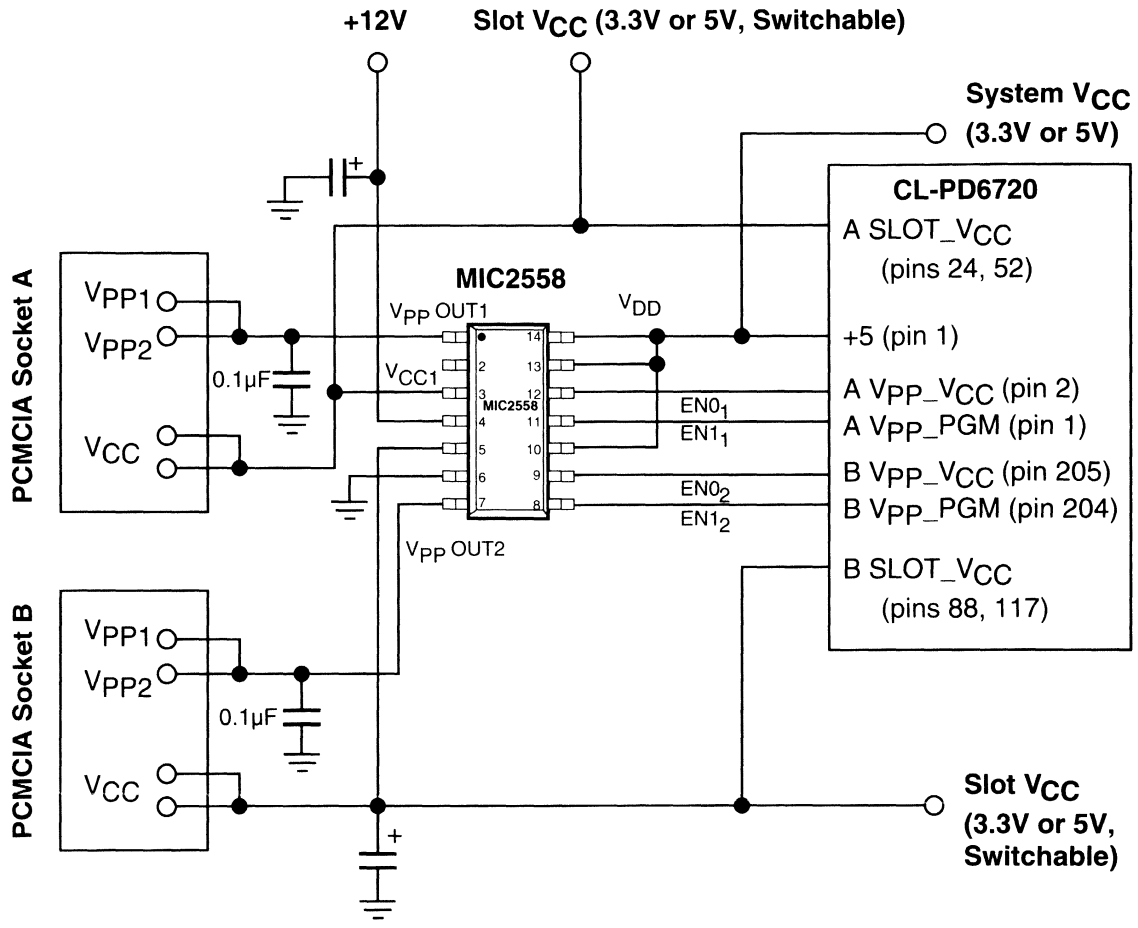


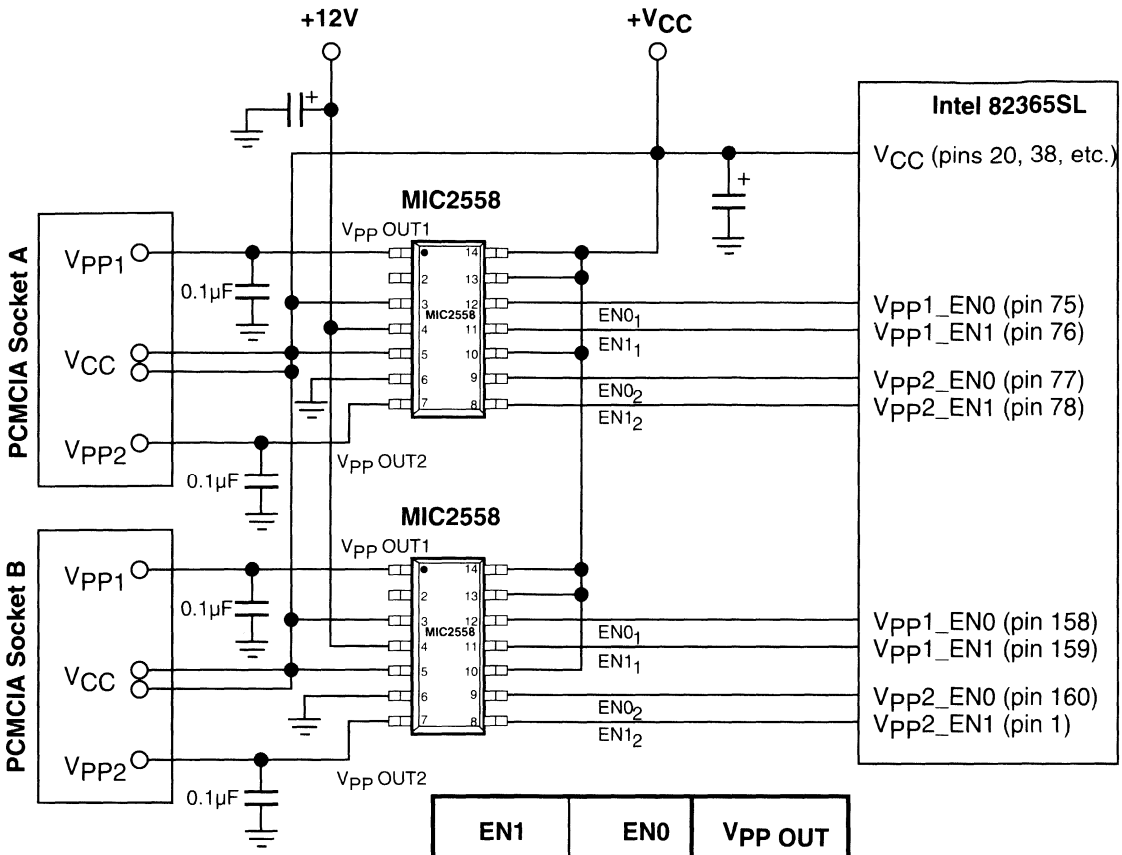
Figure 4. Cirrus Logic CL-PD6720 dual slot PCMCIA controller

9

Cirrus Logic CL-PD6720

As shown in Figure 4, the Cirrus Logic CL-PD6720 provides support for two PCMCIA sockets. Key features include full support for dual V_{CC} voltages. The CL-PD6720 assumes V_{PP1} is tied directly to V_{PP2}. The MIC2558, in a small 14-pin surface mount package, provides all necessary V_{PP} power control for both sockets. V_{CC} switching is accomplished using the circuit of (either) Figure 1 or Figure 2. No additional components are necessary, but filter capacitors are recommended for best performance.

A complete dual slot PCMCIA power control subsystem using this controller appears as Figure 8.



EN1	EN0	VPP OUT
0	0	0
0	1	VCC
1	0	VPP
X	X	0 (reserved)

Figure 5. Intel 82365SL "PC Card Interface Controller (PCIC)" implementation

Intel 82365SL

The Intel 82365SL supports fully independent V_{PP1} and V_{PP2} for two PCMCIA slots. Two MIC2558 allow the necessary voltage combinations for all four V_{PP} pins. No additional components are necessary, although filter capacitors are recommended for best performance. The Intel 82365SL does not support dual V_{CC} selection, so no other power control is required. V_{CC} ON/OFF is supported, and may be implemented by a simple V_{CC} switch consisting of a MIC5014 and a single power MOSFET (per slot). Refer to Figure 6 for details on this ON/OFF V_{CC} switch.

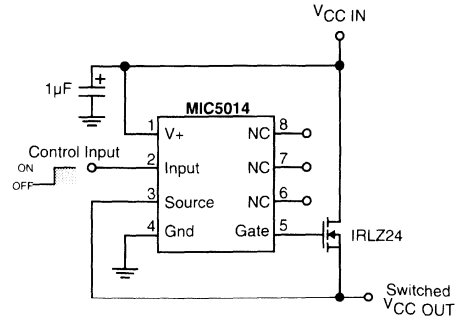


Figure 6. V_{CC} ON/OFF Switch for use with the Intel 82365SL.

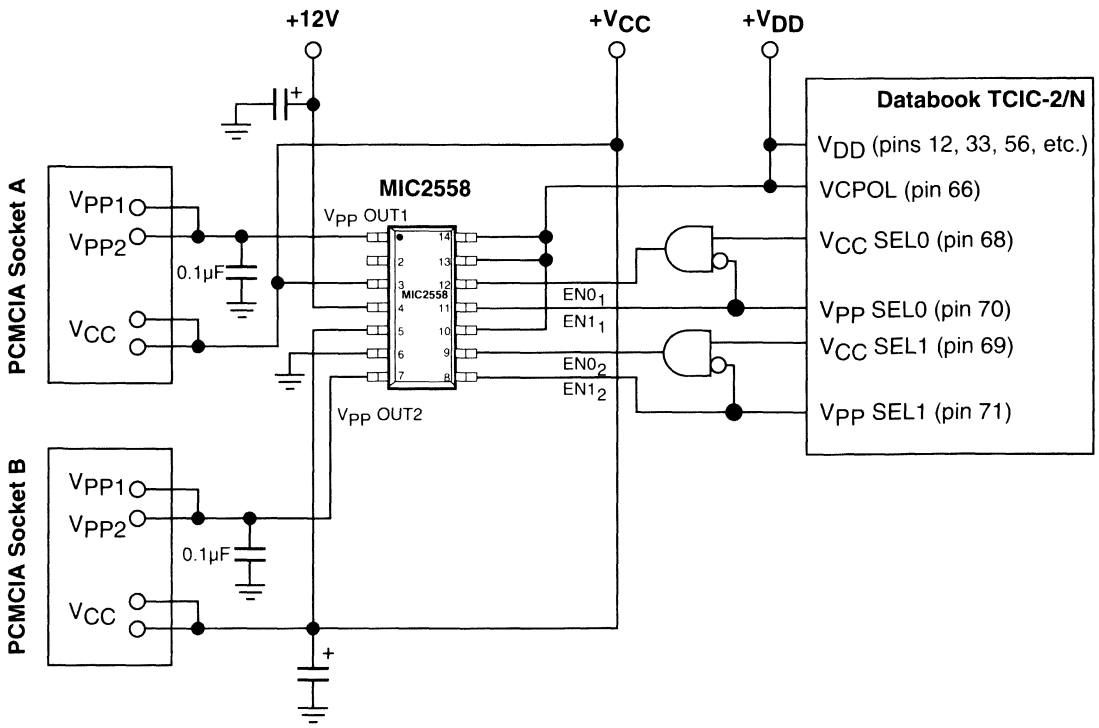


Figure 7. Databook TCIC-2/N family PCMCIA controller interfacing with the MIC2558.

V_{PP} SEL	V_{CC} SEL	EN1	EN0	V_{PP} OUT
0	0	0	0	0
0	1	0	1	V_{CC}
1	1	1	0	V_{PP}
1	0	X	X	0 (illegal)

Databook TCIC-2/N Control Logic

Databook TCIC-2/N Family

The Databook TCIC-2/N family of PCMCIA controllers has V_{PP} and V_{CC} voltage enable signals a bit different than provided by the other controllers. A logic gate is necessary to complete the interface between the TCIC-2/N and the MIC2558. The TCIC-2/N has a pin, VCPOL, which controls the polarity of the output enable signals. When VCPOL is tied to V_{DD}, the control signals are active high, and with VCPOL low, the control outputs are active low. The configuration shown uses the active high option.

Complete PCMCIA Power Control Circuitry Using MIC2558 and Cirrus Logic CL-PD6720

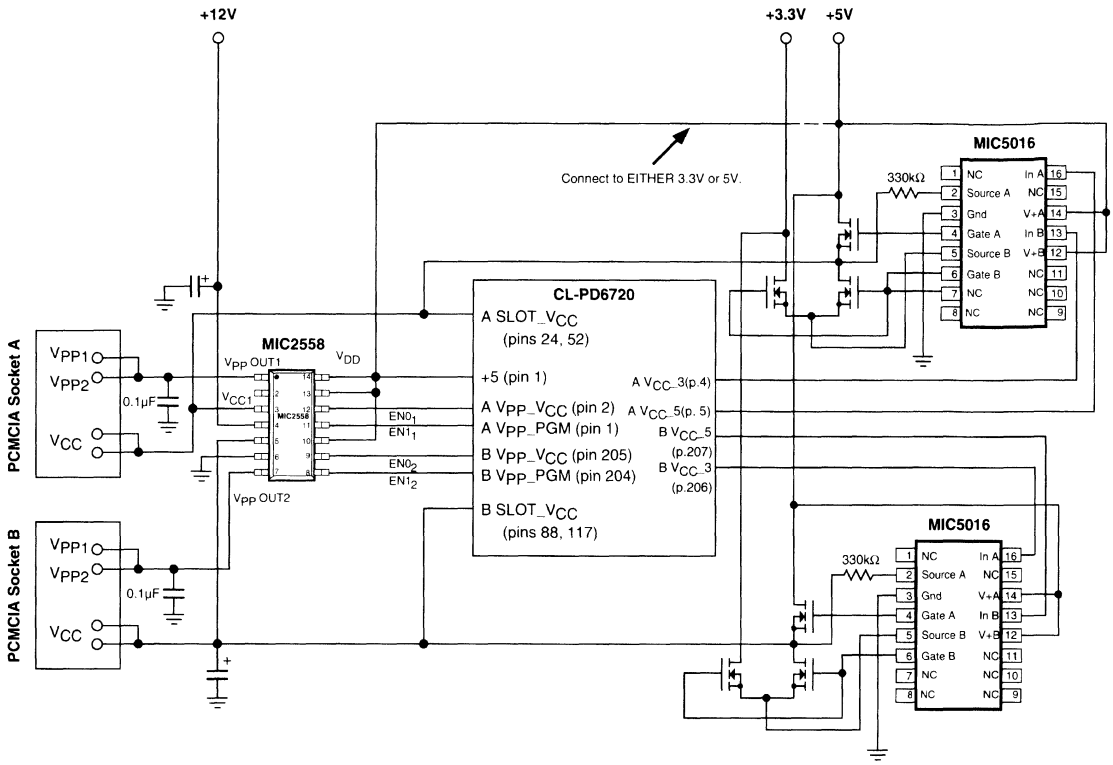


Figure 8. Complete dual slot PCMCIA power control system using MIC2558 and Cirrus Logic CL-PD6720

Figure 7 shows a complete dual slot PCMCIA power control implementation for dual V_{CC} systems. CL-PD6720 pin 1 ("+5V") is connected to 5V if available, and to 3.3V if the logic lines are powered from this voltage. This pin, and the MIC2558 V_{DD} pin (pin 14) set up reference levels for the logic input pins (and output pins on the CL-PD6720).

As of the time of this writing, the PCMCIA field is quite dynamic. Please contact Micrel for the latest information on PCMCIA controller compatibility and new Micrel devices designed for this application.

Application Hint 15

A High Current V_{CC} Switching Matrix

by Brenda Kovacevic

Introduction

Some applications require a multiplexer that can deliver two or more supply voltages at 1A or greater. An example is the V_{CC} multiplexer for the PCMCIA interface. A low cost multiplexer for high current loads can be made using the Micrel MIC5014 and a few discrete power MOSFETs. A simple 3.3V and 5V switch is shown in Figure 1. Since low cost discrete MOSFETs are available with ON resistances of a few milli-ohms, these multiplexers can manage currents exceeding several tens of amperes.

The MIC5014

Making this solution possible is the MIC5014 MOSFET driver. This driver is designed to provide gate enhancement above the positive rail for an N-channel FET. N-channel FETs have the advantages of lower cost and lower $R_{DS(ON)}$ than similar P-channel FETs. The MIC5014 consumes a maximum of 1µA in the OFF state and typically 100µA in the ON state while powered from a 5V supply. The MIC5014 does not require its supply to be the input logic supply since the control input threshold is approximately 1.2V and is independent of supply voltage. Likewise, the MIC5014 does not require its supply to be the MOSFET drain supply voltage because the voltage supplied to the gate is regulated and will not exceed 16V above the source voltage and is also independent of the supply voltage. The MIC5014 is available in an 8-pin SOIC package which helps minimizes the size of the complete switch matrix.

The Switch Matrices

Figure 1 shows the basic switching matrix configurations. Q1 through Q3 can be any low impedance N-channel power FETs. Table 1 shows the expected V_{OUT} for several FETs with different $R_{DS(ON)}$ values.

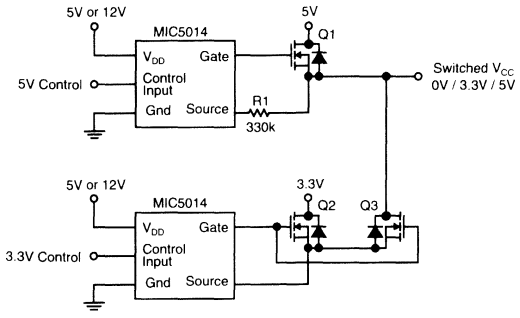


Figure 1. Switch Matrix for 0V, 3.3V, and 5V

Each FET has its body internally connected to its source, resulting in an intrinsic diode between the body and the drain known as a "body diode." Figure 1 shows that the body diode does not present a problem for the Q1 switch, because it is always reverse biased. If Q3 were not in the circuit and the source of Q2 connected directly to the output, then Q2's body diode would be reverse biased when both Q1 and Q2 are OFF and the output voltage is zero. However, Q2's body diode would be forward biased when Q1 is ON and the 5V supply would be shorted to the 3.3V supply through Q1 and the forward biased body diode of Q2. Similarly, if Q2 were not in the circuit and the source of Q3 connected to 3.3V, then Q3's body diode would be reverse biased when Q1 is ON but forward biased when both Q1 and Q3 are OFF and the load would be held one diode drop below 3.3V. With two MOSFETs connected back to back, both body diodes will be reverse biased when all switches are OFF as long as the output voltage remains positive with respect to ground. Although Q3 conducts current in the reverse direction when it is ON, the body diode will not conduct because it is shorted by Q3's ON resistance.

FET Part Number	$R_{DS(ON)}$	V_{OUT} at 1A	
		5.0V Input	3.3V Input
IRFZ20	100mΩ	4.9V	3.1V
IRFZ30	50mΩ	4.95V	3.20V
SMP06N06-14	14mΩ	4.99V	3.27V

Table 1. Power FETs and Expected Output Voltages at 1A

Low Current PCMCIA V_{PP} Switching Matrices

If V_{PP} programming currents are switched, the new MIC2557/2558 devices provide all level shifting, timing, and high current switches for this function in one package. The MIC2557 serves as a single channel and is available in an 8-pin SOIC package (see Figure 2). The MIC2558 is a dual channel device, and is available in a 14-pin SOIC package (see Figure 3). See the MIC2557 or MIC2558 data sheets for full details.

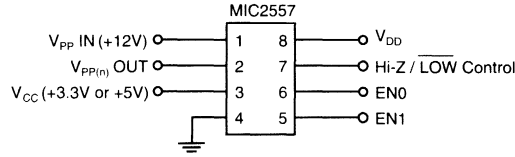


Figure 2. Typical MIC2557 Application

9

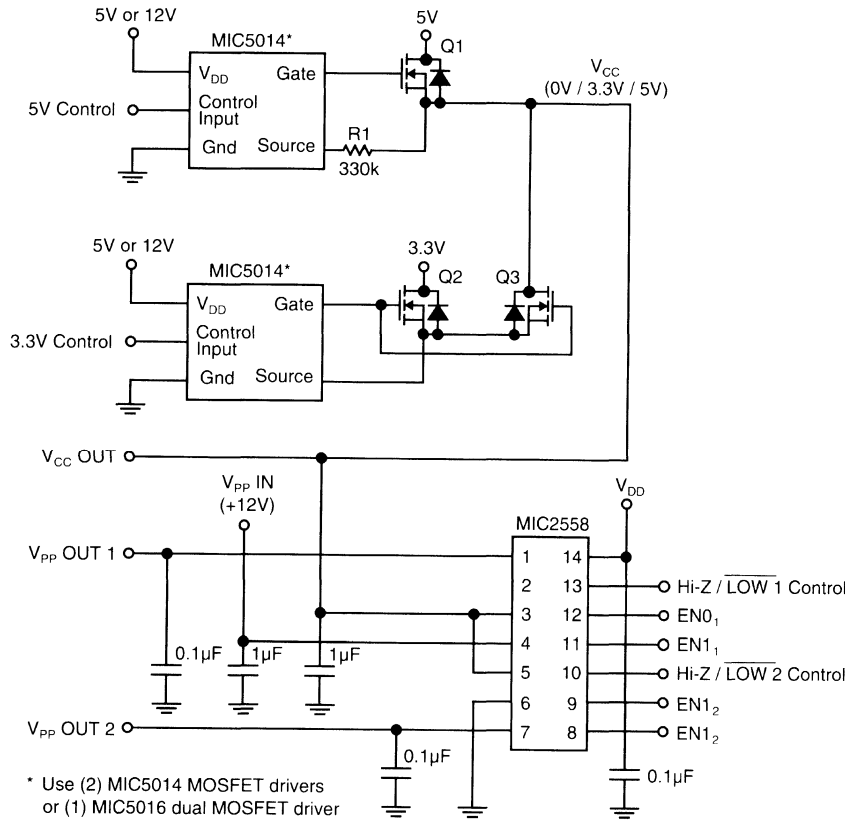


Figure 3. Full PCMCIA V_{PP} and V_{CC} Circuit using MIC5014 (or MIC5016) and MIC2558

SECTION 10 : MOSFET SWITCHES

TinyFET is a trademark of Micrel Inc.

MIC94001BLM

P-Channel MOSFET

Preliminary Information

General Description

The MIC94001BLM is a silicon gate P-channel MOSFET designed for low ON resistance high-side switch applications. The MIC94001BLM has a maximum ON resistance of 0.4Ω at 4.5V gate to source voltage.

The MIC94001 also functions (with a lower threshold voltage specification of 0.8V to 2V) at 2.7V gate-to-source voltage with approximately double the 4.5V gate-to-source voltage ON resistance. Contact the factory for more information.

Improved ESD protection is provided by the gate protection network shown in the schematic diagram.

The MIC94001BLM is supplied in a low-profile version of the 8-lead SOIC package.

The MIC94001 die can be assembled in a 4-terminal configuration with the body not shorted to the source for use in analog switch applications. Contact the factory for more information.

Features

- 0.4Ω maximum ON resistance at 4.5V gate to source voltage
- Functional at 2.7V gate to source voltage
- 0.063" maximum height

Applications

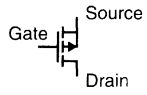
- High-side Switch
- Stepper Motor Control
- Logic Switching
- Power Management
- 1.8" PCMCIA disk drive V_{CC} switch

Ordering Information

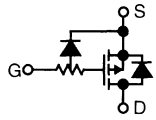
Part Number	Temperature Range*	Package
MIC94001BLM	–55°C to +150°C	8-lead SOIC†

* Operating Junction Temperature
† Low Profile Leads, see Package Information

Schematic Information

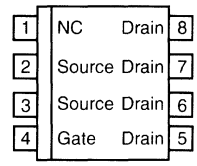


Schematic Symbol



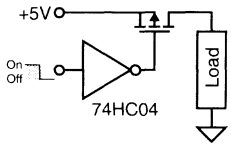
Schematic Diagram

Pin Configuration



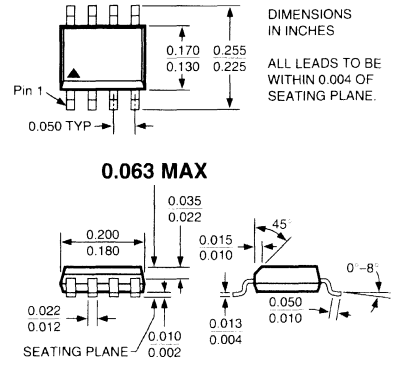
8-lead Low-Profile SOIC Package (LM)

Typical Application



Power Switch Application

Package Information



Patents Pending

Absolute Maximum Ratings

Voltage and current values are negative. Signs not shown for clarity.

Drain to Source Voltage 15V
Gate to Source Voltage 15V
Continuous Drain Current
T_A = 25°C 1.6A
T_A = 100°C 1A
Operating Junction Temperature ..... –55°C to +150°
Storage Temperature ..... –55°C to +150°C

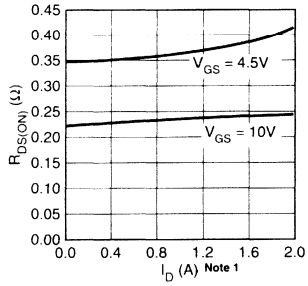
Total Power Dissipation
T_A = 25°C 1W
T_A = 100°C 0.4W
Thermal Resistance
θ_{JA} ..... 125°C/W
θ_{JC} ..... 76°C/W
Lead Temperature
1/16" from case, 10s ..... +300°C

Electrical Characteristics T_A = 25°C unless noted. *All values are negative. Signs not shown for clarity.*

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{BDSS}	Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250µA	15			V
V_{GS}	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250µA	1		3	V
I_{GSS}	Gate-Body Leakage	V_{DS} = 0V, V_{GS} = 15V, **Note 2**			100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 15V, V_{GS} = 0V			25	µA
		V_{DS} = 15V, V_{GS} = 0V, T_J = 125°C			250	µA
$I_{D(ON)}$	On-State Drain Current	V_{DS} ≥ 10V, V_{GS} = 10V	2.3			A
$R_{DS(ON)}$	Drain-Source ON-State Resist.	V_{GS} = 4.5V, I_D = 50mA, **Note 1**		0.35	0.40	Ω
g_{FS}	Forward Transconductance	V_{DS} = 15V, I_D = 1A, **Note 1**	1.9			S

Note 1 Pulse Test: Pulse Width ≤ 300µsec, Duty Cycle ≤ 2%
Note 2 ESD gate protection diode conducts during positive gate to source voltage excursions.

On Resistance vs. Drain Current



10

MIC94002BLM

Dual P-Channel MOSFET

Preliminary Information

General Description

The MIC94002BLM contains two silicon gate P-channel MOSFETs designed for low ON resistance high-side switch applications.

The MIC94002BLM has a maximum ON resistance of 0.4Ω at 4.5V gate to source voltage. ON resistance can also be reduced to half by connecting both MOSFETs in parallel.

The MIC94002 also functions (with a lower threshold voltage specification of 0.8V to 2V) at 2.7V gate-to-source voltage with approximately double the 4.5V gate-to-source voltage ON resistance. Contact the factory for more information.

Improved ESD protection is provided by the gate protection network shown in the schematic diagram.

The MIC94002BLM is supplied in a low-profile version of the 8-lead SOIC package.

The MIC94002 can be assembled with the body not shorted to the sources for use in analog switch applications. Contact the factory for more information.

Features

- 0.4Ω maximum ON resistance at 4.5V gate to source voltage (each MOSFET)
- Functional at 2.7V gate to source voltage
- 0.063" maximum height

Applications

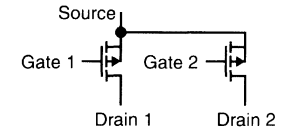
- High-side Switch
- Stepper Motor Control
- Logic Switching
- Power Management
- 1.8" PCMCIA disk drive V_{CC} switch

Ordering Information

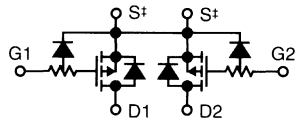
Part Number	Temperature Range*	Package
MIC94002BLM	–55°C to +150°C	8-lead SOIC†

* Operating Junction Temperature
† Low Profile Leads, see Package Information

Schematic Information

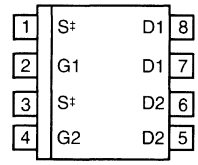


Schematic Symbols



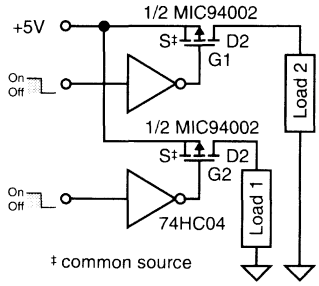
Schematic Diagram

Pin Configuration



8-lead Low-Profile SOIC Package (LM)

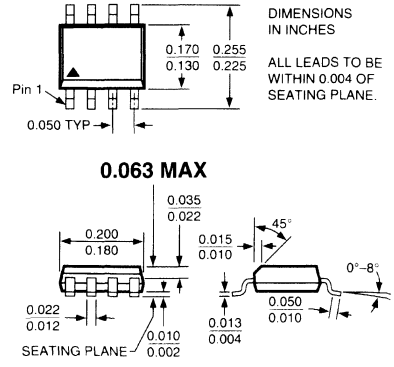
Typical Application



Dual Power Switch Application

Patents Pending

Package Information



Absolute Maximum Ratings

Voltage and current values are negative. Signs not shown for clarity.

Drain to Source Voltage 15V
Gate to Source Voltage 15V
Continuous Drain Current (each MOSFET, both on)
T_A = 25°C 1.2A
T_A = 100°C 0.7A
Operating Junction Temperature ..... –55°C to +150°
Storage Temperature ..... –55°C to +150°C

Total Power Dissipation
T_A = 25°C 1W
T_A = 100°C 0.4W
Thermal Resistance
θ_{JA} ..... 125°C/W
θ_{JC} ..... 76°C/W
Lead Temperature
1/16" from case, 10s ..... +300°C

Electrical Characteristics[Note 1] T_A = 25°C unless noted. *All values are negative. Signs not shown for clarity.*

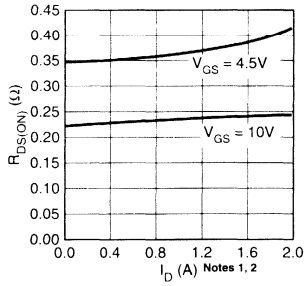
Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{BDSS}	Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250µA	15			V
V_{GS}	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250µA	1		3	V
I_{GSS}	Gate-Body Leakage	V_{DS} = 0V, V_{GS} = 15V, **Note 3**			100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 15V, V_{GS} = 0V			25	µA
		V_{DS} = 15V, V_{GS} = 0V, T_J = 125°C			250	µA
$I_{D(ON)}$	On-State Drain Current	V_{DS} ≥ 10V, V_{GS} = 10V	2.3			A
$R_{DS(ON)}$	Drain-Source ON-State Resist.	V_{GS} = 4.5V, I_D = 50mA, **Note 2**		0.35	0.40	Ω
g_{FS}	Forward Transconductance	V_{DS} = 15V, I_D = 1A, **Note 2**	1.9			S

Note 1 Values for each MOSFET

Note 2 Pulse Test: Pulse Width ≤ 300µsec, Duty Cycle ≤ 2%

Note 3 ESD gate protection diode conducts during positive gate to source voltage excursions.

On Resistance vs. Drain Current



10

MIC94030 and MIC94031

P-Channel TinyFET™ MOSFET

Preliminary Information–Production Q1 '94

General Description

The MIC94030 and MIC94031 are 4-terminal silicon gate P-channel MOSFETs that each provide low R_{ON} in a very small package.

Designed for high-side switch applications where space is critical, the MIC94030/1 exhibits an $R_{DS(ON)}$ of typically 0.75Ω at 4.5V gate-to- source voltage. The MIC94030/1 also operates with only 2.7V gate-to- source voltage.

The MIC94030 is the basic 4-lead P-channel MOSFET. The MIC94031 is a variation that includes an internal gate pull-up resistor which can reduce the system parts count in many applications.

The 4-terminal SOT-143 package permits a substrate connection separate from the source connection. This 4-terminal configuration improves the θ_{JA} (improved heat dissipation) and makes analog switch applications practical.

The small size, low threshold, and low $R_{DS(ON)}$ make the MIC94030/1 the ideal choice for PCMCIA card sleep mode or distributed power management applications.

Features

- 0.75Ω typical ON resistance at 4.5V gate to source voltage
- 0.45Ω typical ON resistance at 10V gate-to-source voltage
- Operates with 2.7V gate to source voltage
- Separate substrate connection for added control
- Industry's smallest surface mount package
- V_{GS} and V_{BDSS} to 13.5V

Applications

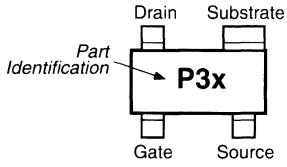
- PCMCIA Card Power Management
- Battery Powered Computers & Peripherals
- Portable Communications Equipment
- Hand Held Bar Code Scanners
- Distributed Power Management

Ordering Information

Part Number	Temperature Range*	Package
MIC94030BM4	–55°C to +150°C	SOT-143
MIC94031BM4	–55°C to +150°C	SOT-143

* Operating Junction Temperature

Pin Configuration

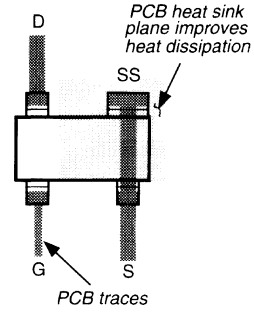


Part Number	Identification
MIC94030BM4	P30
MIC94031BM4	P31

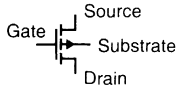
SOT-143 Package (M4)

SOT-143 Package Actual Size

Typical PCB Layout

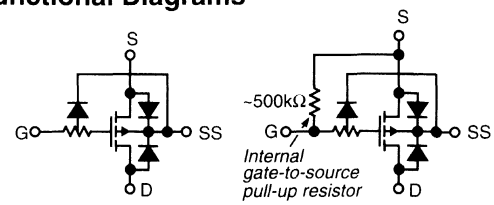


Schematic Symbol



Schematic Symbol

Functional Diagrams



MIC94030 **MIC94031**

TinyFET™ is a trademark of Micrel, Inc. Patents pending.

Absolute Maximum Ratings

Voltage and current values are negative. Signs not shown for clarity.

Drain to Source Voltage 16V
Gate to Source Voltage 16V
Continuous Drain Current
T_A = 25°C 1A
T_A = 100°C 0.5A
Operating Junction Temperature ..... –55°C to +150°
Storage Temperature ..... –55°C to +150°C

Total Power Dissipation
T_A = 25°C 568mW
T_A = 100°C 227mW
Thermal Resistance
θ_{JA} ..... 220°C/W
θ_{JC} ..... 130°C/W
Lead Temperature
1/16" from case, 10s ..... +300°C

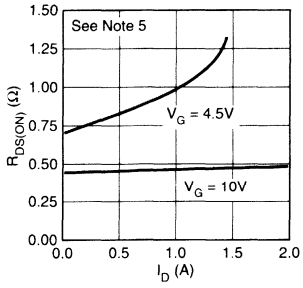
Electrical Characteristics *Voltage and current values are negative. Signs not shown for clarity.*

Symbol	Parameter	Condition (Note 1)	Min	Typ	Max	Units
V_{BDSS}	Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250µA	13.5			V
V_{GS}	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250µA	0.6	1.0	1.4	V
I_{GSS}	Gate-Body Leakage	V_{DS} = 0V, V_{GS} = 12V, **Note 2**, **Note 3**			1	µA
R_{GS}	Gate-Source Resistor	V_{DS} = 0V, V_{GS} = 12V, **Note 2**, **Note 4**		500	1000	kΩ
C_{ISS}	Input Capacitance	V_{GS} = 0V, V_{DS} = 12V		100		pF
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 12V, V_{GS} = 0V			25	µA
		V_{DS} = 12V, V_{GS} = 0V, T_J = 125°C		0.010	250	µA
$I_{D(ON)}$	On-State Drain Current	V_{DS} = 10V, V_{GS} = 10V, **Note 5**		6.3		A
$R_{DS(ON)}$	Drain-Source ON-State Resist.	V_{GS} = 10V, I_D = 100mA V_{GS} = 4.5V, I_D = 100mA V_{GS} = 2.7V, I_D = 100mA		0.45 0.75 1.20	 1.00 	Ω Ω Ω
g_{FS}	Forward Transconductance	V_{DS} = 10V, I_D = 200mA, **Note 5**		480		mS

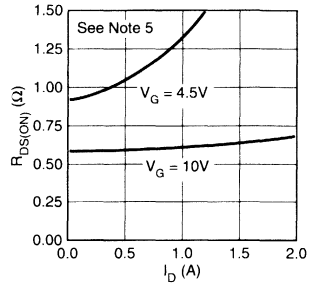
Note 1 T_A = 25°C unless noted. Substrate connected to source for all conditions
Note 2 ESD gate protection diode conducts during positive gate to source voltage excursions.
Note 3 MIC94030 only
Note 4 MIC94031 only
Note 5 Pulse Test: Pulse Width ≤ 80µsec, Duty Cycle ≤ 0.5%

Typical Characteristics

ON Resistance vs. Drain Current at 25°C



On Resistance vs. Drain Current at 125°C



10

Typical Applications

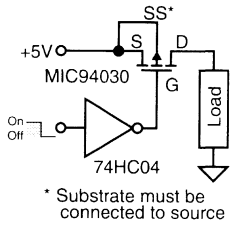


Figure 1. Power Switch Application

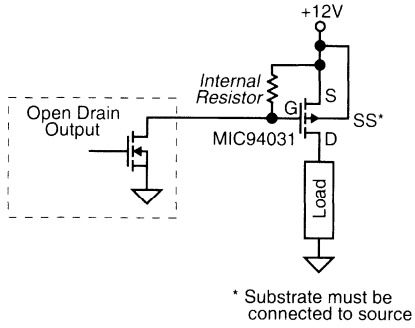
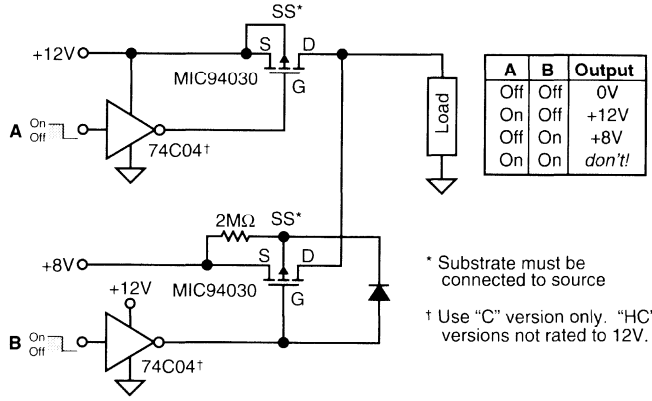


Figure 2. Power Control Application



A	B	Output
Off	Off	0V
On	Off	+12V
Off	On	+8V
On	On	*don't!*

Figure 3. Analog Switch Application

SECTION 11: SPECIAL PURPOSE PRODUCTS

LM4040/4041

Precision Micropower Shunt Voltage Reference

Preliminary Information

General Description

Ideal for space critical applications, the LM4040 and LM4041 precision voltage references are available in the sub-miniature (3mm × 1.3mm) SOT-23 surface-mount package, the SO-8 surface-mount package, or the TO-92 package.

The LM4040 is the available in several fixed reverse breakdown voltages: 2.500V, 4.096V, 5.000V, 8.192V, and 10.000V.

The LM4041 is available with a fixed 1.225V or an adjustable reverse breakdown voltage.

The LM4040 and LM4041's advanced design eliminates the need for an external stabilizing capacitor while ensuring stability with any capacitive load, making them easy to use.

The minimum operating current increases from 60μA for the LM4041-1.2 to 100μA for the LM4040-10.0. LM4040 versions have a maximum operating current of 15mA. LM4041 versions have a maximum operating current of 12mA.

The LM4040 and LM4041 utilizes zener-zap reverse breakdown voltage trim during wafer sort to ensure that the prime parts have an accuracy of better than ±0.1% (A grade) at 25°C. Bandgap reference temperature drift curvature correction and low dynamic impedance ensure stable reverse breakdown voltage accuracy over a wide range of operating temperatures and currents.

Features

- Small Package: SOT-23, TO-92, and SO-8
- No output capacitor required
- Tolerates capacitive loads
- Fixed reverse breakdown voltages of 1.225, 2.500V, 4.096V, 5.000V, 8.192V, and 10.000V
- Adjustable reverse breakdown version
- Contact Micrel for parts with extended temperature range.

Key Specifications

- Output voltage tolerance (A grade, 25°C) ...±0.1% (max)
- Low output noise (10Hz to 100Hz)
  - LM4040 ..... $35\mu V_{RMS}$ (typ)
  - LM4041 ..... $20\mu V_{RMS}$ (typ)
- Wide operating current range
  - LM4040 ..... 60μA to 15mA
  - LM4041 ..... 60μA to 12mA
- Industrial temperature range ..... –40°C to +85°C
- Low temperature coefficient ..... 100ppm/°C (max)

Applications

- Battery-Powered Equipment
- Data Acquisition Systems
- Instrumentation
- Process Control
- Energy Management
- Product Testing
- Automotive Electronics
- Precision Audio Components

Typical Applications

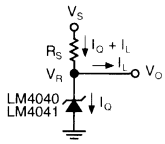


Figure 1. LM4040, LM4041 Fixed Shunt Regulator Application

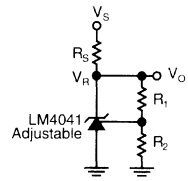


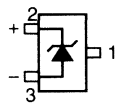
Figure 2. LM4041 Adjustable Shunt Regulator Application

Recommended Parts* (Ordering Information)

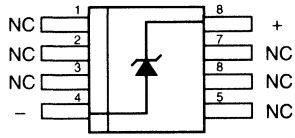
LM4040CIM-2.5	***2.500V, ±0.5%***	**LM4040DIM-5.0**	***5.000V, ±1.0%***	**LM4041CIM3-1.2 T&R†**	***1.225V, ±0.5%***
LM4040DIM-2.5	***2.500V, ±1.0%***	**LM4040DIM3-5.0 T&R†**	***5.000V, ±1.0%***	**LM4041DIM3-1.2 T&R†**	***1.225V, ±1.0%***
LM4040CIM3-2.5 T&R†	***2.500V, ±0.5%***	**LM4040DIZ-5.0**	***5.000V, ±1.0%***	**LM4041DIZ-1.2**	***1.225V, ±1.0%***
LM4040DIM3-2.5 T&R†	***2.500V, ±1.0%***			**LM4041CIM3-ADJ T&R†**	***1.24–10V, ±0.5%***
LM4040CIZ-2.5	***2.500V, ±0.5%***			**LM4041DIM3-ADJ T&R†**	***1.24–10V, ±1.0%***
LM4040DIZ-2.5	***2.500V, ±1.0%***			**LM4041DIZ-ADJ**	***1.24–10V, ±1.0%***

*Contact factory for availability of other part numbers. †M3 (SOT-23) package available in Tape & Reel only.

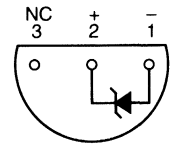
Pin Configuration



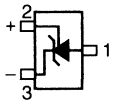
Fixed Version
SOT-23 (M3) Package
Top View



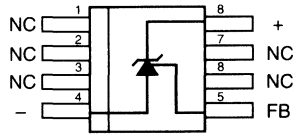
Fixed Version
SO-8 (M) Package
Top View



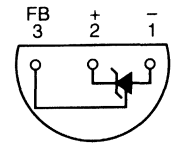
Fixed Version
TO-92 (Z) Package
Bottom View



Adjustable Version
SOT-23 (M3) Package
Top View



Adjustable Version
SO-8 (M) Package
Top View



Adjustable Version
TO-92 (Z) Package
Bottom View

Ordering Information‡ (Expanded Version)

Part Number	Voltage	Accuracy, Temp. Coefficient
LM4040AI*-2.5	2.500V	±0.1%, 100ppm/°C
LM4040BI*-2.5	2.500V	±0.2%, 100ppm/°C
LM4040CI*-2.5	2.500V	±0.5%, 100ppm/°C
LM4040DI*-2.5	2.500V	±1.0%, 150ppm/°C
LM4040EI*-2.5†	2.500V	±2.0%, 150ppm/°C
LM4040AI*-4.1	4.096V	±0.1%, 100ppm/°C
LM4040BI*-4.1	4.096V	±0.2%, 100ppm/°C
LM4040CI*-4.1	4.096V	±0.5%, 100ppm/°C
LM4040DI*-4.1	4.096V	±1.0%, 150ppm/°C
LM4040AI*-5.0	5.000V	±0.1%, 100ppm/°C
LM4040BI*-5.0	5.000V	±0.2%, 100ppm/°C
LM4040CI*-5.0	5.000V	±0.5%, 100ppm/°C
LM4040DI*-5.0	5.000V	±1.0%, 150ppm/°C
LM4040AI*-8.2	8.192V	±0.1%, 100ppm/°C
LM4040BI*-8.2	8.192V	±0.2%, 100ppm/°C
LM4040CI*-8.2	8.192V	±0.5%, 100ppm/°C
LM4040DI*-8.2	8.192V	±1.0%, 150ppm/°C
LM4040AI*-10.0	10.00V	±0.1%, 100ppm/°C
LM4040BI*-10.0	10.00V	±0.2%, 100ppm/°C
LM4040CI*-10.0	10.00V	±0.5%, 100ppm/°C
LM4040DI*-10.0	10.00V	±1.0%, 150ppm/°C
LM4041AI*-1.2	1.225V	±0.1%, 100ppm/°C
LM4041BI*-1.2	1.225V	±0.2%, 100ppm/°C
LM4041CI*-1.2	1.225V	±0.5%, 100ppm/°C
LM4041DI*-1.2	1.225V	±1.0%, 150ppm/°C
LM4041EI*-1.2†	1.225V	±2.0%, 150ppm/°C
LM4041CI*-ADJ	1.24V to 10V	±0.5%, 100ppm/°C
LM4041DI*-ADJ	1.24V to 10V	±1.0%, 150ppm/°C

Refer to **Recommended Parts** list for most common part numbers.
Contact factory for availability of other part numbers.

* M = SO-8, M3 = SOT-23, Z = TO-92

† available only in M3 and Z packages

‡ **M3 (SOT-23) available in Tape and Reel only. Add suffix "T&R". Quantity = 3000/reel.**

SOT-23 Package Markings (Example: R4A)

Example	Field	Code
R _ _	1st Character	R = Reference

Explanation: The SOT-23 package size does not allow conventional part number markings, therefore a 3-character coding system is used for identification. See note for 3rd character.

Example: R4A represents *Reference, 4.096V, ±0.1%* (LM4040AIM3-4.1)

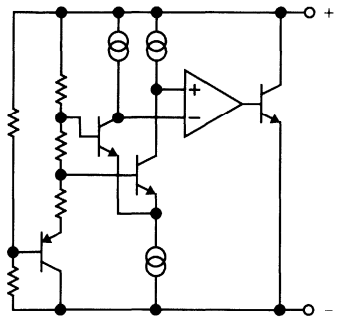
Example	Field	Code
_ 4 _	2nd Character	1 = 1.225V 2 = 2.500V 4 = 4.096V 5 = 5.000V 8 = 8.192V 10 = 10.00V A = Adjustable

Example	Field	Code
_ _ A	3rd Character	A = ±0.1% B = ±0.2% C = ±0.5% D = ±1.0% E = ±2.0%

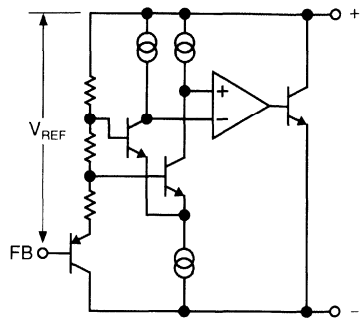
Note: If 3rd character is omitted, container will indicate tolerance.

11

Functional Diagram
LM4040, LM4041 Fixed



Functional Diagram
LM4041 Adjustable



Absolute Maximum Ratings

Reverse Current 20mA
Forward Current 10mA
Maximum Output Voltage
  LM4041-Adjustable 15V
Power Dissipation (T_A = 25°C) (Note 2)
  M Package 540mW
  M3 Package 306mW
  Z Package 550mW
Storage Temperature ..... –65°C to +150°C
Lead Temperature
  M and M3 Packages
    Vapor phase (60 seconds) ..... +215°C
    Infrared (15 seconds) ..... +220°C
  Z Package
    Soldering (10 seconds) ..... +260°C
ESD Susceptibility
    Human Body Model (Note 3) 2kV
    Machine Model (Note 3) 200V

Operating Ratings (Notes 1 & 2)

Temperature Range
  ($T_{MIN} \le T_A \le T_{MAX}$) ..... $-40°C \le T_A \le +85°C$
Reverse Current
  LM4040-2.5 ..... 60µA to 15mA
  LM4040-4.1 ..... 68µA to 15mA
  LM4040-5.0 ..... 74µA to 15mA
  LM4040-8.2 ..... 91µA to 15mA
  LM4040-10.0 ..... 100µA to 15mA
  LM4041-1.2 ..... 60µA to 12mA
  LM4041-ADJ ..... 60µA to 12mA
Output Voltage Range
  LM4041-ADJ ..... 1.24V to 10V

LM4040 and LM4041 Applications Information

The LM4040 and LM4041 have been designed for stable operation without the need of an external capacitor connected between the (+) and (–) pins. If a bypass capacitor is used, the references remain stable.

SOT-23 Versions

LM4040-x.x and LM4041-1.2s in the SOT-23 packages have a parasitic Schottky diode between pin 3 (–) and pin 1 (die attach interface connect). Pin 1 of the SOT-23 package must float or be connected to pin 3. LM4041-ADJs use pin 1 as the (–) output.

Conventional Shunt Regulator

In a conventional shunt regulator application (see Figure 1), an external series resistor (R_S) is connected between the supply voltage and the LM4040-x.x or LM4041-1.2 reference. R_S determines the current that flows through the load (I_L) and the reference (I_Q). Since load current and supply voltage may vary, R_S should be small enough to supply at least the minimum acceptable I_Q to the reference even when the supply voltage is at its minimum and the load current is at its

(continued following LM4041 typical characteristics)

LM4040-2.5 Electrical Characteristics

Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$. The grades A, B, C, D, and E designate initial Reverse Breakdown Voltage tolerance of ±0.1%, ±0.2%, ±0.5%, ± 1.0%, and ±2.0 respectively.

Symbol	Parameter	Conditions	Typical (Note 4)	LM4040AIM LM4040AIM3 LM4040AIZ Limits (Note 5)	LM4040BIM LM4040BIM3 LM4040BIZ Limits (Note 5)	LM4040CIM LM4040CIM3 LM4040CIZ Limits (Note 5)	Units (Limit)
V_R	Reverse Breakdown Voltage	I_R = 100µA	2.500				V
	Reverse Breakdown Voltage Tolerance	I_R = 100µA		±2.5 **±19**	±5.0 **±21**	±12 **±29**	mV (max) mV (max)
I_{RMIN}	Minimum Operating Current		45	 60 **65**	 60 **65**	 60 **65**	µA µA (max) µA (max)
$\Delta V_R/\Delta T$	Average Reverse Breakdown Voltage Temperature Coefficient	I_R = 10mA I_R = 1mA I_R = 100µA	20 15 15	 **100**	 **100**	 **100**	ppm/°C ppm/°C (max) ppm/°C (max)
$\Delta V_R/\Delta I_R$	Reverse Breakdown Voltage Change with Operating Current Change	$I_{RMIN} \le I_R$ 1mA	0.3	 0.8 **1.0**	 0.8 **1.0**	 0.8 **1.0**	mV mV (max) mV (max)
		1mA ≤ I_R 15mA	2.5	 0.6 **8.0**	 0.6 **8.0**	 0.6 **8.0**	mV mV (max) mV (max)
Z_R	Reverse Dynamic Impedance	I_R = 1mA, f = 120Hz $I_{AC} = 0.1\ I_R$	0.3	 0.8	 0.8	 0.9	Ω Ω (max)
e_N	Wideband Noise	I_R = 100µA 10Hz ≤ f ≤ 10kHz	35				μV_{RMS}
ΔV_R	Reverse Breakdown Voltage Long Term Stability	t = 1000hrs T = 25°C ±0.1°C I_R = 100µA	120				ppm

Symbol	Parameter	Conditions	Typical (Note 4)	LM4040DIM LM4040DIM3 LM4040DIZ Limits (Note 5)	LM4040EIM3 LM4040EIZ Limits (Note 5)		Units (Limit)
V_R	Reverse Breakdown Voltage	I_R = 100µA	2.500				V
	Reverse Breakdown Voltage Tolerance	I_R = 100µA		±25 **±49**	±50 **±74**		mV (max) mV (max)
I_{RMIN}	Minimum Operating Current		45	 65 **70**	 65 **70**		µA µA (max) µA (max)
$\Delta V_R/\Delta T$	Average Reverse Breakdown Voltage Temperature Coefficient	I_R = 10mA I_R = 1mA I_R = 100µA	20 15 15	 **150**	 **150**		ppm/°C ppm/°C (max) ppm/°C (max)
$\Delta V_R/\Delta I_R$	Reverse Breakdown Voltage Change with Operating Current Change	$I_{RMIN} \le I_R$ 1mA	0.3	 1.0 **1.2**	 1.0 **1.2**		mV mV (max) mV (max)
		1mA ≤ I_R 15mA	2.5	 8.0 **10.0**	 8.0 **10.0**		mV mV (max) mV (max)
Z_R	Reverse Dynamic Impedance	I_R = 1mA, f = 120Hz $I_{AC} = 0.1\ I_R$	0.3	 1.1	 1.1		Ω Ω (max)
e_N	Wideband Noise	I_R = 100µA 10Hz ≤ f ≤ 10kHz	35				μV_{RMS}
ΔV_R	Reverse Breakdown Voltage Long Term Stability	t = 1000hrs T = 25°C ±0.1°C I_R = 100µA	120				ppm

11

LM4040-4.1 Electrical Characteristics

Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$. The grades A, B, C, and D designate initial Reverse Breakdown Voltage tolerance of ±0.1%, ±0.2%, ±0.5%, and ± 1.0% respectively.

Symbol	Parameter	Conditions	Typical (Note 4)	LM4040AIM LM4040AIM3 LM4040AIZ Limits (Note 5)	LM4040BIM LM4040BIM3 LM4040BIZ Limits (Note 5)	Units (Limit)
V_R	Reverse Breakdown Voltage	I_R = 100µA	4.096			V
	Reverse Breakdown Voltage Tolerance	I_R = 100µA		±4.1 **±31**	±8.2 **±35**	mV (max) mV (max)
I_{RMIN}	Minimum Operating Current		50	 68 **73**	 68 **73**	µA µA (max) µA (max)
$\Delta V_R/\Delta T$	Average Reverse Breakdown Voltage Temperature Coefficient	I_R = 10mA I_R = 1mA I_R = 100µA	30 20 20	 **100**	 **100**	ppm/°C ppm/°C (max) ppm/°C (max)
$\Delta V_R/\Delta I_R$	Reverse Breakdown Voltage Change with Operating Current Change	$I_{RMIN} \le I_R$ 1mA	0.5	 0.9 **1.2**	 0.9 **1.2**	mV mV (max) mV (max)
		1mA ≤ I_R 15mA	3.0	 7.0 **10.0**	 7.0 **10.0**	mV mV (max) mV (max)
Z_R	Reverse Dynamic Impedance	I_R = 1mA, f = 120Hz I_{AC} = 0.1 I_R	0.5	 1.0	 1.0	Ω Ω (max)
e_N	Wideband Noise	I_R = 100µA 10Hz ≤ f ≤ 10kHz	 80			 μV_{RMS}
ΔV_R	Reverse Breakdown Voltage Long Term Stability	t = 1000hrs T = 25°C ±0.1°C I_R = 100µA	120			ppm

Symbol	Parameter	Conditions	Typical (Note 4)	LM4040CIM LM4040CIM3 LM4040CIZ Limits (Note 5)	LM4040DIM LM4040DIM3 LM4040DIZ Limits (Note 5)	Units (Limits)
V_R	Reverse Breakdown Voltage	I_R = 100µA	4.096			V
	Reverse Breakdown Voltage Tolerance	I_R = 100µA		±20 **±47**	±41 **±81**	mV (max) mV (max)
I_{RMIN}	Minimum Operating Current		50	 68 **73**	 73 **78**	µA µA (max) µA (max)
$\Delta V_R/\Delta T$	Average Reverse Breakdown Voltage Temperature Coefficient	I_R = 10mA I_R = 1mA I_R = 100µA	30 20 20	 **100**	 **150**	ppm/°C ppm/°C (max) ppm/°C (max)
$\Delta V_R/\Delta I_R$	Reverse Breakdown Voltage Change with Operating Current Change	$I_{RMIN} \le I_R$ 1mA	0.5	 0.9 **1.2**	 1.2 **1.5**	mV mV (max) mV (max)
		1mA ≤ I_R 15mA	3.0	 7.0 **10.0**	 9.0 **13.0**	mV mV (max) mV (max)
Z_R	Reverse Dynamic Impedance	I_R = 1mA, f = 120Hz I_{AC} = 0.1 I_R	0.5	 1.0	 1.3	Ω Ω (max)
e_N	Wideband Noise	I_R = 100µA 10Hz ≤ f ≤ 10kHz	 80			 μV_{RMS}
ΔV_R	Reverse Breakdown Voltage Long Term Stability	t = 1000hrs T = 25°C ±0.1°C I_R = 100µA	120			ppm

LM4040-5.0 Electrical Characteristics

Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$. The grades A, B, C, and D designate initial Reverse Breakdown Voltage tolerance of ±0.1%, ±0.2%, ±0.5%, and ± 1.0% respectively.

Symbol	Parameter	Conditions	Typical (Note 4)	LM4040AIM LM4040AIM3 LM4040AIZ Limits (Note 5)	LM4040BIM LM4040BIM3 LM4040BIZ Limits (Note 5)	Units (Limit)
V_R	Reverse Breakdown Voltage	I_R = 100µA	5.000			V
	Reverse Breakdown Voltage Tolerance	I_R = 100µA		±5.0 **±38**	±10 **±43**	mV (max) mV (max)
I_{RMIN}	Minimum Operating Current		54	 74 **80**	 74 **80**	µA µA (max) µA (max)
$\Delta V_R/\Delta T$	Average Reverse Breakdown Voltage Temperature Coefficient	I_R = 10mA I_R = 1mA I_R = 100µA	30 20 20	 **100**	 **100**	ppm/°C ppm/°C (max) ppm/°C (max)
$\Delta V_R/\Delta I_R$	Reverse Breakdown Voltage Change with Operating Current Change	$I_{RMIN} \le I_R$ 1mA	0.5	 1.0 **1.4**	 1.0 **1.4**	mV mV (max) mV (max)
		1mA ≤ I_R 15mA	3.5	 8.0 **12.0**	 8.0 **12.0**	mV mV (max) mV (max)
Z_R	Reverse Dynamic Impedance	I_R = 1mA, f = 120Hz $I_{AC} = 0.1\ I_R$	0.5	 1.1	 1.1	Ω Ω (max)
e_N	Wideband Noise	I_R = 100µA 10Hz ≤ f ≤ 10kHz	 80			 μV_{RMS}
ΔV_R	Reverse Breakdown Voltage Long Term Stability	t = 1000hrs T = 25°C ±0.1°C I_R = 100µA	40			ppm

Symbol	Parameter	Conditions	Typical (Note 4)	LM4040CIM LM4040CIM3 LM4040CIZ Limits (Note 5)	LM4040DIM LM4040DIM3 LM4040DIZ Limits (Note 5)	Units (Limits)
V_R	Reverse Breakdown Voltage	I_R = 100µA	5.000			V
	Reverse Breakdown Voltage Tolerance	I_R = 100µA		±25 **±58**	±50 **±99**	mV (max) mV (max)
I_{RMIN}	Minimum Operating Current		54	 74 **80**	 79 **85**	µA µA (max) µA (max)
$\Delta V_R/\Delta T$	Average Reverse Breakdown Voltage Temperature Coefficient	I_R = 10mA I_R = 1mA I_R = 100µA	30 20 20	 **100**	 **150**	ppm/°C ppm/°C (max) ppm/°C (max)
$\Delta V_R/\Delta I_R$	Reverse Breakdown Voltage Change with Operating Current Change	$I_{RMIN} \le I_R$ 1mA	0.5	 1.0 **1.3**	 1.3 **1.8**	mV mV (max) mV (max)
		1mA ≤ I_R 15mA	3.5	 8.0 **12.0**	 10.0 **15.0**	mV mV (max) mV (max)
Z_R	Reverse Dynamic Impedance	I_R = 1mA, f = 120Hz $I_{AC} = 0.1\ I_R$	0.5	 1.1	 1.5	Ω Ω (max)
e_N	Wideband Noise	I_R = 100µA 10Hz ≤ f ≤ 10kHz	 80			 μV_{RMS}
ΔV_R	Reverse Breakdown Voltage Long Term Stability	t = 1000hrs T = 25°C ±0.1°C I_R = 100µA	120			ppm

11

LM4040-8.2 Electrical Characteristics

Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$. The grades A, B, C, and D designate initial Reverse Breakdown Voltage tolerance of ±0.1%, ±0.2%, ±0.5%, and ± 1.0% respectively.

Symbol	Parameter	Conditions	Typical (Note 4)	LM4040AIM LM4040AIM3 LM4040AIZ Limits (Note 5)	LM4040BIM LM4040BIM3 LM4040BIZ Limits (Note 5)	Units (Limit)
V_R	Reverse Breakdown Voltage	I_R = 150µA	8.192			V
	Reverse Breakdown Voltage Tolerance	I_R = 150µA		±8.2 **±61**	±16 **±70**	mV (max) mV (max)
I_{RMIN}	Minimum Operating Current		67	 91 **95**	 91 **95**	µA µA (max) µA (max)
$\Delta V_R/\Delta T$	Average Reverse Breakdown Voltage Temperature Coefficient	I_R = 10mA I_R = 1mA I_R = 150µA	40 20 20	**100**	**100**	ppm/°C ppm/°C (max) ppm/°C (max)
$\Delta V_R/\Delta I_R$	Reverse Breakdown Voltage Change with Operating Current Change	$I_{RMIN} \le I_R$ 1mA	0.6	 1.3 **2.5**	 1.3 **2.5**	mV mV (max) mV (max)
		1mA ≤ I_R 15mA	7.0	 10.0 **18.0**	 10.0 **18.0**	mV mV (max) mV (max)
Z_R	Reverse Dynamic Impedance	I_R = 1mA, f = 120Hz I_{AC} = 0.1 I_R	0.6	1.5	1.5	Ω Ω (max)
e_N	Wideband Noise	I_R = 150µA 10Hz ≤ f ≤ 10kHz	130			μV_{RMS}
ΔV_R	Reverse Breakdown Voltage Long Term Stability	t = 1000hrs T = 25°C ±0.1°C I_R = 150µA	120			ppm

Symbol	Parameter	Conditions	Typical (Note 4)	LM4040CIM LM4040CIM3 LM4040CIZ Limits (Note 5)	LM4040DIM LM4040DIM3 LM4040DIZ Limits (Note 5)	Units (Limits)
V_R	Reverse Breakdown Voltage	I_R = 150µA	8.192			V
	Reverse Breakdown Voltage Tolerance	I_R = 150µA		±41 **±94**	±82 **±162**	mV (max) mV (max)
I_{RMIN}	Minimum Operating Current		67	 91 **95**	 96 **100**	µA µA (max) µA (max)
$\Delta V_R/\Delta T$	Average Reverse Breakdown Voltage Temperature Coefficient	I_R = 10mA I_R = 1mA I_R = 150µA	40 20 20	**100**	**150**	ppm/°C ppm/°C (max) ppm/°C (max)
$\Delta V_R/\Delta I_R$	Reverse Breakdown Voltage Change with Operating Current Change	$I_{RMIN} \le I_R$ 1mA	0.6	 1.3 **2.5**	 1.7 **3.0**	mV mV (max) mV (max)
		1mA ≤ I_R 15mA	7.0	 10.0 **18.0**	 15.0 **24.0**	mV mV (max) mV (max)
Z_R	Reverse Dynamic Impedance	I_R = 1mA, f = 120Hz I_{AC} = 0.1 I_R	0.6	1.5	1.9	Ω Ω (max)
e_N	Wideband Noise	I_R = 150µA 10Hz ≤ f ≤ 10kHz	130			μV_{RMS}
ΔV_R	Reverse Breakdown Voltage Long Term Stability	t = 1000hrs T = 25°C ±0.1°C I_R = 150µA	120			ppm

LM4040-10.0 Electrical Characteristics

Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$. The grades A, B, C, and D designate initial Reverse Breakdown Voltage tolerance of ±0.1%, ±0.2%, ±0.5%, and ± 1.0% respectively.

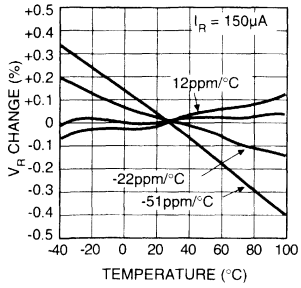
Symbol	Parameter	Conditions	Typical (Note 4)	LM4040AIM LM4040AIM3 LM4040AIZ Limits (Note 5)	LM4040BIM LM4040BIM3 LM4040BIZ Limits (Note 5)	Units (Limit)
V_R	Reverse Breakdown Voltage	I_R = 150µA	10.00			V
	Reverse Breakdown Voltage Tolerance	I_R = 150µA		±10 **±75**	±20 **±85**	mV (max) mV (max)
I_{RMIN}	Minimum Operating Current		75	 100 **103**	 100 **103**	µA µA (max) µA (max)
$\Delta V_R/\Delta T$	Average Reverse Breakdown Voltage Temperature Coefficient	I_R = 10mA I_R = 1mA I_R = 150µA	40 20 20	 **100**	 **100**	ppm/°C ppm/°C (max) ppm/°C (max)
$\Delta V_R/\Delta I_R$	Reverse Breakdown Voltage Change with Operating Current Change	$I_{RMIN} \le I_R$ 1mA	0.8	 1.5 **3.5**	 1.6 **3.5**	mV mV (max) mV (max)
		1mA ≤ I_R 15mA	8.0	 12.0 **23.0**	 12.0 **23.0**	mV mV (max) mV (max)
Z_R	Reverse Dynamic Impedance	I_R = 1mA, f = 120Hz $I_{AC} = 0.1\ I_R$	0.7	 1.7	 1.7	Ω Ω (max)
e_N	Wideband Noise	I_R = 150µA 10Hz ≤ f ≤ 10kHz	 180			 μV_{RMS}
ΔV_R	Reverse Breakdown Voltage Long Term Stability	t = 1000hrs T = 25°C ±0.1°C I_R = 150µA	120			ppm

Symbol	Parameter	Conditions	Typical (Note 4)	LM4040CIM LM4040CIM3 LM4040CIZ Limits (Note 5)	LM4040DIM LM4040DIM3 LM4040DIZ Limits (Note 5)	Units (Limits)
V_R	Reverse Breakdown Voltage	I_R = 150µA	10.00			V
	Reverse Breakdown Voltage Tolerance	I_R = 150µA		±50 **±115**	±100 **±198**	mV (max) mV (max)
I_{RMIN}	Minimum Operating Current		75	 100 **103**	 110 **113**	µA µA (max) µA (max)
$\Delta V_R/\Delta T$	Average Reverse Breakdown Voltage Temperature Coefficient	I_R = 10mA I_R = 1mA I_R = 150µA	40 20 20	 **100**	 **150**	ppm/°C ppm/°C (max) ppm/°C (max)
$\Delta V_R/\Delta I_R$	Reverse Breakdown Voltage Change with Operating Current Change	$I_{RMIN} \le I_R$ 1mA	0.8	 1.5 **3.5**	 2.0 **4.0**	mV mV (max) mV (max)
		1mA ≤ I_R 15mA	8.0	 12.0 **23.0**	 18.0 **29.0**	mV mV (max) mV (max)
Z_R	Reverse Dynamic Impedance	I_R = 1mA, f = 120Hz $I_{AC} = 0.1\ I_R$	0.7	 1.7	 2.3	Ω Ω (max)
e_N	Wideband Noise	I_R = 150µA 10Hz ≤ f ≤ 10kHz	 180			 μV_{RMS}
ΔV_R	Reverse Breakdown Voltage Long Term Stability	t = 1000hrs T = 25°C ±0.1°C I_R = 150µA	120			ppm

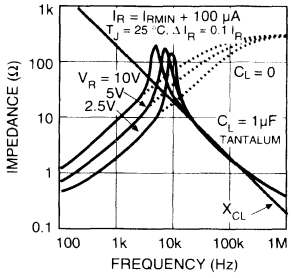
11

LM4040 Typical Characteristics

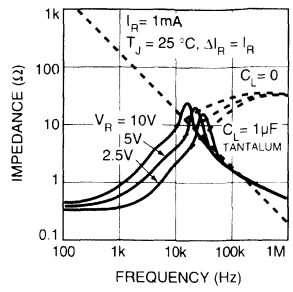
Temperature Drift for Different Average Temperature Coefficient



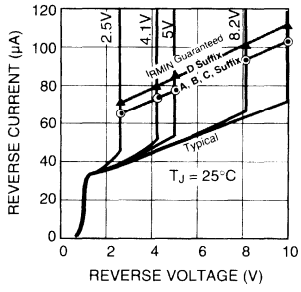
Output Impedance vs. Frequency



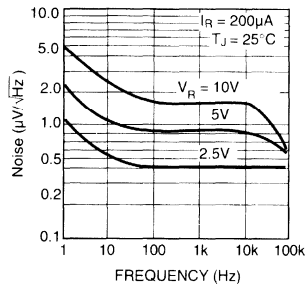
Output Impedance vs. Frequency

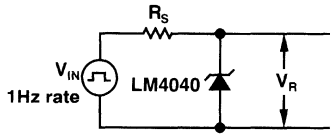


Reverse Characteristics and Minimum Operating Current



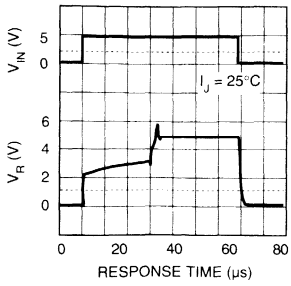
Noise Voltage vs. Frequency



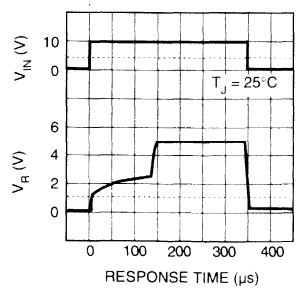


Test Circuit

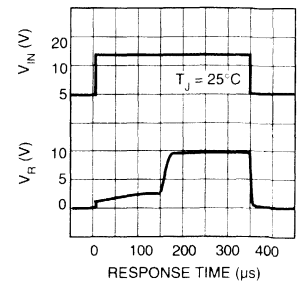
LM4040-2.5 R_S = 30k



LM4040-5.0 R_S = 30k



LM4040-10.0 R_S = 30k



LM4041-1.2 Electrical Characteristics

Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$. The grades A, B, C, D, and E designate initial Reverse Breakdown Voltage tolerance of ±0.1%, ±0.2%, ±0.5%, ± 1.0%, and ±2.0 respectively.

Symbol	Parameter	Conditions	Typical (Note 4)	LM4041AIM LM4041AIM3 LM4041AIZ Limits (Note 5)	LM4041BIM LM4041BIM3 LM4041BIZ Limits (Note 5)	LM4041CIM LM4041CIM3 LM4041CIZ Limits (Note 5)	Units (Limit)
V_R	Reverse Breakdown Voltage	I_R = 100µA	1.225				V
	Reverse Breakdown Voltage Tolerance	I_R = 100µA		±1.2 **±9.2**	±2.4 **±10.4**	±6 **±14**	mV (max) mV (max)
I_{RMIN}	Minimum Operating Current		45	 60 **65**	 60 **65**	 60 **65**	µA µA (max) µA (max)
$\Delta V_R/\Delta T$	Average Reverse Breakdown Voltage Temperature Coefficient	I_R = 10mA I_R = 1mA I_R = 100µA	20 15 15	 **±100**	 **±100**	 **±100**	ppm/°C ppm/°C (max) ppm/°C (max)
$\Delta V_R/\Delta I_R$	Reverse Breakdown Voltage Change with Operating Current Change	$I_{RMIN} \le I_R$ 1mA	0.7	 1.5 **2.0**	 1.5 **2.0**	 1.5 **2.0**	mV mV (max) mV (max)
		1mA ≤ I_R 15mA	4.0	 6.0 **8.0**	 6.0 **8.0**	 6.0 **8.0**	mV mV (max) mV (max)
Z_R	Reverse Dynamic Impedance	I_R = 1mA, f = 120Hz $I_{AC} = 0.1\ I_R$	0.5	 1.5	 1.5	 1.5	Ω Ω (max)
e_N	Wideband Noise	I_R = 100µA 10Hz ≤ f ≤ 10kHz	 20				 μV_{RMS}
ΔV_R	Reverse Breakdown Voltage Long Term Stability	t = 1000hrs T = 25°C ±0.1°C I_R = 100µA	120				ppm

Symbol	Parameter	Conditions	Typical (Note 4)	LM4041DIM LM4041DIM3 LM4041DIZ Limits (Note 5)	LM4041EIM3 LM4041EIZ Limits (Note 5)		Units (Limit)
V_R	Reverse Breakdown Voltage	I_R = 100µA	1.225				V
	Reverse Breakdown Voltage Tolerance	I_R = 100µA		±12 **±24**	±25 **±36**		mV (max) mV (max)
I_{RMIN}	Minimum Operating Current		45	 65 **70**	 65 **70**		µA µA (max) µA (max)
$\Delta V_R/\Delta T$	Average Reverse Breakdown Voltage Temperature Coefficient	I_R = 10mA I_R = 1mA I_R = 100µA	20 15 15	 **±150**	 **±150**		ppm/°C ppm/°C (max) ppm/°C (max)
$\Delta V_R/\Delta I_R$	Reverse Breakdown Voltage Change with Operating Current Change	$I_{RMIN} \le I_R$ 1mA	0.3	 2.0 **2.5**	 2.0 **2.5**		mV mV (max) mV (max)
		1mA ≤ I_R 15mA	2.5	 8.0 **10.0**	 8.0 **10.0**		mV mV (max) mV (max)
Z_R	Reverse Dynamic Impedance	I_R = 1mA, f = 120Hz $I_{AC} = 0.1\ I_R$	0.3	 2.0	 2.0		Ω Ω (max)
e_N	Wideband Noise	I_R = 100µA 10Hz ≤ f ≤ 10kHz	 35				 μV_{RMS}
ΔV_R	Reverse Breakdown Voltage Long Term Stability	t = 1000hrs T = 25°C ±0.1°C I_R = 100µA	120				ppm

11

LM4041-Adjustable Electrical Characteristics

Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_J = 25°C$ unless otherwise specified (SOT-23, see Note 7), $I_{RMIN} \le I_R < 12mA$, $V_{REF} \le V_{OUT} \le 10V$. The grades C and D designate initial Reverse Breakdown Voltage tolerance of ±0.5% and ±1%, respectively for $V_{OUT} = 5V$.

Symbol	Parameter	Conditions	Typical (Note 4)	LM4041CIM LM4041CIM3 LM4041CIZ Limits (Note 5)	LM4041DIM LM4041DIM3 LM4041DIZ Limits (Note 5)	Units (Limit)
V_{REF}	Reference Breakdown Voltage	I_R = 100µA V_{OUT} = 5V	1.233			V
	Reference Breakdown Voltage Tolerance (Note 8)	I_R = 100µA		±6.2 **±14**	±12 **±24**	mV (max) mV (max)
I_{RMIN}	Minimum Operating Current		45	 60 **65**	 65 **70**	µA µA (max) µA (max)
ΔV_{REF} /ΔI_R	Reference Voltage Change with Operating Current Change	$I_{RMIN} \le I_R$ 1mA SOT-23: $V_{OUT} \ge 1.6V$ (Note 7)	0.7	 1.5 **2.0**	 2.0 **2.5**	mV mV (max) mV (max)
		1mA ≤ I_R 15mA SOT-23: $V_{OUT} \ge 1.6V$ (Note 7)	2	 4 **6**	 6 **8**	mV mV (max) mV (max)
ΔV_{REF} /ΔV_O	Reference Voltage Change with Output Voltage Change	I_R = 1mA	−1.3	 −2.0 **−2.5**	 −2.5 **−3.0**	mV/V mV/V (max) mV/V (max)
I_{FB}	Feedback Current		60	 **100** **120**	 **150** **200**	nA nA (max) nA (max)
ΔV_{REF} /ΔT	Average Reference Voltage Temperature Coefficient (Note 8)	V_{OUT} = 5V I_R = 10mA I_R = 1mA I_R = 100µA	 20 15 15	 **±100**	 **±150**	 ppm/°C ppm/°C (max) ppm/°C (max)
Z_{OUT}	Dynamic Output Impedance	I_R = 1mA, f = 120Hz $I_{AC} = 0.1\ I_R$ $V_{OUT} = V_{REF}$ V_{OUT} = 10V	 0.3 2			 Ω Ω (max)
e_N	Wideband Noise	I_R = 100µA 10Hz ≤ f ≤ 10kHz	 20			 μV_{RMS}
ΔV_{REF}	Reference Voltage Long Term Stability	t = 1000hrs T = 25°C ±0.1°C I_R = 100µA	 120			 ppm

LM4040 and LM4041 Electrical Characteristic Notes

Note 1 Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specification and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2 The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX} (maximum junction temperature), θ_{JA} (junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $PD_{MAX} = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For the LM4040 and LM4041, T_{JMAX} = 125°C, and the typical thermal resistance (θ_{JA}), when board mounted, is 185°C/W for the M package, 326°C/W for the SOT-23 package, and 180°C/W with 0.4" lead length and 170°C/W with 0.125" lead length for the TO-92 package.

Note 3 The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin.

Note 4 Typicals are at T_J = 25°C and represent most likely parametric norm.

Note 5 Limits are 100% production tested at 25°C. Limits over temperature are guaranteed through correlation using Statistical Quality Control (SQL) methods.

Note 6 The boldface (over temperature limit for Reverse Breakdown Voltage Tolerance is defined as the room temperature Reverse Breakdown Voltage Tolerance $\pm[(\Delta V_R/\Delta T)(65°C)(V_R)]$. $\Delta V_R/\Delta T$ is the V_R temperature coefficient, 65°C is the temperature range from –40°C to the reference point of 25°C, and V_R is the reverse breakdown voltage. The total over temperature tolerance for the different grades follows:

A-grade: ±0.75% = ±0.1% ±100ppm/°C × 65°C
B-grade: ±0.85% = ±0.2% ±100ppm/°C × 65°C
C-grade: ±1.15% = ±0.5% ±100ppm/°C × 65°C
D-grade: ±1.98% = ±1.0% ±150ppm/°C × 65°C
E-grade: ±2.98% = ±1.0% ±150ppm/°C × 65°C

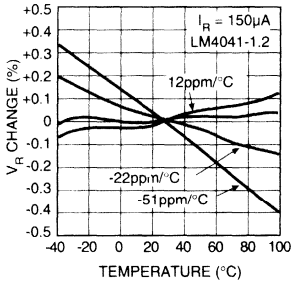
Example: The A-grade LM4040-2.5 has an over temperature Reverse Breakdown Voltage tolerance of ±2.5 × 0.75% = ±19mV.

Note 7 When $V_{OUT} \leq 1.6V$, the LM4041-ADJ in the SOT-23 package must operate at reduced I_R. This is caused by the series resistance of the die attach between the die (–) output and the package (–) output pin. See the Output Saturation (SOT-23 only) curve in the Typical Performance Characteristics section.

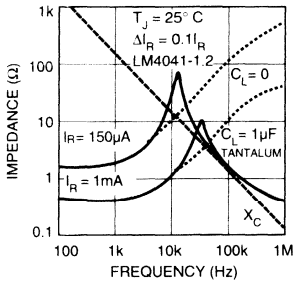
Note 8 Reference voltage and temperature coefficient will change with output voltage. See Typical Performance Characteristics curves.

LM4041 Typical Characteristics

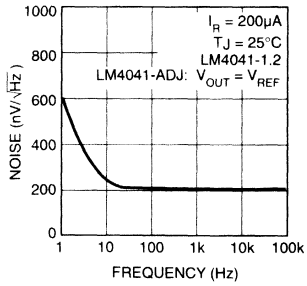
Temperature Drift for Different Average Temperature Coefficient



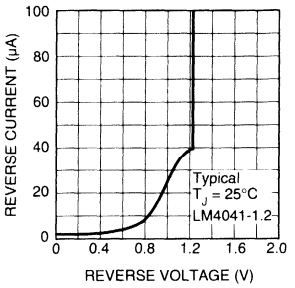
Output Impedence vs. Frequency



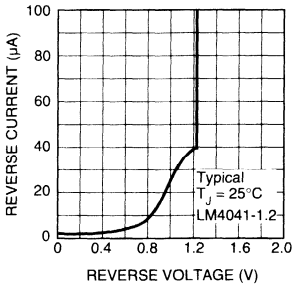
Voltage Impedance

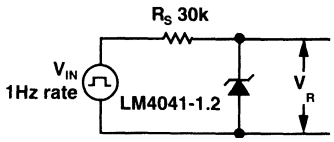


Reverse Characteristics and Minimum Operating Current



Reverse Characteristics and Minimum Operating Current



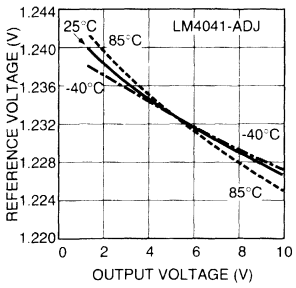


Test Circuit

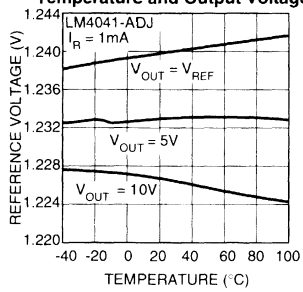
11

LM4041 Typical Characteristics

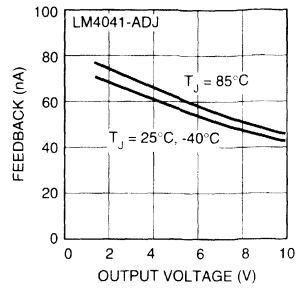
Reference Voltage vs. Output Voltage and Temperature



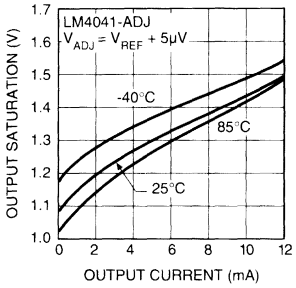
Reference Voltage vs. Temperature and Output Voltage



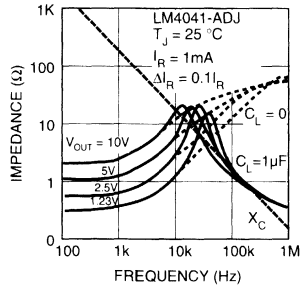
Feedback Current vs. Output Voltage and Temperature



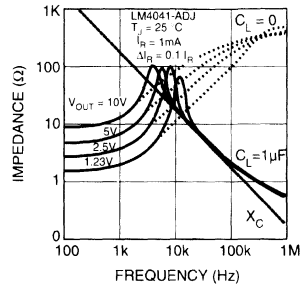
Output Saturation (SOT-23 Only)



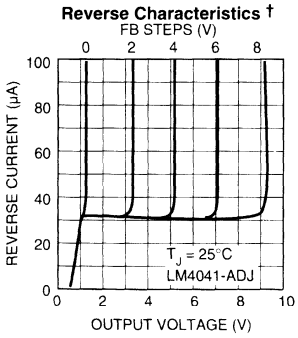
Output Impedence vs. Frequency *

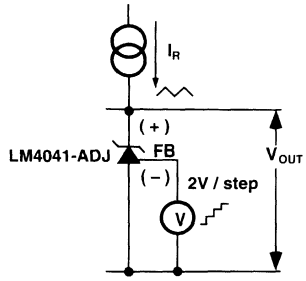


Output Impedence vs. Frequency *

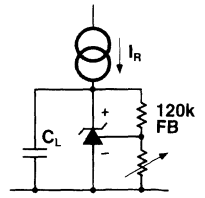


Reverse Characteristics †



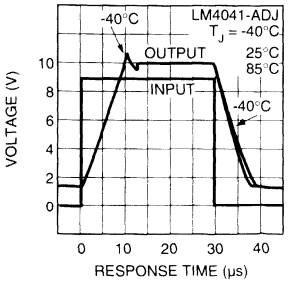


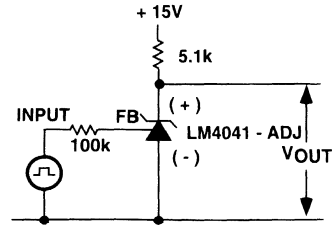
† Reverse Characteristics Test Circuit



*** Output Impedance vs. Freq. Test Circuit**

Large Signal Response †





‡ Large Signal Response Test Circuit

maximum value. When the supply voltage is at its maximum and I_L is at its minimum, R_S should be large enough so that the current flowing through the LM4040-x.x is less than 15mA, and the current flowing through the LM4041-1.2 or LM4041-ADJ is less than 12mA.

R_S is determined by the supply voltage (V_S), the load and operating current, (I_L and I_Q), and the reference's reverse breakdown voltage (V_R).

$$R_s = (V_s - V_R) / (I_L + I_Q)$$

Adjustable Regulator

The LM4041-ADJ's output voltage can be adjusted to any value in the range of 1.24V through 10V. It is a function of the internal reference voltage (V_{REF}) and the ratio of the external feedback resistors as shown in Figure 2. The output is found using the equation

(1) $$V_O = V_{REF}' [(R2/R1) + 1]$$

where V_O is the desired output voltage. The actual value of the internal V_{REF} is a function of V_O. The "corrected" V_{REF} is determined by

(2) $$V_{REF}' = V_O (\Delta V_{REF} / \Delta V_O) = V_Y$$

where V_O is the desired output voltage. $\Delta V_{REF} / \Delta V_O$ is found in the Electrical Characteristics and is typically –1.3mV/V and V_Y is equal to 1.240V. Replace the value of V_{REF}' in equation (1) with the value found using equation (2).

Note that actual output voltage can deviate from that predicted using the typical $\Delta V_{REF} / \Delta V_O$ in equation (2); for C-grade parts, the worst-case $\Delta V_{REF} / \Delta V_O$ is –2.5mV/V and V_Y = 1.248V.

The following example shows the difference in output voltage resulting from the typical and worst case values of $\Delta V_{REF} / \Delta V_O$:

Let V_O = +9V. Using the typical values of $\Delta V_{REF} / \Delta V_O$, V_{REF} is 1.228V. Choosing a value of R1 = 10kΩ, R2 = 63.272kΩ. Using the worst case $\Delta V_{REF} / \Delta V_O$ for the C-grade and D-grade parts, the output voltage is actually 8.965V and 8.946V respectively. This results in possible errors as large as 0.39% for the C-grade parts and 0.59% for the D-grade parts. Once again, resistor values found using the typical value of $\Delta V_{REF} / \Delta V_O$ will work in most cases, requiring no further adjustment.

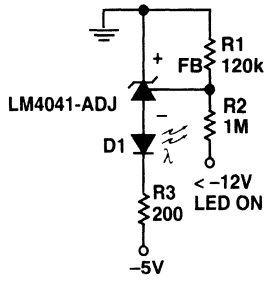


Figure 3. Voltage Level Detector

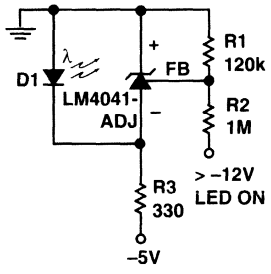


Figure 4. Voltage Level Detector

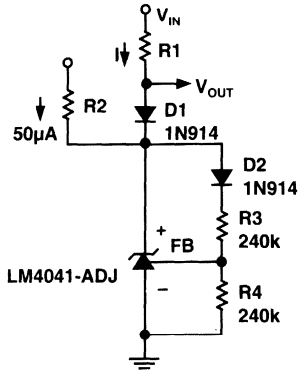


Figure 5. Fast Positive Clamp
2.4V + ΔV_{D1}

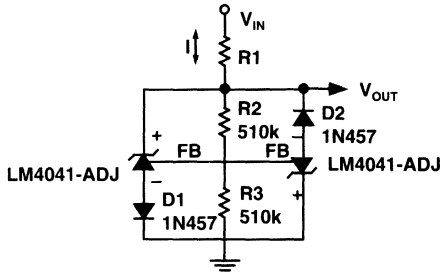


Figure 6. Bidirectional Clamp
±2.4V

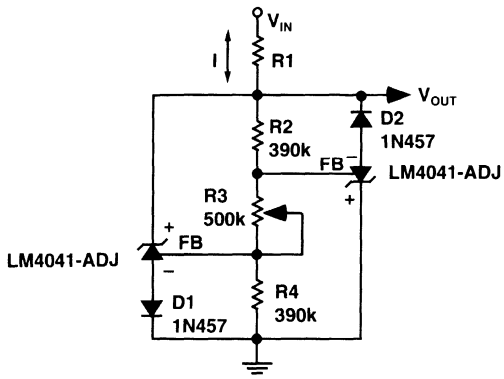


Figure 7. Bidirectional Adjustable Clamp ±18V to ±2.4V

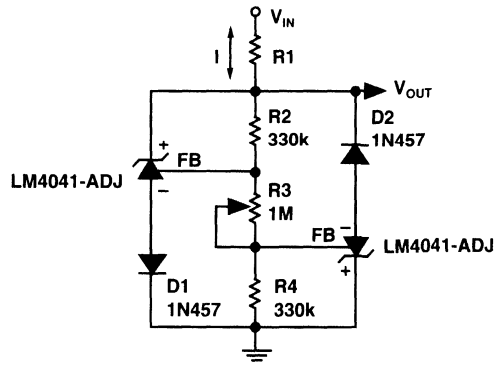


Figure 8. Bidirectional Adjustable Clamp ±2.4 to ±6V

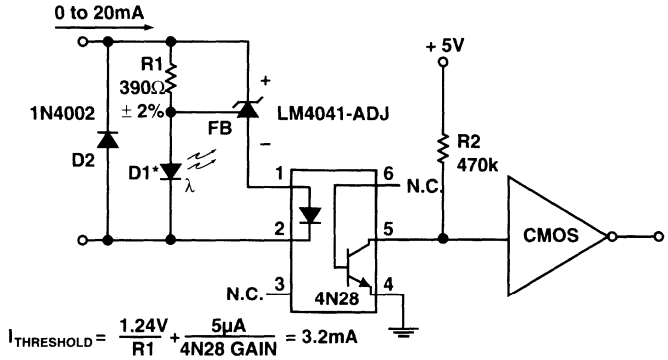


Figure 9. Floating Current Detector

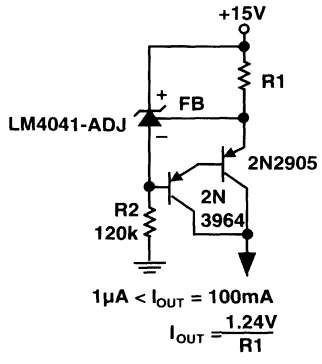


Figure 10. Current Source

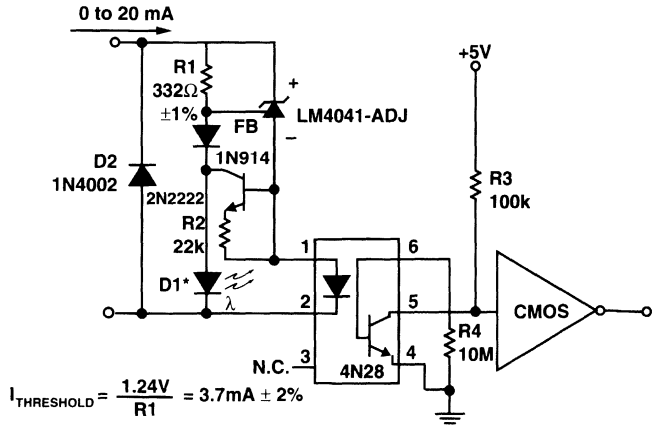


Figure 11. Precision Floating Current Detector

* D1 can be any LED, V_F = 1.5V to 2.2V at 3mA. D1 may act as an indicator. D1 will be on if $I_{THRESHOLD}$ falls below the threshold current, except with I = O.

MIC5009CN

Counter Time-Base Circuit

Summary Information*

General Description

The MIC5009 is a highly versatile MOS oscillator and divider chain manufactured by Micrel using a depletion-load ion-implantation process and P-channel technology. The 16-pin DIP package provides frequency division ranges from 1 to 36 x 10^8. The circuit will operate from any of three frequency sources: the internal oscillator with an external RC combination, the internal oscillator with an external crystal, or with an externally-applied TTL signal. Control inputs provide additional versatility and allow the circuit to be used in a variety of applications including instruments, timers, and clocks.

The MIC5009 consists basically of a series of counters, selectable via an internal multiplexer. The $\div 10^1$ counter output is used to generate an internal clock signal for the 10^2 through 36 x 10^8 counter stages, which are fully synchronous with each other.

With an input frequency of 1MHz, the MIC5009 provides the basic time periods necessary for most frequency measuring instruments, i.e., 1μs through 100 seconds. One-minute, ten-minute, and one-hour periods are also available using a 1MHz input. Using a 1/1.2 MHz input, the MIC5009 can also provide a 50/60Hz output for accurate generation of line frequencies in portable instruments or clocks.

Features

- Ion-implanted for full TTL/DTL compatibility
- Internal clock operates from:
  - External signal
  - External RC network
  - External crystal
- Operates DC to above 1MHz
- Binary-encoded for frequency selection
- Resettable to highest or lowest state
- Twenty different modes of division

Ordering Information

Part Number	Temperature Range	Package
MIC5009CN	0°C to 70°C	16-pin Plastic DIP

Functional Diagram

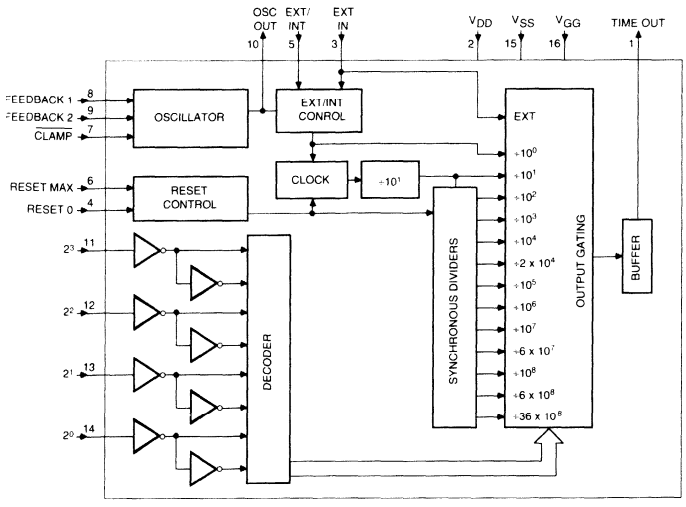
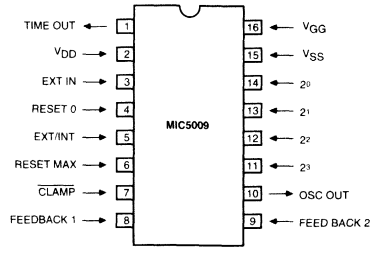


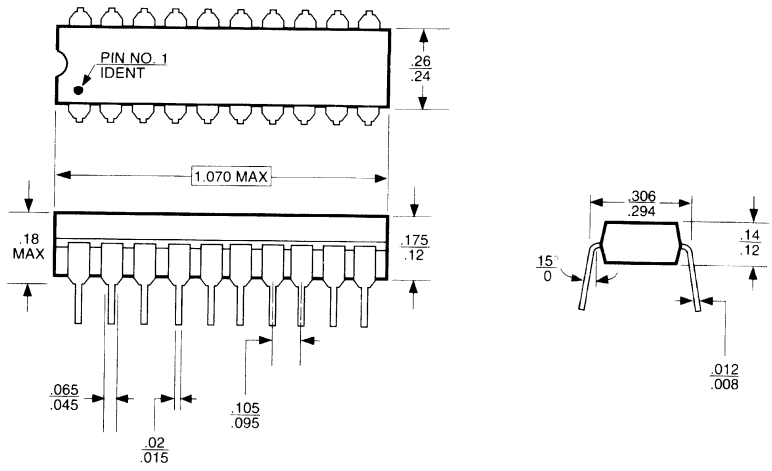
Figure 1

Pin Configuration

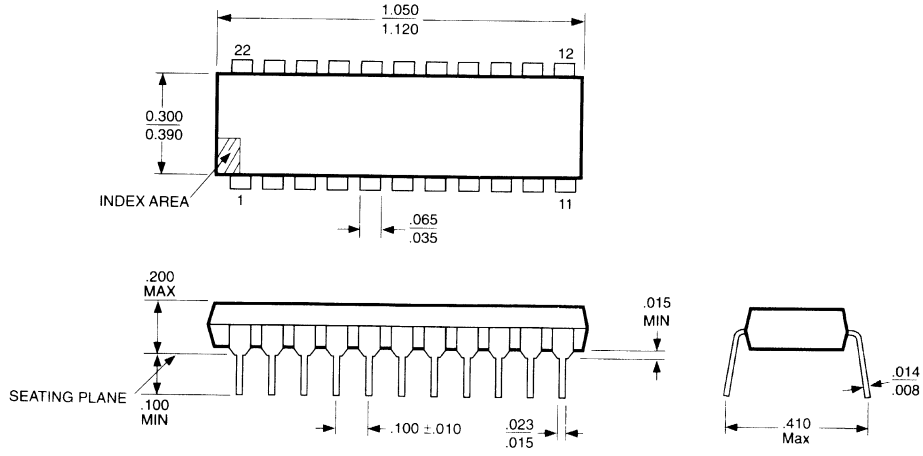


* Contact Micrel for more information.

SECTION 12: PACKAGING INFORMATION

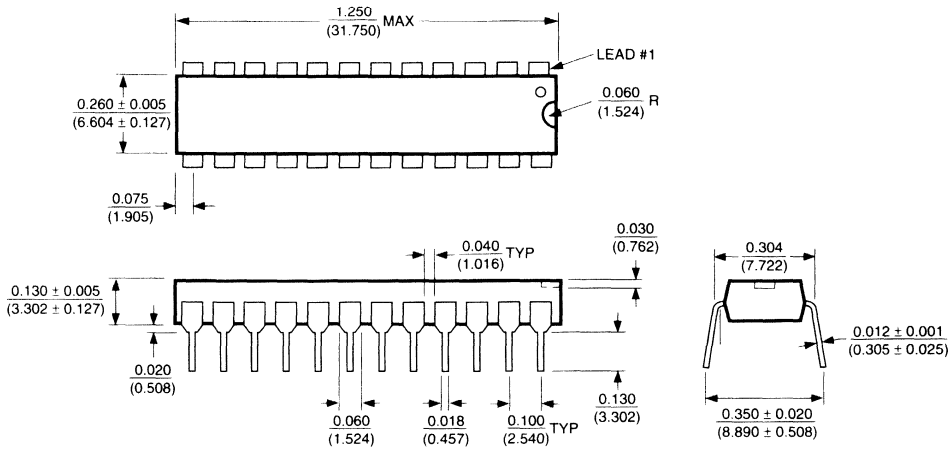


20-pin Plastic DIP (N)

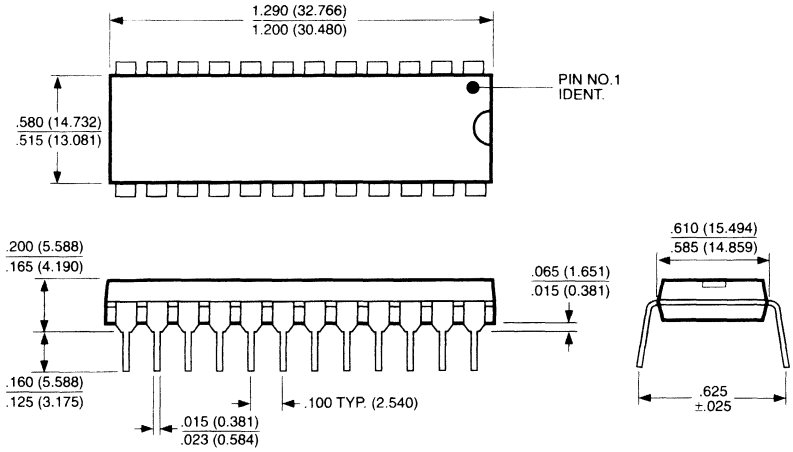


22-pin Plastic DIP (N)

Note: Pin 1 will be denoted by one or more of the following: a notch, a printed triangle, or a mold mark.



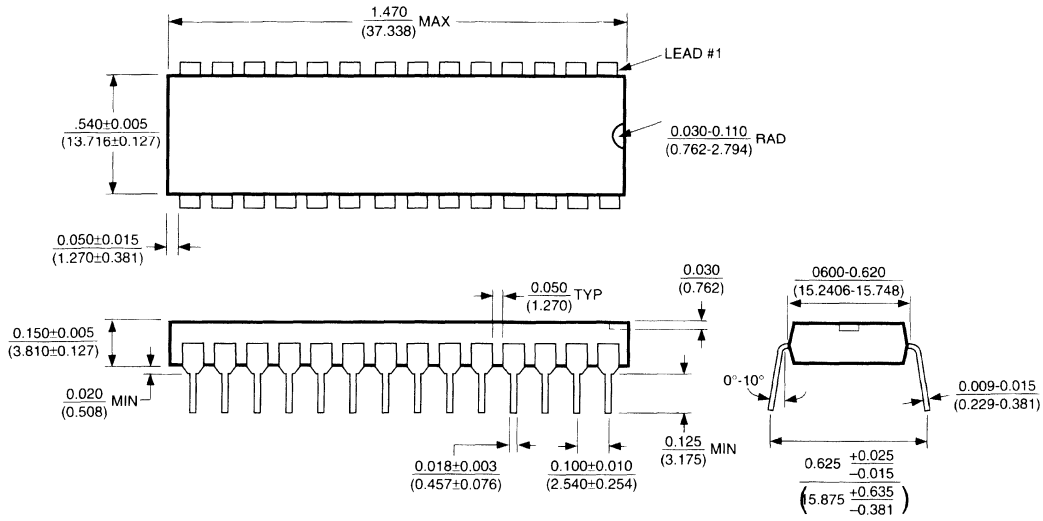
24-pin Plastic Skinny DIP (N)



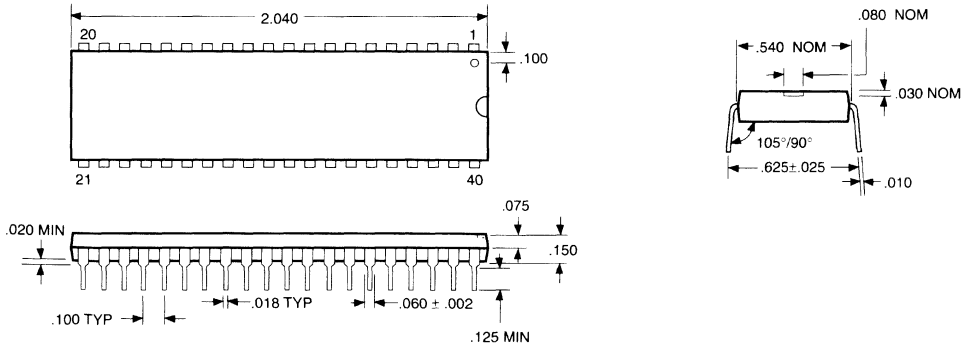
24-pin Plastic DIP (N)

Note: Pin 1 will be denoted by one or more of the following: a notch, a printed triangle, or a mold mark.

12

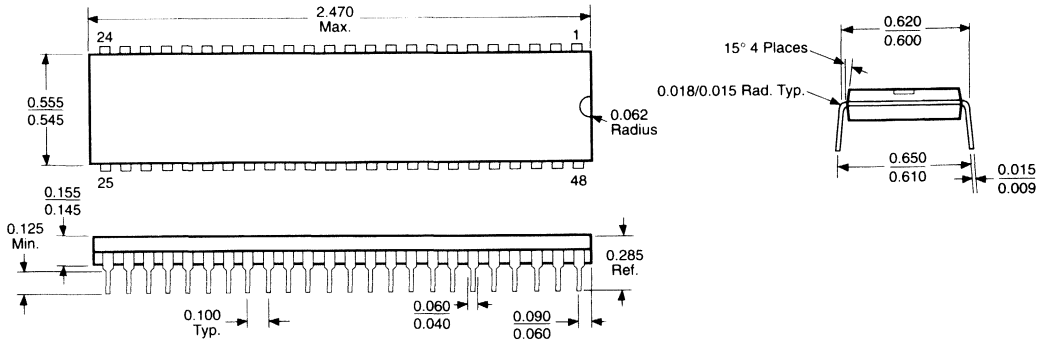


28-pin Plastic DIP (N)



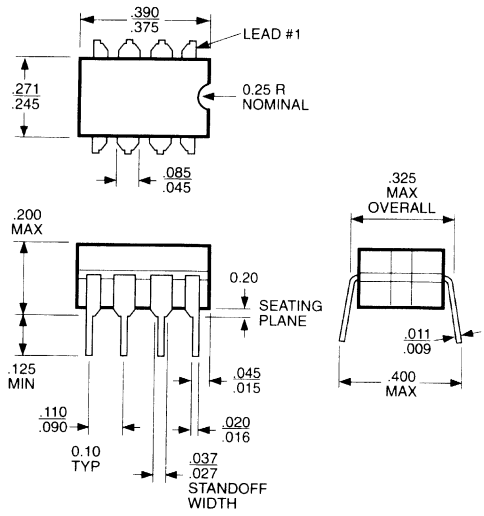
40-pin Plastic DIP (N)

Note: Pin 1 will be denoted by one or more of the following: a notch, a printed triangle, or a mold mark.

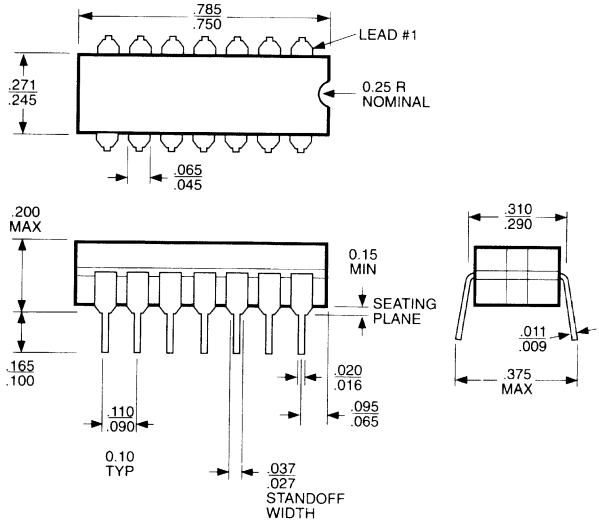


48-pin Plastic DIP (N)

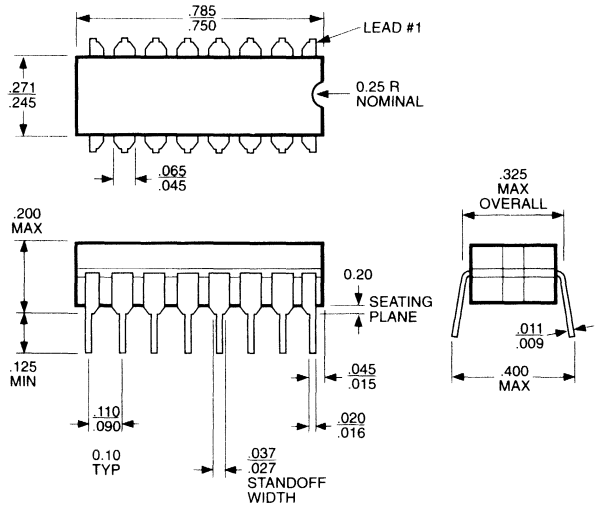
Note: Pin 1 will be denoted by one or more of the following: a notch, a printed triangle, or a mold mark.



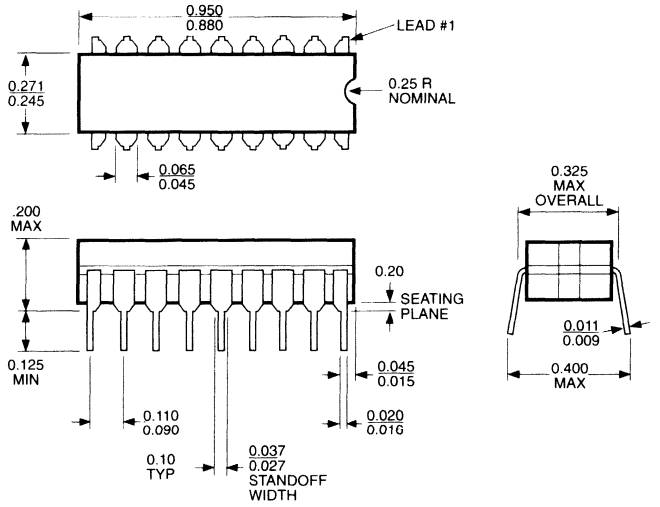
8-pin Ceramic DIP (J)



14-pin Ceramic DIP (J)

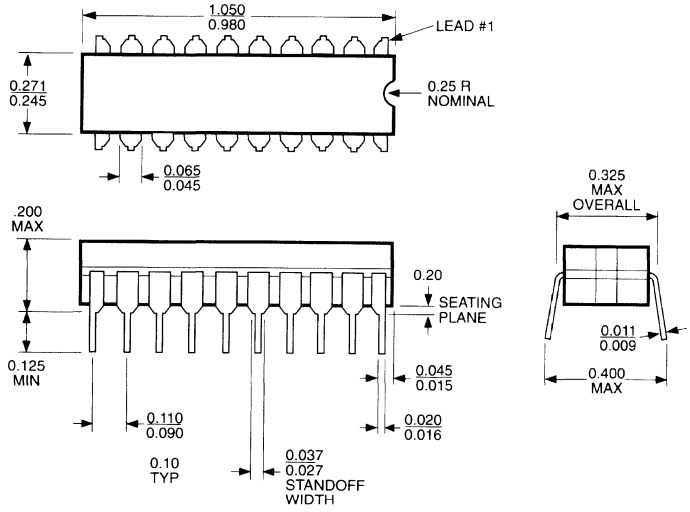


16-pin Ceramic DIP (J)

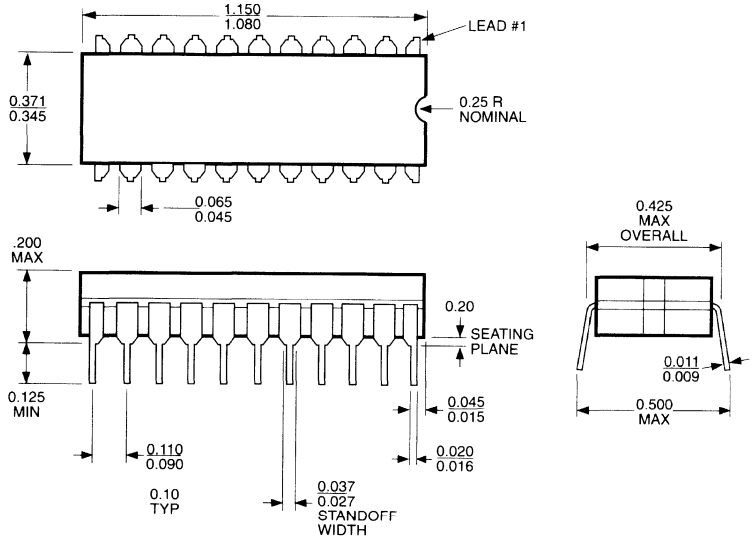


18-pin Ceramic DIP (J)

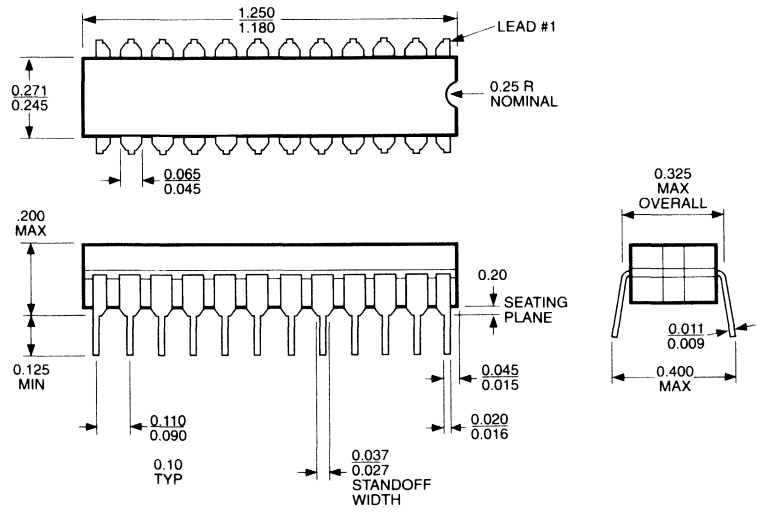
12



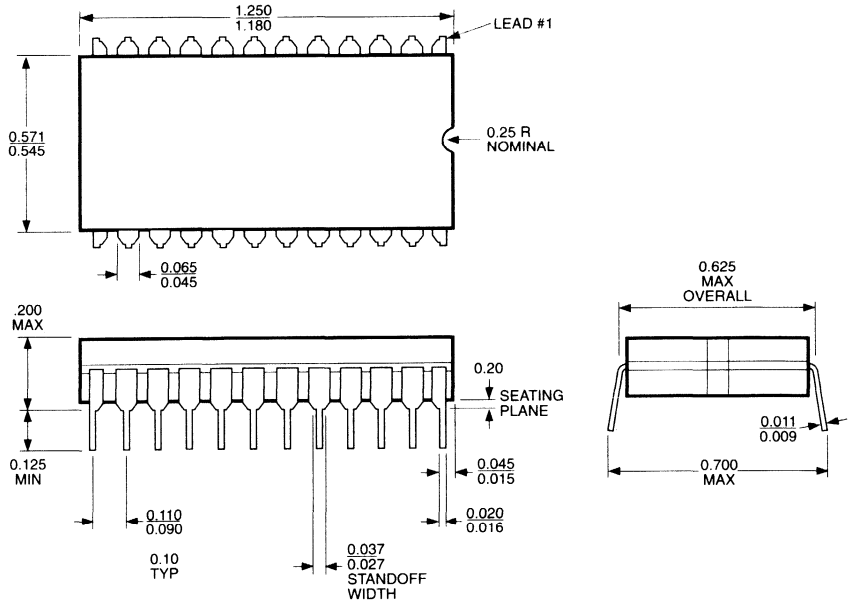
20-pin Ceramic DIP (J)



22-pin Ceramic DIP (J)

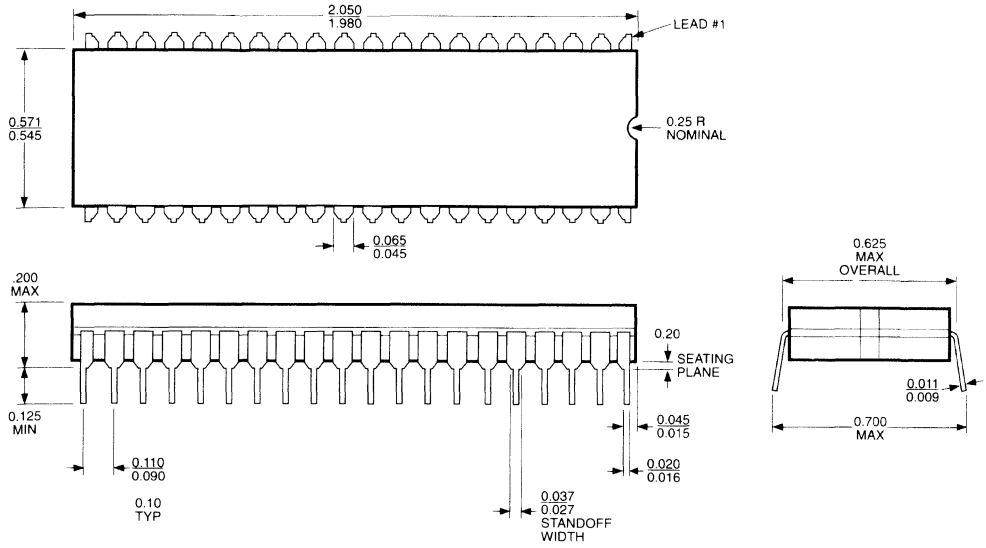


24-pin Ceramic Skinny DIP (J)

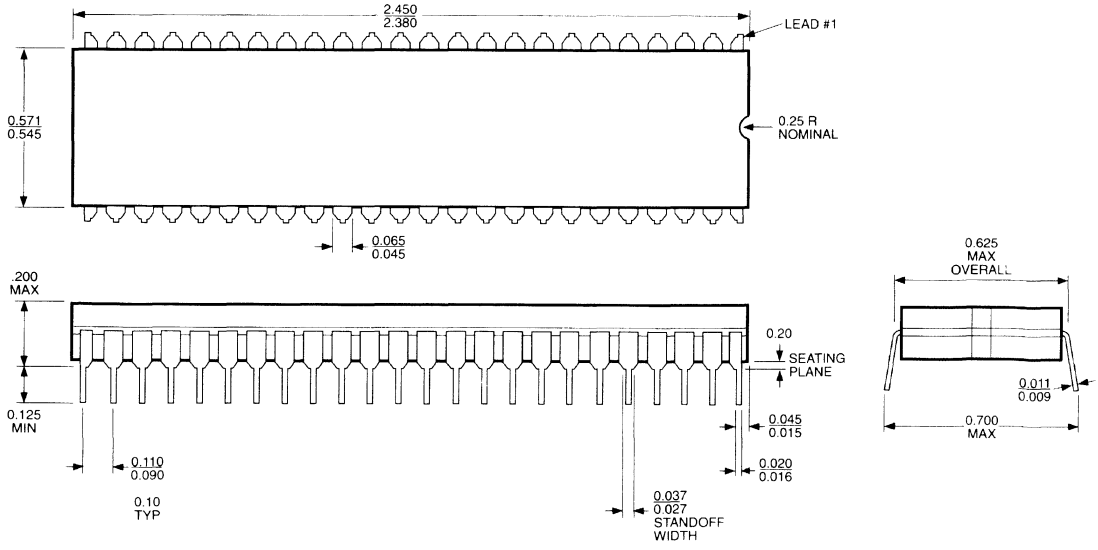


24-pin Ceramic DIP (J)

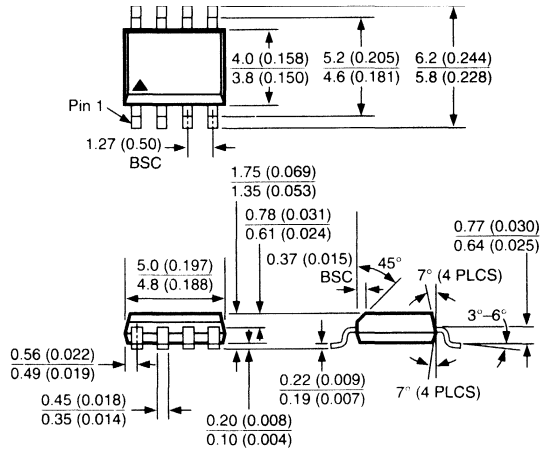
12



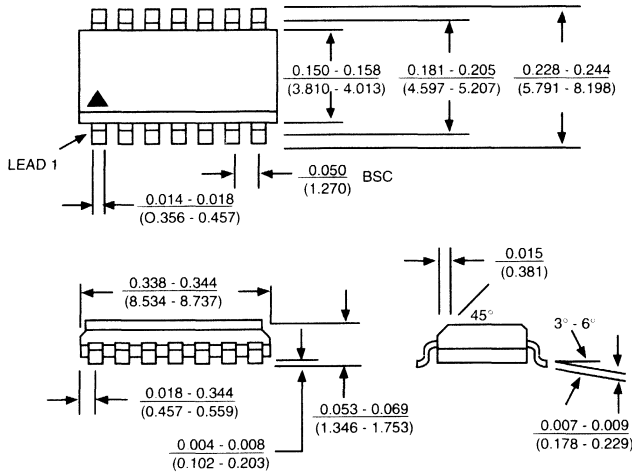
40-pin Ceramic DIP (J)



48-pin Ceramic DIP (J)

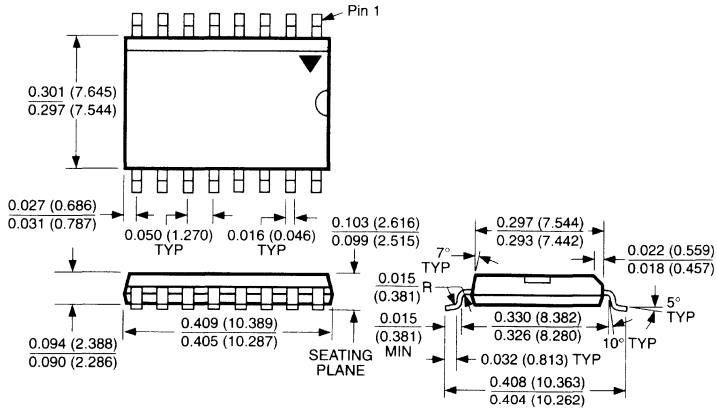


8-pin SOIC (M)

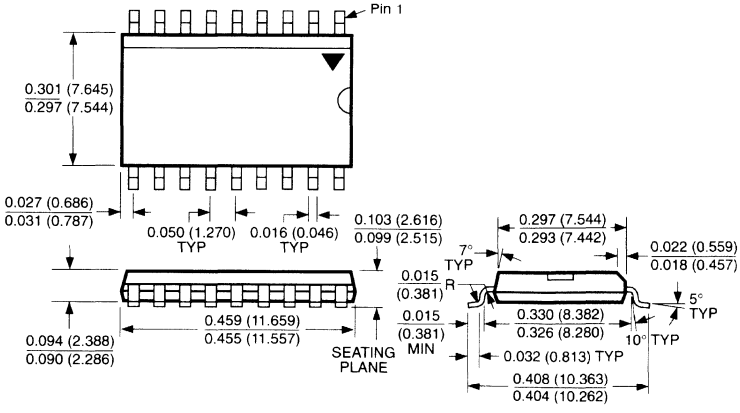


14-pin SOIC (M)

Note: Pin 1 will be denoted by one or more of the following: a notch, a printed triangle, or a mold mark.

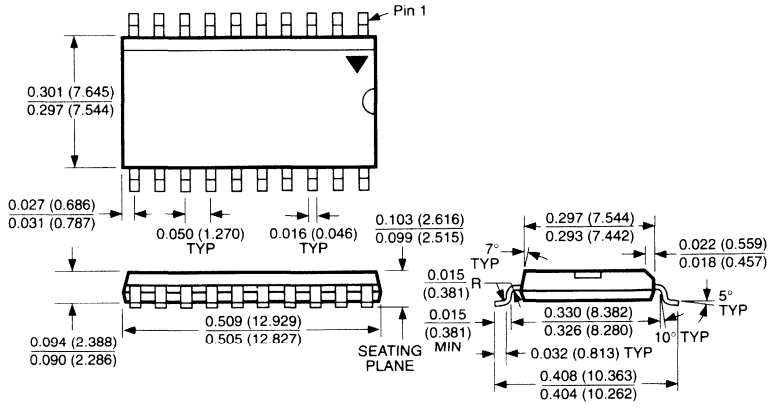


16-pin Wide SOIC (WM)

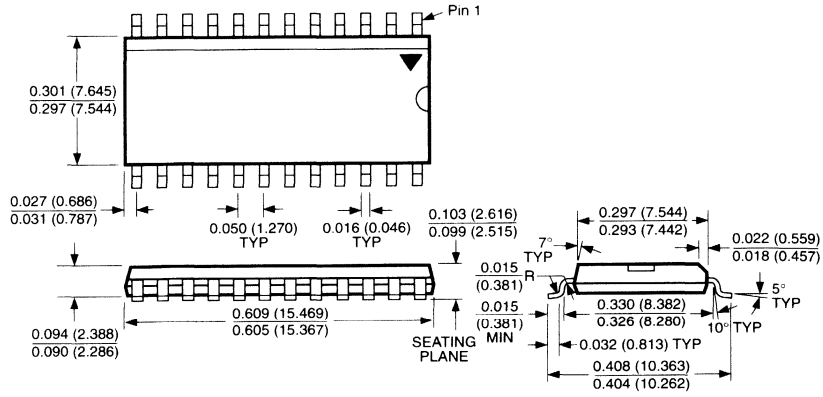


18-pin Wide SOIC (WM)

Note: Pin 1 will be denoted by one or more of the following: a notch, a printed triangle, or a mold mark.

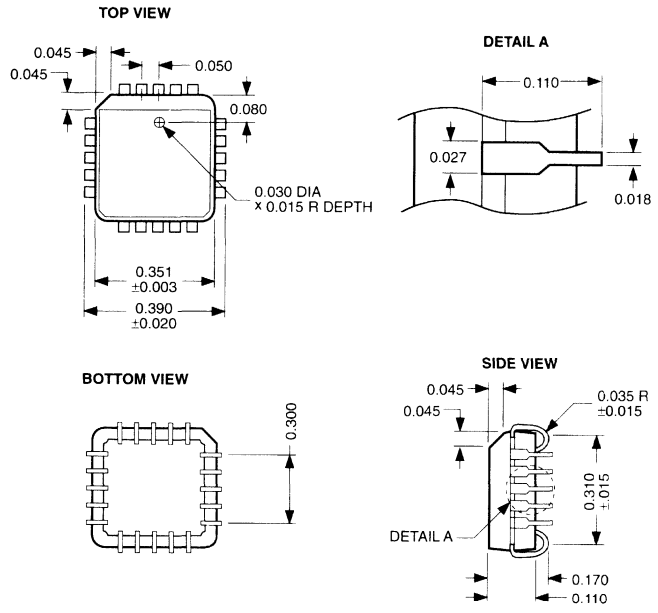


20-pin Wide SOIC (WM)

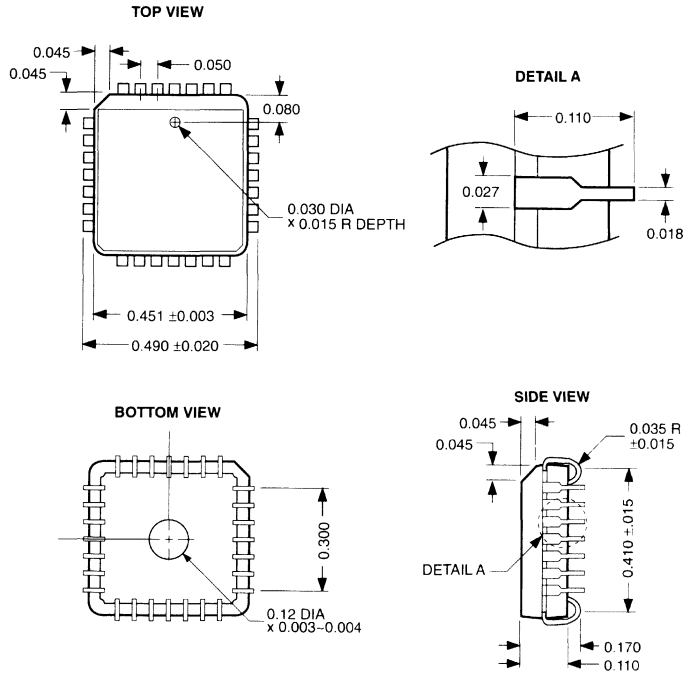


24-pin Wide SOIC (WM)

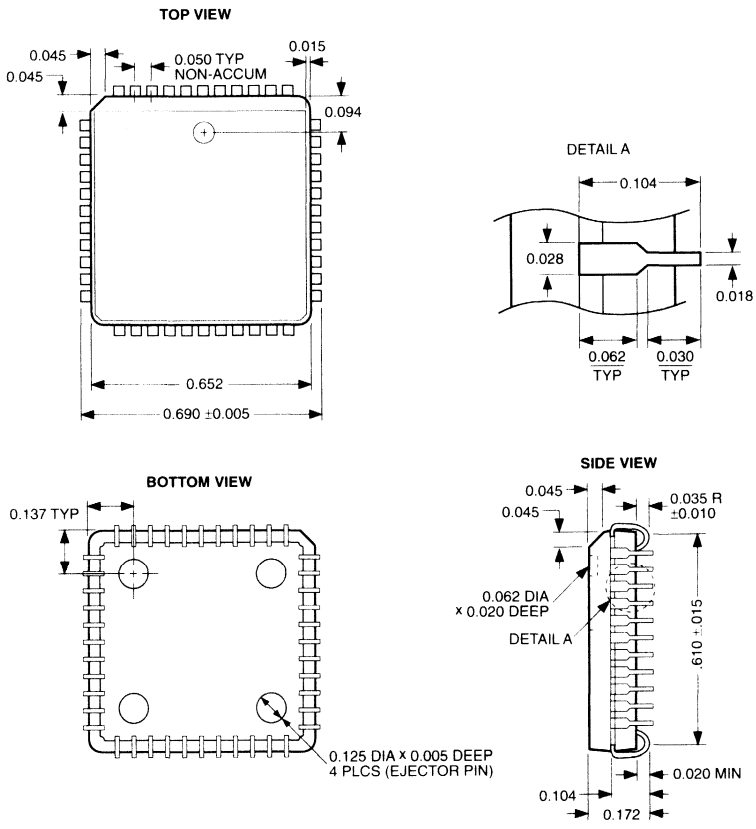
Note: Pin 1 will be denoted by one or more of the following: a notch, a printed triangle, or a mold mark.



20-pin PLCC (V)

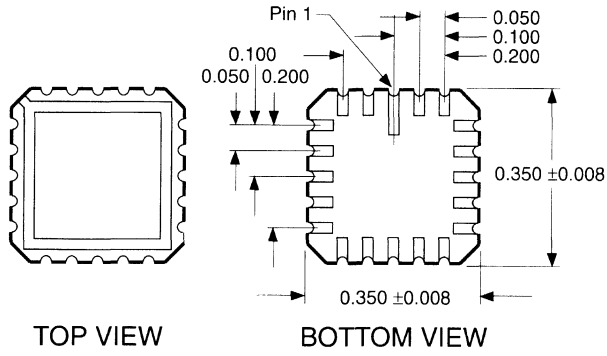


28-pin PLCC (V)

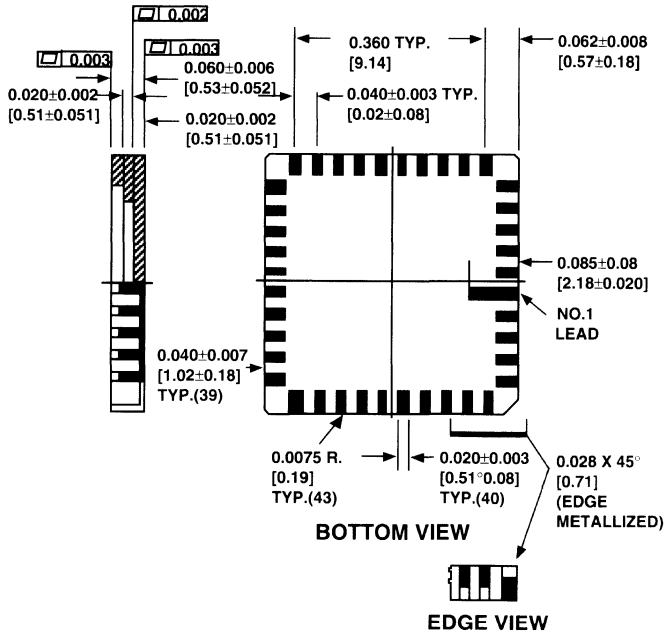


44-pin PLCC (V)

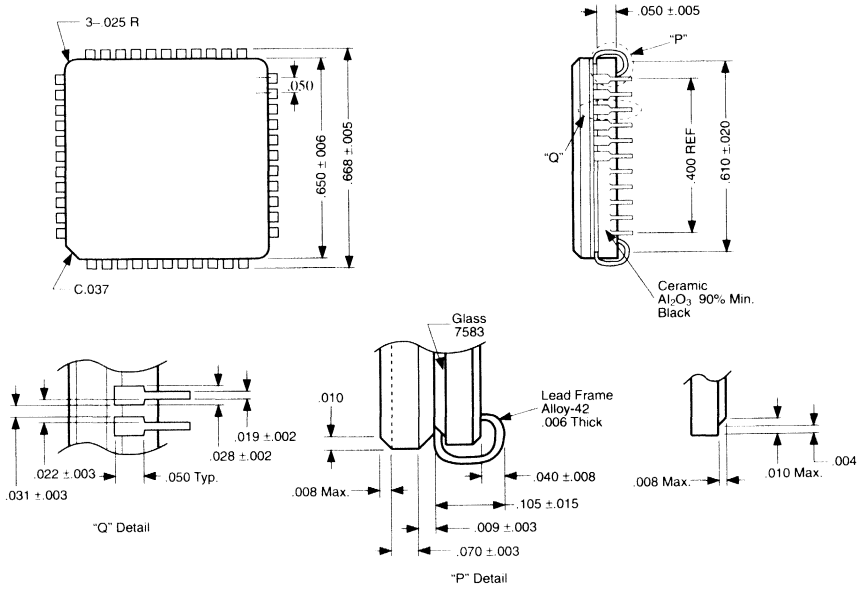
12



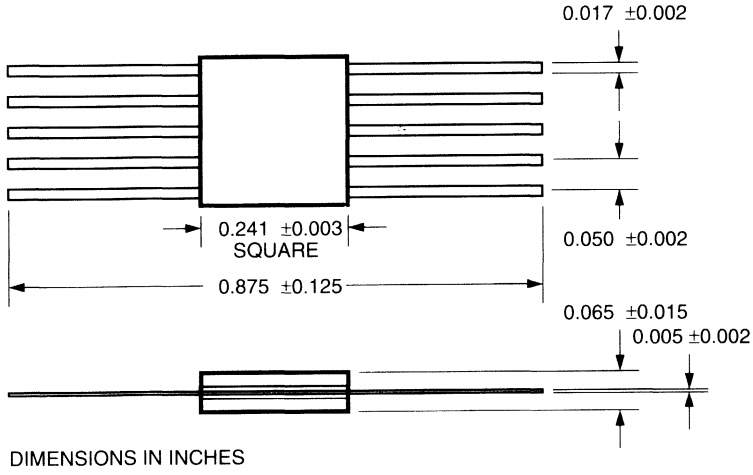
20-lead LCC (L)



40-lead LCC (L)

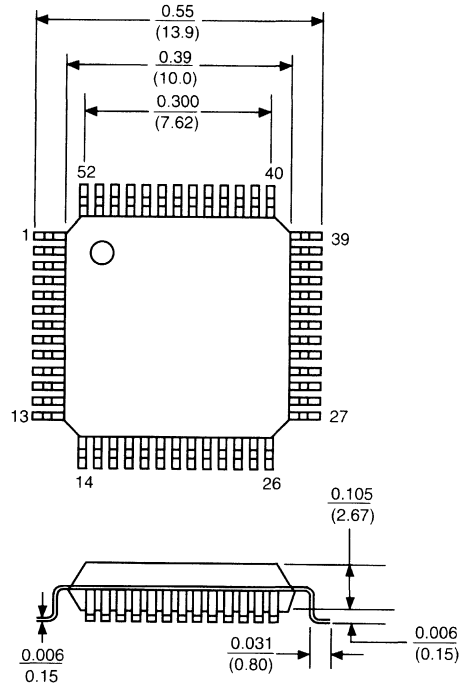


44-pin CerQuad (E)

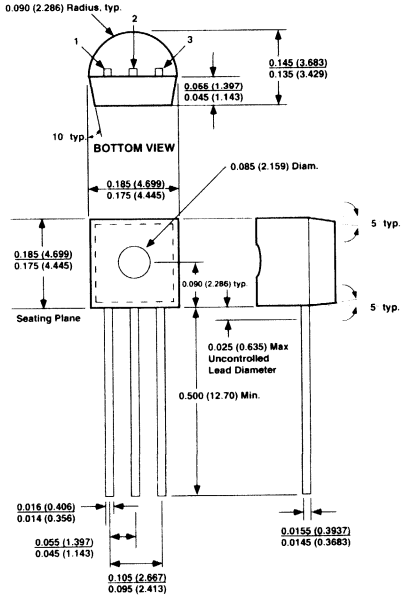


10-pin CerPack(F)

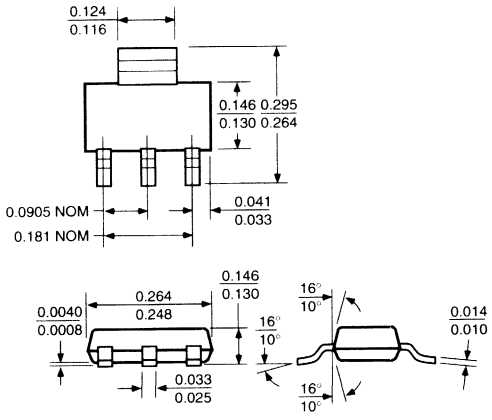
12


0.55
(13.9)
0.39
(10.0)
0.300
(7.62)
52
40
1
39
13
27
14
26
0.105
(2.67)
0.006
(0.15)
0.031
(0.80)
0.006
0.15

52-pin QFP (Q)

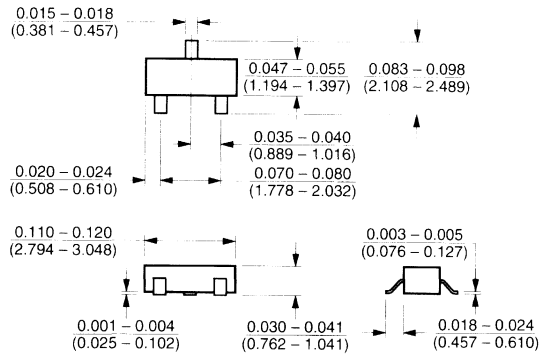


3-lead TO-92 (Z)

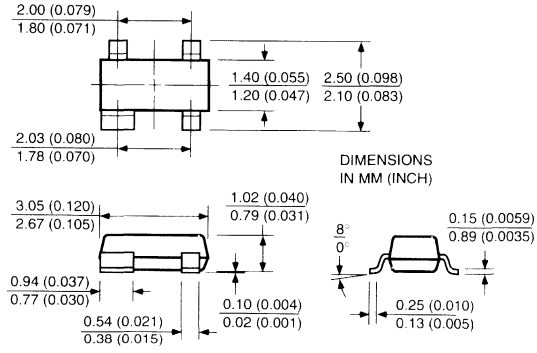


3-lead SOT-223 (S)

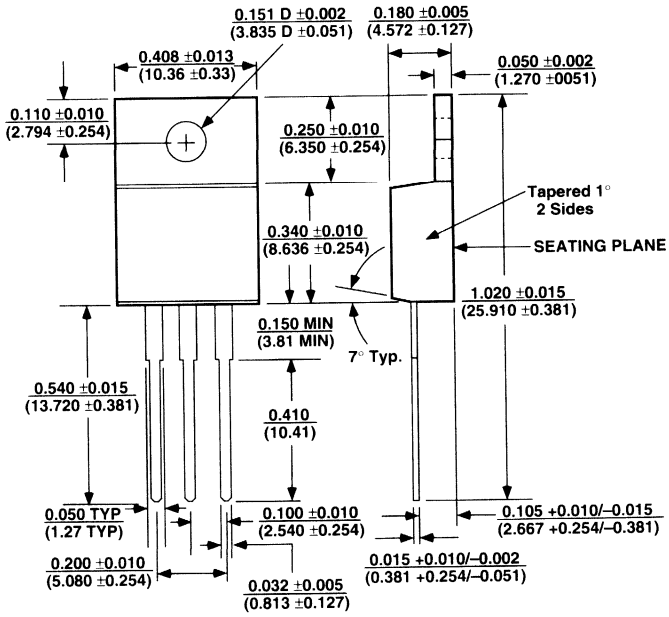
12



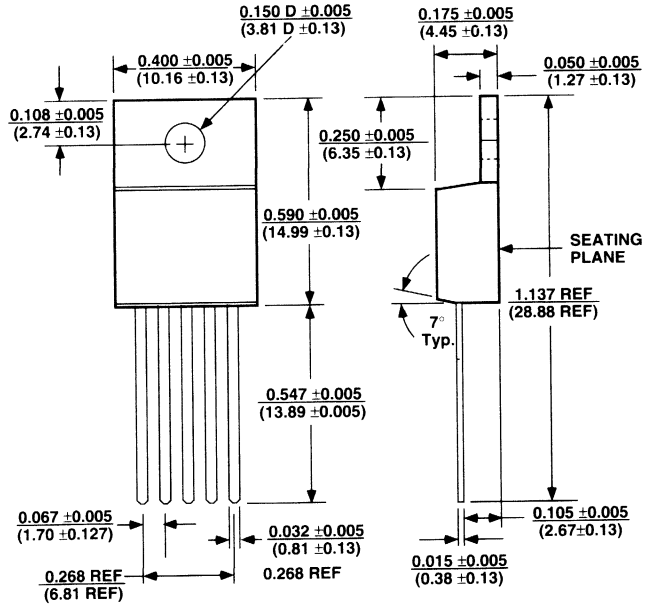
3-lead SOT-23 (M3)



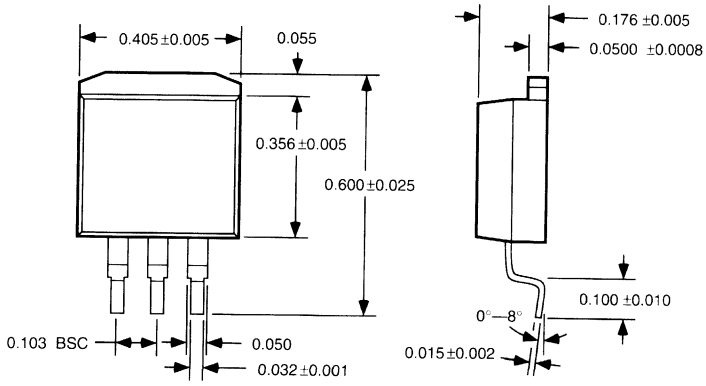
4-lead SOT-143 (M4)



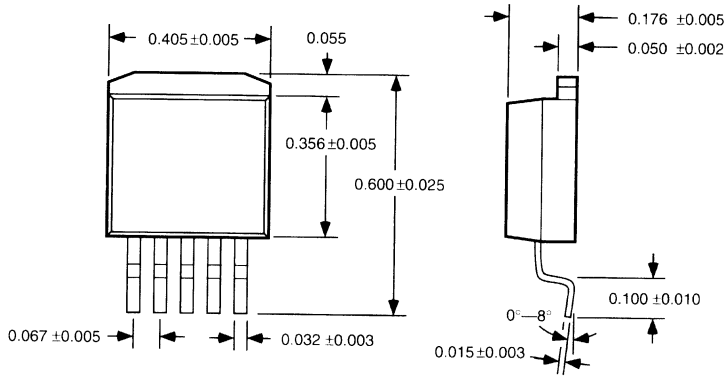
3-lead TO-220 (T)



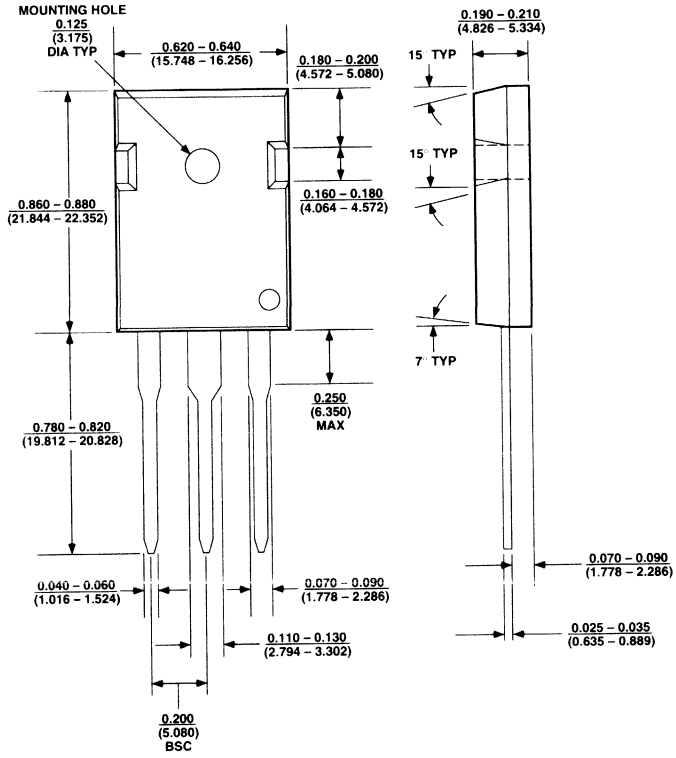
5-lead TO-220 (T)



3-lead TO-263 (U)

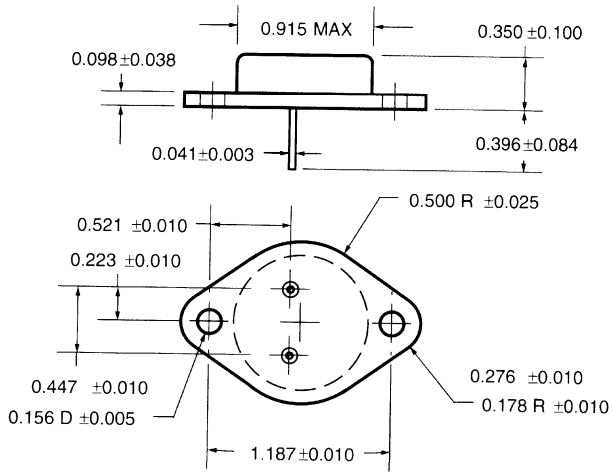


5-lead TO-263 (U)

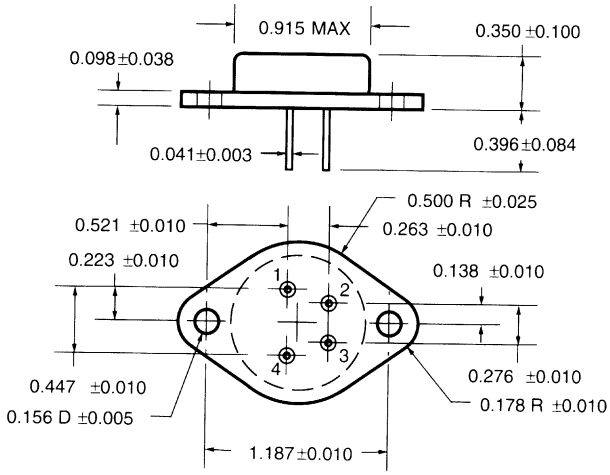


3-lead TO-247 (WT)

12



2-lead TO-3 (K)



4-lead TO-3 (K)

Embossed Tape & Reel

PLCC and SOIC Packages

General Description

SOIC and PLCC packaged devices are now available on tape and reel, allowing simplification of testing and handling which leads to greatly increased throughput! The cover tape also provides protection against moisture or ESD damage during storage and/or shipping.

Although compatibility with most automatic insertion machines is guaranteed by compliance with existing standards, we recommend verification of compatibility prior to placing your order.

Should you have a need for tape and reel shipments of other packages, such as the TO-92, please contact the factory.

Features

- 13mm reels
- Compatible with most automatic lead insertion and/or pick and place machines
- Allows flexible circuit layout
- Conforms to EIA ACP standard RS-468
- Simplifies handling and testing
- Available for PLCC and SOIC packages

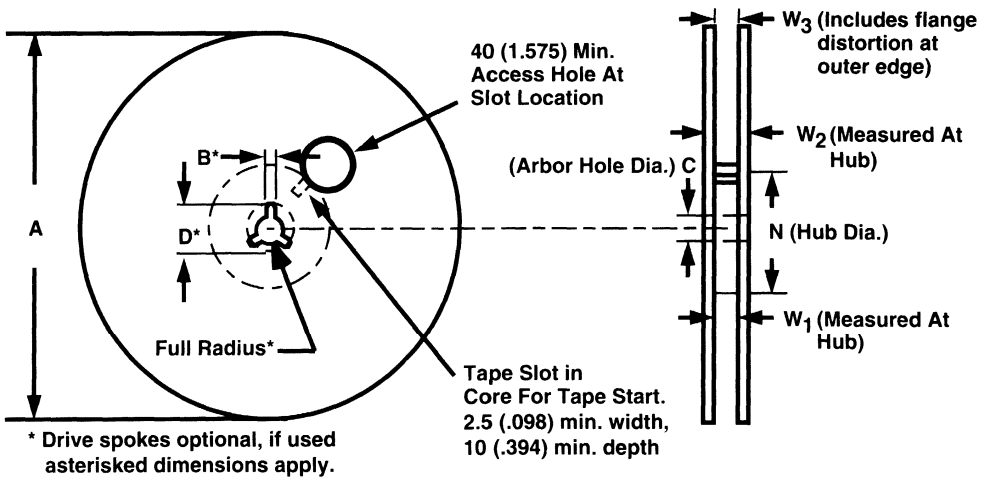
Ordering Information

- When ordering tape and reel option shipment, simply add the suffix "T&R" to the part number Example: MIC5013BMT&R
- Orders MUST be placed in reel quantities, as follows:

Package	Qty/Reel
SOT-23	3,000
SOT-223	3,000
8-pin SOIC	2,500
14-pin SOIC	2,500
16-pin SOIC	2,500
16-pin Wide SOIC	1,000
20-pin PLCC	1,000
24-pin PLCC	1,000
44-pin PLCC	500

Reel Configuration

Metric Dimensions Will Govern. (English given in parentheses)



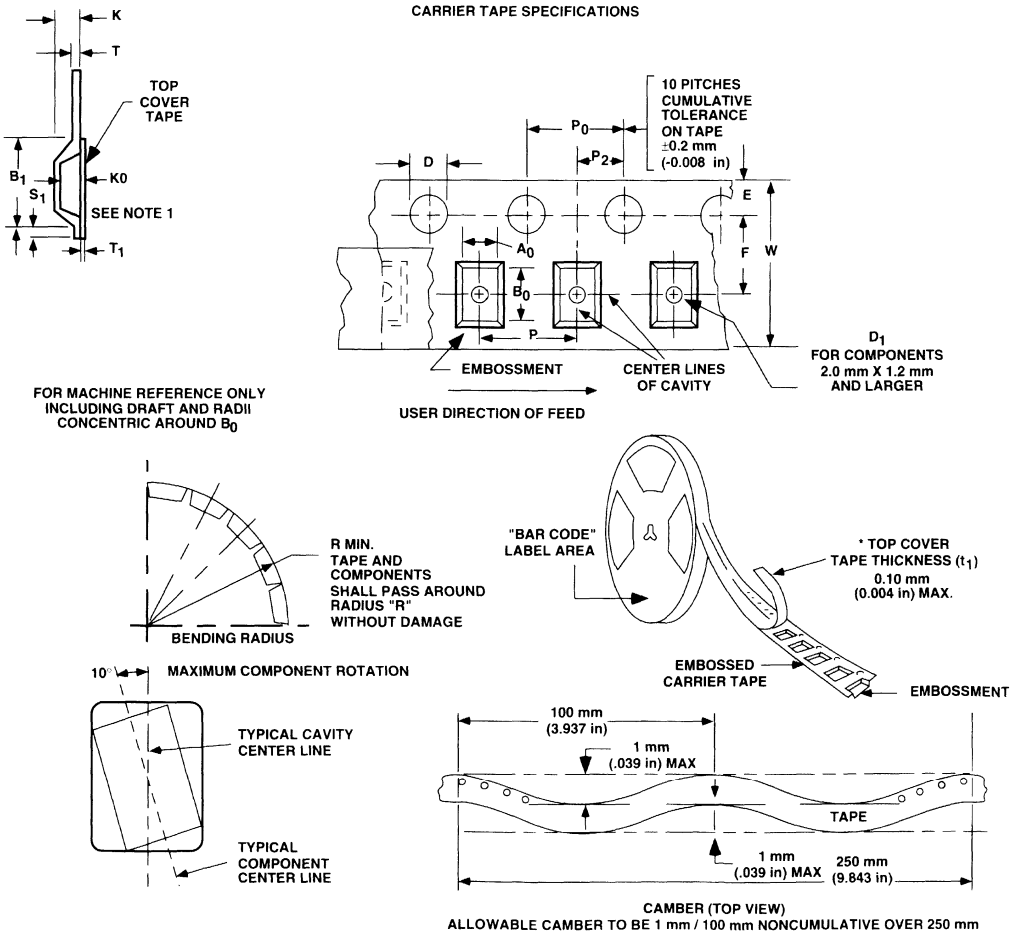
*** Drive spokes optional, if used asterisked dimensions apply.**

12

Reel Dimensions

Tape Size	Corresponding Package	A_{max}	B^*_{min}	C	D^*_{min}	N_{min}	W_1	$W_{2\ max}$	W_3
12mm	8 pin SOIC	330mm (12.992in)	1.5mm (.059in)	13.0±0.20 mm (0.512± .008in)	20.2mm (0.795in)	50mm (1.969in)	12.4+2.0 −0.0mm (.488 +.075 −0.0in)	18.4mm (0.724in)	11.9mm min (0.311in min) 15.4mm max (0.607in max)
16mm	14 pin SOIC 16 pin SOIC 16 pin Wide SOIC 20 pin PLCC	360mm (14.173in)	1.5mm (.059in)	13.0±0.50 −0.2mm (0.512+ .02 −.004in)	20.2mm (0.795in)	50mm (1.969in)	16.4+2.0 −0.0mm (0.646 +.070 −0.20in)	22.4mm (0.882in)	15.9mm min (0.626in min) 19.4mm max (0.764in max)
24mm	22 pin PLCC	360mm (14.173in)	1.5mm (.059in)	13.0±0.50 −0.2mm (0.512+ .02 −.004in)	20.2mm (0.795in)	60mm (2.362in)	24.4+2.0 −0.0mm (0.961 +.070 −0.0in)	30.4mm (1.197in)	23.9mm min (0.941in min) 27.4mm max (1.079in max)
32mm	44 pin PLCC	360mm (14.173in)	1.5mm (.059in)	13.0±0.20 mm (0.512± .008in)	20.2mm (0.795in)	60mm (2.362in)	32.4+2.0 −0.0mm (1.276 +.07 −0.0in)	—	31.9mm min (1.259in min) 35.4mm max (1.394in max)

Tape Specifications



Tape Dimensions

Tape Size	Corresponding Package	D	E	P_0	P_2	T_{max}	T_1	S_1 min	B_1 max	D_1 min	F	P	R_{min}	K	W_{max}
12mm	8 pin SOIC	1.5+0.10 -0.0mm (.059+.004 -0.0in)	1.75±0.10 mm (.069±.004in)	4.0±0.10 mm (0.157±.004in)	2.0±0.05 mm (.079±.002in)	0.60mm (.024in)	0.10mm (.004in) max	0.6mm (.024in)	8.2mm (0.323in)	1.5mm (.059in)	5.5±0.05 mm (0.217±.002in)	4.0±0.10 mm (0.157±.004in) (or in even increments of 4.0mm)	30mm (1.181in)	6.5mm max (.256in max)	12.3mm (0.484in)
16mm	14 pin SOIC 16 pin SOIC 16 pin Wide SOIC 20 pin PLCC	1.5+0.10 -0.0mm (.059+.004 -0.0in)	1.75±0.10 mm (.069± .004in)	4.0±0.10 mm (0.157± .004in)	2.0±0.1 mm (.079± 004in)	0.60mm (.024in)	0.10mm (.004in) max	0.6mm (.024in)	12.1mm (0.476in)	1.5mm (.059in)	7.5±0.1 mm (0.295± 004in)	4.0±0.10 mm (0.157±.004in) (or in even increments of 4.0mm)	30mm (1.181in)	8.0mm max (0.315in)	16.3mm (0.642in)
24mm	22 pin PLCC	1.5+0.10 -0.0mm (.059+.004 -0.0in)	1.75±0.10 mm (.069± 004in)	4.0±0.10 mm (0.157± .004in)	2.0±0.1 mm (.079± 004in)	0.60mm (.024in)	0.10mm (.004in) max	0.6mm (.024in)	20.1mm (0.791in)	1.5mm (.059in)	11.5±0.1 mm (0.453± .004in)	4.0±0.10 mm (0.157±.004in) (or in even increments of 4.0mm)	30mm (1.181in)	12.0mm max (0.472in)	24.3mm (0.957in)
32mm	44 pin PLCC	1.5+0.10 -0.0mm (.059+.004 -0.0in)	1.75±0.10 mm (.069± 004in)	4.0±0.10 mm (0.157± .004in)	2.0±0.1 mm (.079± .004in)	0.60mm (.024in)	0.10mm (.004in) max	--	23.0mm (0.906in)	1.5mm (.059in)	14.2±0.10 mm (0.559± .004in)	4.0±0.10 mm (0.157±.004in) (or in even increments of 4.0mm)	50mm (1.969in)	12.0mm max (0.472in)	32.3 (1.272in)

Note 1: Dimension P is a factor of component size

Note 2: A_0, B_0 & K_0 are determined by component size. The clearance between the components and the cavity must be within .05mm min to 1.0 mm max. The component cannot rotate more than 10° within the cavity

Note 3: Dimension B is for tape feeder clearance reference only.

Note 4: Leader length shall be 230mm min

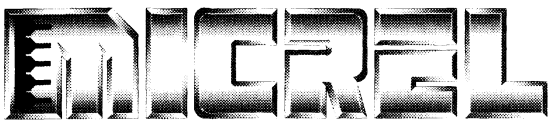
Note 5: Trailer length shall be 160mm min.

12

Worldwide Representatives and Distributors

WORLDWIDE REPRESENTATIVES AND DISTRIBUTORS

13



U.S. Sales Representatives

ALABAMA

Electronic Marketing Associates
7500 S. Memorial Parkway — Tel: (205) 880-8050
Ste. 215-A — Fax: (205) 880-8054
Huntsville, AL 35802

ALASKA

contact factory — Tel: (408) 944-0800

ARIZONA

Sun State Tech
2323 E. Magnolia, Ste. 115 — Tel: (602) 220-0595
Phoenix, AZ 85034 — Fax: (602) 220-0685

CALIFORNIA (NORTHERN)

W-J Electronic Sales
2118 Walsh Avenue, Ste. 140 — Tel: (408) 982-9222
Santa Clara, CA 95050 — Fax: (408) 982-9224

CALIFORNIA (SOUTHERN)

D² Sales Incorporated
777 S. Pacific Coast Hwy., Ste. 212 — Tel: (619) 481-9310
P.O. Box 1311 — Fax: (619) 481-2026
Solana Beach, CA 92075

Select Electronics
14730 Beach Blvd. — Tel: (714) 739-8891
Ste. 106, Bldg. F — Tel: (310) 921-5159
La Mirada, CA 90638 — Fax: (714) 739-1604

COLORADO

Lindberg Company
6140 East Evans Avenue — Tel: (303) 758-9033
Denver, CO 80222 — Fax: (303) 758-5863

CONNECTICUT

Dynamic Sales
6 Cedar Ridge Road — Tel: (203) 693-6567
Collinsville, CT 06022 — Fax: (203) 693-1302

DELAWARE

TCA Incorporated
Westown Business Center — Tel: (215) 692-6853
1570 McDaniel Drive — Fax: (215) 692-6873
West Chester, PA 19380

FLORIDA/PUERTO RICO

Micro-Electronic Components
400 Fairway Drive, Ste. 107 — Tel: (305) 426-8944
Deerfield Beach, FL 33441 — Fax: (305) 570-8568

Micro-Electronic Components
10637 Harborside Drive North — Tel: (813) 393-5011
Largo, FL 34643 — Fax: (813) 393-5202

Micro-Electronic Components
1305 Raintree Pl. — Tel: (407) 740-0023
Winter Park, FL 32789 — Fax: (407) 740-0083

Micro-Electronics Components/Caribe
P.O. Box 5038 — Tel: (809) 746-9897
Caguas, PR 00726 — Fax: (809) 746-9441

GEORGIA

Electronic Marketing Associates
6695 Peachtree Industrial Blvd. — Tel: (404) 448-1215
Ste. 101 — Fax: (404) 446-9363
Atlanta, GA 30360

HAWAII

contact factory — Tel: (408) 944-0800

IDAHO

SPS Electronic Sales
128 North Shore Circle — Tel: (503) 697-7768
Oswego, OR 97034 — Fax: (503) 697-7764

ILLINOIS

ESA Technical Marketing
5725 St. Charles Road, Ste. 211 — Tel: (708) 544-0120
Berkeley, IL 60163 — Fax: (708) 544-0266

INDIANA

Applied Data Management
P.O. Box 213 *(mailing)* — Tel: (317) 257-8949
Batesville, IN 47006 — Fax: (513) 579-8510

IOWA

J.R. Sales Engineering
1930 St. Andrews N.E. — Tel: (319) 393-2232
Cedar Rapids, IA 52402 — Fax: (319) 393-0109

KANSAS

contact factory — Tel: (408) 944-0800

U.S. Sales Representatives

KENTUCKY

Crest Component Sales
Mike Kilroy Corporation
12360 Hemple Road — Tel: (513) 696-2277
Farmersville, OH 45325 — Fax: (513) 696-2246

LOUISIANA

contact factory — Tel: (408) 944-0800

MAINE

Dynamic Sales
24 Ray Avenue — Tel: (617) 272-5676
Burlington, MA 01803 — Fax: (617) 273-4856

MARYLAND

Burgin-Kreh Associates, Inc.
7000 Security Blvd, Ste. 330 — Tel: (410) 265-8500
Baltimore, MD 21207 — Fax: (410) 265-8536

MASSACHUSETTS

Dynamic Sales
24 Ray Avenue — Tel: (617) 272-5676
Burlington, MA 01803 — Fax: (617) 273-4856

MICHIGAN

Applied Data Management
419 Village Green Blvd. Ste 203 — Tel: (313) 741-8558
Ann Arbor, MI 48105 — Fax: (313) 741-8754

MINNESOTA

George Russell Associates
8030 Cedar Avenue South — Tel: (612) 854-1166
Ste. 114 — Fax: (612) 854-6799
Minneapolis, MN 55425

MISSISSIPPI

Electronic Marketing Associates
7500 S. Memorial Parkway — Tel: (205) 880-8050
Ste. 215-A — Fax: (205) 880-8054
Huntsville, AL 35802

MISSOURI

contact factory — Tel: (408) 944-0800

MONTANA

SPS Electronic Sales
128 North Shore Circle — Tel: (503) 697-7768
Oswego, OR 97034 — Fax: (503) 697-7764

NEBRASKA

J.R. Sales Engineering
1930 St. Andrews N.E. — Tel: (319) 393-2232
Cedar Rapids, IA 52402 — Fax: (319) 393-0109

NEVADA (NORTH)

W-J Electronic Sales
2118 Walsh Avenue, Ste. 140 — Tel: (408) 982-9222
Santa Clara, CA 95050 — Fax: (408) 982-9224

NEVADA (SOUTH)

ESS Incorporated
2300 E. Patrick Lane, Ste. 5 — Tel: (702) 597-1661
Las Vegas, NV 89119 — Fax: (702) 597-1662

NEW HAMPSHIRE

Dynamic Sales
24 Ray Avenue — Tel: (617) 272-5676
Burlington, MA 01803 — Fax: (617) 273-4856

NEW JERSEY (NORTH)

Comp Tech Sales
232 Boulevard, Ste. 11 — Tel: (201) 288-7400
Hasbrouck Heights, NJ 07604 — Fax: (201) 288-7583

NEW JERSEY (SOUTH)

TCA Incorporated
Westown Business Center — Tel: (215) 692-6853
1570 McDaniel Dr. — Fax: (215) 692-6873
West Chester, PA 19380

NEW MEXICO

Lindberg Co.
4163 Montgomery, N.E. — Tel: (505) 881-1006
Albuquerque, NM 87109 — Fax: (505) 881-1007

NEW YORK (UPSTATE)

Harwood Associates
25 High Street — Tel: (516) 673-1900
Huntington, NY 11743 — Fax: (516) 673-2848

U.S. Sales Representatives

NEW YORK CITY/LONG ISLAND

Comp Tech Sales
232 Boulevard, Ste. 11 — Tel: (201) 288-7400
Hasbrouck Heights, NJ 07604 — Fax: (201) 288-7583

NORTH CAROLINA

Electronic Marketing Associates
6600 Six Forks Road, Ste. 201 — Tel: (919) 847-8800
Raleigh, NC 27615 — Fax: (919) 848-1787

NORTH DAKOTA

George Russell Associates
8030 Cedar Avenue South — Tel: (612) 854-1166
Ste. 114 — Fax: (612) 854-6799
Minneapolis, MN 55425

OHIO (NORTH)

Crest Component Sales
11681 Stafford Road — Tel: (216) 543-9808
Burton, OH 44021 — Fax: (216) 543-9800

OHIO (SOUTH)

Crest Component Sales
Mike Kilroy Corporation
12360 Hemple Road — Tel: (513) 696-2277
Farmersville, OH 45325 — Fax: (513) 696-2246

OREGON

SPS Electronic Incorporated
128 North Shore Circle — Tel: (503) 697-7768
Oswego, OR 97034 — Fax: (503) 697-7764

PENNSYLVANIA (EAST)

TCA Incorporated
Westown Business Center — Tel: (215) 692-6853
1570 McDaniel Dr. — Fax: (215) 692-6873
West Chester, PA 19380

PENNSYLVANIA (WEST)

Crest Component Sales
Synergistic Technical Services
P.O. Box 98148 — Tel: (412) 833-2522
Pittsburg, PA 15227-9998 — Fax: (412) 833-2522

RHODE ISLAND

Dynamic Sales
24 Ray Avenue — Tel: (617) 272-5676
Burlington, MA 01803 — Fax: (617) 273-4856

SOUTH DAKOTA

George Russell Associates
8030 Cedar Avenue South — Tel: (612) 854-1166
Ste. 114 — Fax: (612) 854-6799
Minneapolis, MN 55425

SOUTH CAROLINA

Electronic Marketing Associates
6600 Six Forks Road, Ste. 201 — Tel: (919) 847-8800
Raleigh, NC 27615 — Fax: (919) 848-1787

TENNESSEE

Electronic Marketing Associates
6695 Peachtree Industrial Blvd. — Tel: (404) 448-1215
Ste. 101 — Fax: (404) 446-9363
Atlanta, GA 30360

TEXAS

Kruvand Associates Inc.
13405 Floyd Circle, Ste. 112 — Tel: (214) 437-3355
Dallas, TX 75243 — Fax: (214) 580-8854

Kruvand Associates Inc.
11754 Jollyville Road, Ste. 109 — Tel: (512) 219-9443
Austin, TX 78759 — Fax: (512) 219-1932

UTAH

Lindberg Company
P.O. Box 526458 — Tel: (801) 484-8689
Salt Lake City, UT 84152 — Fax: (801) 484-9691

VERMONT

Dynamic Sales
Rd #1, Box 117-W — Tel: (802) 476-4223
Graniteville, VT 05654 — Fax: (802) 476-4223

U.S. Sales Representatives

VIRGINIA

Burgin-Kreh Associates, Inc.
7000 Security Blvd, Ste. 330
Baltimore, MD 21207
Tel: (410) 265-8500
Fax: (410) 265-8536

WASHINGTON

SPS Electronic Incorporated
21303 52nd West, Unit C216
Mountlake Terrace, WA 98043
Tel: (206) 323-4140
Fax: (206) 672-8766

WASHINGTON D.C.

Burgin-Kreh Associates, Inc.
7000 Security Blvd, Ste. 330
Baltimore, MD 21207
Tel: (410) 265-8500
Fax: (410) 265-8536

WEST VIRGINIA

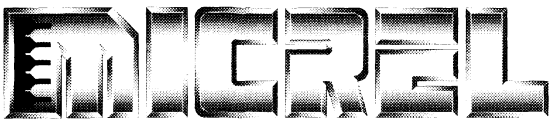
Crest Component Sales
Synergistic Technical Services
P.O. Box 98148
Pittsburg, PA 15227-9998
Tel: (412) 833-2522
Fax: (412) 833-2522

WISCONSIN

ESA Technical Marketing
5725 St. Charles Road, Ste. 211
Berkeley, IL 60163
Tel: (708) 544-0120
Fax: (708) 544-0266

WYOMING

Lindberg Company
6140 East Evans Avenue
Denver, CO 80222
Tel: (303) 758-9033
Fax: (303) 758-5863



U.S. Distributors

ALABAMA

Future Electronics
4825 University Square, Ste. 12 — Tel: (205) 830-2322
Huntsville, AL 35816

Jaco Electronics, Inc.
Tel: (800) 777-9373
Fax: (919) 876-6964

Nu Horizons
4801 University Square, Ste. 11 — Tel: (205) 722-9330
Huntsville, AL 35816 — Fax: (205) 722-9348

ARIZONA

Future Electronics
4636 E. University Dr., Ste. 245 — Tel: (602) 968-7140
Phoenix, AZ 85034

Jaco Electronics, Inc.
Tel: (602) 340-0752
Fax: (805) 494-3864

CALIFORNIA

Active Electronics (Retail Location)
1717 El Camino Real — Tel: (408) 249-5494
Santa Clara, CA 95051

Competitive Components
2013 W. Commonwealth, Unit K — Tel: (714) 871-8700
Fullerton, CA 92633 — Tel: (714) 871-3500
Tel: (800) 466-4036

Future Electronics
9301 Oakdale Ave., Ste. 210 — Tel: (818) 772-6240
Chattsworth, CA 91311

1692 Browning Ave. — Tel: (714) 250-4141
Irvine, CA 92714

5151 Shoreham Place, Ste. 220 — Tel: (619) 625-2800
San Diego, CA 92122

2220 O'Toole Ave. — Tel: (408) 434-1122
San Jose, CA 95131

Integrated Electronics Corp.
16 Technology, Ste. 125 — Tel: (714) 837-9960
Irvine, CA 92718 — Fax: (714) 837-8308

9940 Business Park Drive — Tel: (916) 363-6030
Ste. 145 — Fax: (916) 362-6926
Sacramento, CA 95827

Jaco Electronics, Inc.
San Diego, CA — Tel: (619) 549-8000
Fax: (714) 258-1909

2880 Zanker Road, Ste. 103A — Tel: (408) 432-9290
San Jose, CA 95134 — Tel: (800) 696-0948
Fax: (408) 432-9298

1541 Parkway Loop #A — Tel: (714) 258-9003
Tustin, CA 92680 — Fax: (714) 258-1909

2282 Townsgate Road — Tel: (805) 495-9998
Westlake, CA 91361 — Tel: (800) 350-9992
Fax: (805) 494-3864

Jan Devices Incorporated
6925 Canby, Building 109 — Tel: (818) 757-2000
Reseda, CA 91335 — Fax: (818) 708-7436

COLORADO

Future Electronics
12600 W. Colfax Ave., Ste. B110 — Tel: (303) 232-2008
Lakewood, CO 80215

Integrated Electronics Corp.
5750 N. Logan Street — Tel: (303) 292-6121
Denver, CO 80216 — Fax: (303) 292-2053

Jaco Electronics, Inc.
Tel: (303) 828-3074
Fax: (805) 494-3864

QPS Electronics Incorporated
12445 E. 39th Ave. Ste. 405 — Tel: (303) 373-2766
Denver, CO 80239 — Fax: (303) 373-4029

CONNECTICUT

Future Electronics
700 W. Johnson Ave. — Tel: (203) 250-0083
Cheshire, CT 06410

Jaco Electronics, Inc.
Tel: (800) 225-0818
Fax: (508) 640-0755

FLORIDA

Future Electronics
650 S. Northlake Blvd., Ste. 520 — Tel: (407) 767-8414
Altamonte Springs, FL 32701

Crown Center IV Bldg. — Tel: (305) 351-0660
1451 W. Cypress Creek Rd., Ste. 373
Ft. Lauderdale, FL 33309

2200 Tall Pines Dr., Ste. 108 — Tel: (813) 530-1222
Largo, FL 34641

U.S. Distributors

Jaco Electronics, Inc.
9900 West Sample Road, Ste. 404 Tel: (305) 341-8280
Coral Springs, FL 33065 Tel: (800) 776-5226
Fax: (305) 341-7848

Nu Horizons
600 South North Lake Blvd. Ste. 270 Tel: (407) 831-8008
Altamonte Springs, FL 32701 Fax: (407) 831-8862

3421 N.W. 55th Street Tel: (305) 735-2555
Ft. Lauderdale, FL 33309 Fax: (305) 735-2880

RM Electronics Company, Inc.
1237 Piney Branch Circle Tel: (407) 767-8005
Varico, FL 33594 Fax: (407) 767-8165

GEORGIA

Future Electronics
3150 Holcomb Bridge Road, Ste. 130 Tel: (404) 441-7676
Norcross, GA 30071

Jaco Electronics, Inc.
Tel: (800) 768-2868
Fax: (919) 876-6964

Nu Horizons
5555 Oakbrook Parkway, Ste. 370 Tel: (404) 416-8666
Norcross, GA 30093 Fax: (404) 416-9060

ILLINOIS

Active Electronics (Retail Location)
1776 W. Golf Road Tel: (708) 640-7713
Mount Prospect, IL

Future Electronics
3150 West Higgins Road, Ste. 160 Tel: (708) 882-1255
Hoffman Estates, IL 60195

Integrated Electronics Corp.
2200 N. Stonington Avenue Tel: (708) 843-2040
Ste. 210 Fax: (708) 843-2320
Hoffman Estates, IL 60195

QPS Electronics Incorporated
101 East Commerce Drive Tel: (708) 884-6620
Schaumburg, IL 60173 Fax: (708) 884-7573

Voyager Electronics Corporation
804 Thorndale Ave. Tel: (708) 860-1300
Bensenville, IL 60106 Fax: (708) 860-1573

INDIANA

CAM/RPC Electronics
1329 W 96th Street, Ste. 210 Tel: (317) 580-9999
Indianapolis, IN 46260 Fax: (317) 580-9615

RM Electronics
1329 W 96th Street, Ste. 10 Tel: (317) 291-7110
Indianapolis, IN 46260 Fax: (317) 580-9615

KANSAS

Future Electronics
8826 Sante Fe Drive, Ste. 150 Tel: (913) 649-1531
Overland Park, KS 66212

MARYLAND

Active Electronics (Retail Location)
1530 Caton Center Dr., Ste. F Tel: (410) 536-5400
Baltimore, MD Fax: (410) 536-5406

Future Electronics
6716 Alexander Bell Dr., Ste. 101 Tel: (410) 290-0600
Columbia, MD 21046

Jaco Electronics, Inc.
Rivers Center Tel: (410) 995-6620
10270 Old Columbia Road Fax: (410) 995-6032
Columbia, MD 21046

Nu Horizons
8965 Guilford Road, Ste. 160 Tel: (410) 995-6330
Columbia, MD 20146 Fax: (410) 995-6332

MASSACHUSETTS

Active Electronics (Retail Location)
11 Cummings Park Tel: (617) 932-0050
Woburn, MA 01801

Future Electronics
41 Main Street Tel: (508) 779-3000
Bolton, MA 01740

Jaco Electronics, Inc.
1053 East Street Tel: (508) 640-0010
Tewksbury, MA 01876 Fax: (508) 640-0755

Nu Horizons
19 Corporate Place Tel: (617) 246-4442
107 Audubon Road, Building 1 Fax: (617) 246-4462
Wakefield, MA 01880

U.S. Distributors

MICHIGAN

Active Electronics (Retail Location)
1393 Wheaton, Ste. 100 Tel: (313) 698-8000
Troy, MI 48083

Calder Electronics
4245 Brockton Dr. S.E. Tel: (616) 698-7400
Grand Rapids, MI 49508 Fax: (616) 698-9216

Future Electronics
4505 Broadmoor S.E. Tel: (616) 698-6800
Grand Rapids, MI 49512

35200 Schoolcraft Road, Ste. 106 Tel: (313) 261-5270
Livonia, MI 48150

RM Electronics
4310 Roger B Chaffee, S.E. Tel: (616) 531-9300
Grand Rapids, MI 49548 Fax: (616) 531-2990

MINNESOTA

Future Electronics
10025 Valley View Rd., Ste. 196 Tel: (612) 944-2200
Eden Prairie, MN 53045

Jaco Electronics, Inc. Tel: (612) 943-3908
6458 City West Pkwy. Fax: (612) 941-0327
Eden Prairie, MN 55344

Voyager Electronics Corporation
5201 East River Road Tel: (612) 571-7766
Fridley, MN 55421 Fax: (612) 571-9519

MISSOURI

Future Electronics
12125 Woodcrest Executive Dr. Tel: (314) 469-6805
Ste. 220
St. Louis, MO 63141

NEVADA

Competitive Components
1200 S. Jones #A4 Tel. (702) 878-7881
Las Vegas, NV 89102 Fax (702) 878-7661

NEW JERSEY

Active Electronics (Retail Location)
1871 Route 70 Tel: (609) 424-7070
Heritage Square
Cherryhill, NJ 08034

Future Electronics
12 E. Stow Rd., Ste. 200 Tel: (609) 596-4080
Marlton, NJ 08053

1259 Route 46 East Tel: (201) 299-0400
Parsippany, NJ 07054

Jaco Electronics, Inc.
Tel: (800) 989-JACO
Fax: (201) 942-0088

Nu Horizons
18000 Horizon Way, Ste. 200 Tel: (609) 231-0900
Mt. Laurel, NJ 08054 Fax: (609) 231-9510

39 U.S. Route 46 Tel: (201) 882-8300
Pine Brook, NJ 07058 Fax: (201) 882-8398

NEW YORK

Active Electronics (Retail Location)
3075 Veteran's Memorial Tel: (516) 471-5400
Ronkonkona, NY 11779

CAM/RPC Electronics
200 Buell Rd. #9 Tel: (716) 427-9999
Rochester, NY 14623-3183 Fax: (716) 427-7559

Future Electronics
801 Motor Pkwy. Tel: (516) 234-4000
Hauppauge, NY 11788

333 Metro Park Tel: (716) 272-1120
Rochester, NY 14623

200 Salina Meadows Pkwy., Ste. 130 Tel: (315) 451-2371
Syracuse, NY 13212

Jaco Electronics, Inc.
145 Oser Avenue Tel: (516) 273-5500
Hauppauge, NY 11788 Tel: (800) 989-JACO
Fax: (516) 273-5799

Nu Horizons
6000 New Horizons Blvd. Tel: (516) 226-6000
Amityville, NY 11701 Fax: (516) 226-5886

333 Metro Park Tel: (716) 292-0777
Rochester, NY 14623 Fax: (716) 292-0750

U.S. Distributors

NORTH CAROLINA

Future Electronics
Smith Towers, Suite 314
Charlotte Motor Speedway
P.O. Box 600
Concord, NC 28026
Tel: (704) 455-9030
Fax: (704) 455-9173

5225 Capital Blvd.
1 North Commerce Center
Raleigh, NC 27604
Tel: (919) 790-7111

Jaco Electronics, Inc.
5206 Greens Dairy Road
Raleigh, NC 27604
Tel: (919) 876-7767
Fax: (919) 876-6964

OHIO

CAM/RPC Electronics
749 Miner Road
Cleveland, OH 44143
Tel: (216) 461-8259
Fax: (216) 461-4329

733H Lakeview Plaza Road
Worthington, OH 43085
Tel: (614) 888-7777
Fax: (614) 888-1550

Future Electronics
6009-E Landerhaven Dr.
Mayfield Heights, OH 44124
Tel: (216) 449-6996

Nu Horizons
6200 S.O.M. Center Road
Solon, OH 44139
Tel: (216) 349-2008
Fax: (216) 349-2080

OREGON

Future Electronics
Cornell Oaks Corp. Center
15236 N.W. Greenbrier Pkwy.
Beaverton, OR 97006
Tel: (503) 645-9454

Integrated Electronics Corp.
3720 S.W. 141st Street, Ste. 102
Beaverton, OR 97005
Tel: (503) 641-1690
Fax: (503) 646-3737

Jaco Electronics, Inc.
Tel: (800) 245-JACO
Fax: (408) 432-9298

PENNSYLVANIA

CAM/RPC Electronics
620 Alpha Drive
Pittsburg, PA 15238
Tel: (412) 782-3770
Fax: (412) 963-6210

TEXAS

Future Electronics
9020 11 Capital TX Hwy. N.
Ste. 610
Austin, TX 78759
Tel: (512) 502-0991

10333 Richmond Ave., Ste. 970
Houston, TX 77042
Tel: (713) 785-1155

800 E. Campbell, Ste. 130
Richardson, TX 75081
Tel: (214) 437-2437

Jaco Electronics, Inc.
2120-A Braker Lane
Austin, TX 78758
Tel: (512) 835-0220
Fax: (512) 339-9252

1209 N. Glenville Drive
Richardson, TX 75081
Tel: (214) 234-5565
Fax: (214) 238-7068

Houston, TX
Tel: (713) 240-2255
Fax: (713) 240-6988

US Connections Inc.
Austin, TX
Tel: (512) 837-9892

1039-1 N. Stemmons Frwy. #333
Carrollton, TX 75006
Tel: (214) 245-0116
Fax: (214) 245-0034

5818 Arncliffe
Houston, TX 77088
Tel: (713) 956-9091

UTAH

Future Electronics
3450 South Highland, Ste. 301
Salt Lake City, UT 84106
Tel: (801) 467-4448

Integrated Electronics Corp.
Technology Park
2117 S. 3600 West
W. Valley City, UT 84119
Tel: (801) 977-9750
Fax: (801) 975-1207

WASHINGTON

Active Electronics (Retail Location)
13107 Northup Way 20th St. N.E.
Bellevue, WA 98005
Tel: (206) 881-8191

Future Electronics
19102 N. Creek Pkwy., Ste. 118
Bothell, WA 98011
Tel: (206) 489-3400

Jaco Electronics, Inc.
17220 127th Place N.E.
Woodinville, WA 98072
Tel: (206) 481-4837
Fax: (206) 481-1664

U.S. Distributors

Integrated Electronics Corp.
1750-124th Avenue N.E.
Bellevue, WA 98005
Tel: (206) 455-2727
Fax: (206) 453-2963

VESCO
716 Industry Drive
Tukwila, WA 98188
Tel: (206) 575-3607
Fax: (206) 575-1965

WISCONSIN

Future Electronics
250 N. Patrick Blvd., Ste. 170
Brookfield, WI 53045
Tel: (414) 879-0244

Taylor Electric Company
1000 West Donges Bay Road
Mequon, WI 53092
Tel: (414) 241-4321
Fax: (414) 241-4025

International Sales Representatives and Distributors

AUSTRALIA

R & D Electronics
4 Plane Tree Avenue — Tel: 61-3-558-0444
Dingley, Victoria 3171 — Fax: 61-3-558-0955

BELGIUM

Microlink S.A.
Paepsem Business Park — Tel: 32-2-5218650
Paepsemlaan 18E — Fax: 32-2-5216078
1070 Brussel

CANADA

Jaco Electronics, Inc.
1053 East Street — Tel: (508) 640-0010
Tewksbury, MA 01876 — Fax: (508) 640-0755

CANADA—ALBERTA

Active Electronics (Retail Location)
2015 32nd Ave. N.E., Unit 1 — Tel: (403) 291-5333
Calgary, AB T2E 6Z3 — Fax: (403) 291-5444

6029 103rd Street — Tel: (403) 438-5888
Edmonton, AB T6H 2H3 — Fax: (403) 436-1874

Future Electronics
3833 - 29th Street N.E. — Tel: (403) 250-5550
Calgary, AB T1Y 6B5 — Fax: (403) 291-7054

4606 - 97th Street — Tel: (403) 438-2858
Edmonton, AB T6E 5N9 — Fax: (403) 434-0812

CANADA—BRITISH COLUMBIA

Active Electronics (Retail Location)
100 S.E. Marine Dr. — Tel: (604) 654-1057
Vancouver, BC V5X 2S3 — Fax: (604) 324-3100

Future Electronics
1695 Boundary Road — Tel: (604) 294-1166
Vancouver, BC V5K 4X7 — Fax: (604) 294-1206

CANADA—MANITOBA

Active Electronics (Retail Location)
106 King Edward — Tel: (204) 786-3075
Winnipeg, MB R3H 0N8 — Fax: (204) 783-8133

Future Electronics
106 King Edward St. E. — Tel: (204) 944-1446
Winnipeg, MB R3H 0N8 — Fax: (204) 783-8133

CANADA—ONTARIO

Active Electronics (Retail Location)
1350 Matheson Blvd., Unit 2 — Tel: (416) 238-8825
Mississauga, ON — Fax: (416) 238-2817

1023 Merivale Road — Tel: (613) 728-7900
Ottawa, ON K1Z 6A6 — Fax: (613) 728-3586

100 Lombard Street — Tel: (416) 367-2911
Toronto, ON M5C 1M3 — Fax: (416) 367-4706

Electronic Sales Professionals (ESP) Inc.
5936 3rd Line Road North, RR#3 — Tel: (613) 489-3379
North Gower, ON K0A 2T0 — Fax: (613) 489-2778

Suite. 3, 447 McLeod Street — Tel: (613) 567-8547
Ottawa, ON K1R 5P5 — Fax: (613) 567-8548

27 Anne Court — Tel: (416) 458-1103
Brampton, ON L6T 1K2 — Fax: (416) 458-4469

60 Wilderness Drive — Tel: (416) 321-9693
Scarborough, ON M1V 3P6 — Fax: (416) 321-9794

Future Electronics
5935 Airport Rd., Ste. 200 — Tel: (416) 612-9200
Mississauga, ON L4V 1W5 — Fax: (416) 612-9185

Baxter Center — Tel: (613) 820-8313
1050 Baxter Road — Fax: (613) 820-3271
Ottawa, ON K2C 3P2

CANADA—QUEBEC

Active Electronics (Retail Location)
5651 Ferrier Street — Tel: (514) 731-7441
Montreal, PQ H4P 1N1 — Fax: (514) 731-0129

6080 Metropolitan Blvd — Tel: (514) 256-7538
Montreal, PQ H1S 1A9 — Fax: (514) 256-4890

1990 Boul. Charest Ouest, Suite 190 — Tel: (418) 682-5775
Ste. Foy — Fax: (418) 682-6282
Quebec, PQ G1N 4K8

Electronic Sales Professionals (ESP) Inc.
2102 Place Etienne-Brulé — Tel: (514) 388-6596
Montréal, PQ H2B 1Z2 — Fax: (514) 388-8402

Future Electronics
237 Hymus Blvd. — Tel: (514) 694-7710
Pointe Claire, PQ H9R 5C7

1000 Ave. St. Jean Baptist, Ste. 100 — Tel: (418) 877-6666
Quebec, PQ G2E 5G5 — Fax: (418) 877-6671

International Sales Representatives and Distributors

DENMARK

Ditz Schweitzer
Vallensbaekvej 41 Tel: 45-42-453044
DK 2605 Brondby Fax: 45-42-459206

FINLAND

Integrated Electronics Oy Ab
Turkhaudantie 1 Tel: 3580-351-3133
SF-00700 Helsinki Fax: 3580-351-3134

FRANCE

Dim'Pex, Int.
7 Chemin de la Segue Tel: 33-1-56788914
BP 82 Fax: 33-1-57835621
33611 Cestas Cedex

ISC France
8, Avenue du 18 Juin 1940 Tel: 33-1-47083530
92500 Rueil, Malmaison Fax: 33-1-47329925

GERMANY

Astronic GmbH
Grunwalder Weg 30 Tel: 49-89-61303-336
8024 Deisenhofen Fax: 49-89-61316-68

DACOM West GmbH (Headquarters)
In der Freiheit 48 Tel: 49-212-593011
5650 Solingen 1 Fax: 49-212-591639

Kamaka Electronic GmbH
Rheinsrraße 22 Tel: 49-7275-8600
76870 Kandel Fax: 49-7275-8675

HONG KONG

Glory Tact Co., Ltd.
Rm. 405, Tower A Tel: (852) 333-3688
Hunghom Commercial Centre, 37-39 Fax: (852) 333-3399
Ma Tau Wai Rd. Hunghom, Kowloon, H.K.

INDIA

Samura Electronics Private Ltd.
23-122, Plot-189 Tel: 011 91 842 831344
Bhoodevi Nagar Fax: 011 91 842 841697
Secunderabad, A.P., Pin - 500 015

ISRAEL

El-Gev Electronics, Ltd.
Building 101 P.O. Box 50 Tel: (972) 3-9712056
Tirat Yehuda 73175 Fax: (972) 3-9712407

ITALY

Sprague Italiana SpA
Via G. De Castro, 4 Tel: 39-2-48012355
20144 Milano Fax: 39-2-48008167

JAPAN

Nippon Imex Corporation
No. 6 Sanjo Bldg., 5F Tel: 81-3-33218000
1-46-9 Matsubara Setagaya-ku Fax: 81-3-33250021
Tokyo 156, Japan

KOREA

ENC Korea Ltd.
#202 Sungkyung Blvd Tel: 82-2-5793330
66 Yangjae-Dong Fax: 82-2-5794440
Seocho-Ku
Seoul

Shinhwa Corporation
ZF. The Christian Literature Society Tel: 82 (02) 554-6431
of Korea Bldg. Fax: 82-2-554-7649
169-1, Samsung-Dong
Kangnam-Ku
Seoul

MALAYSIA

Desner (Malaysia) Sdn. Bhd.
23 Jalan Sarikei Tel: 03-4211123
53000 Kuala Lumpur Fax: 03-4219923

Desner (Malaysia) Sdn. Bhd.
39 Persiaran Bukit Kecil 5 Tel: 04-838352
Tam Sri Nibong Fax: 04-849370
11900 Bayan Lepas
Penang

NETHERLANDS

Nijkerk Elektronika BV
Drentestraat 7 Tel: 31-20-549-5969
Amsterdam - 1083HK Fax: 31-20-642-3948

PHILIPPINES

Crystalsem Incorporated
216 Ortega Street Tel: 632-79-05-29
San Juan, Metro Manila 1500 Fax: 632-722-1006

International Sales Representatives and Distributors

SINGAPORE

Desner Electronics (Far East) Pte. Ltd.
42 Maetaggart Road #04-01 Tel: 65-2851566
Maetaggart Building Fax: 65-2849466
Singapore 1336

SOUTH AFRICA

Prime Source (PTY) Ltd.
Prime Source House Tel: (27) 11 444-7237
3 Olympia Street, Marlboro Fax: (27) 11 444-7298
P.O. Box 46169, Sandton
Orange Grove 2119

SPAIN

Unitronics S.A.
Pza Espana, 18. PL9 Tel: 34-1-542-5204
28008 Madrid Fax: 34-1-542-7896

SWEDEN

Keltech Components, AB
Box 505 Tel: 46-8-630-8590
Kemistvagen 10 A Fax: 46-8-756-2143
S-183 25 TABY

SWITZERLAND

Electronitel
CH du Grand Clos 1 Tel: 41-37-410060
P.O. Box 93 Fax: 41-37-410070
CH1752 Villars Sur Glane

TAIWAN, R.O.C.

Helm Engineering & Trading Co.
4F, 76 Tun Hua S. Rd. Sec. 2 Tel: (02) 7091888
Taipei, Taiwan Fax: (02) 7060465
Fax: (02) 7557992

Mostek Enterprise Co., Ltd.
8 Fl. No. 82 Lane 142, Sec. 6 Tel: 886-2-9351498
Roosevelt Road Fax: 886-2-9351497
Taipei, Taiwan

THAILAND

Desner Electronics (Thailand) Co. Ltd.
ITF Silom Palace Building Tel: 235-6492 ext. 128
11th Floor, Room 160/128-129 Fax: 266-8040
Silom Road
Bankok 10500

U.K.

Pact Electronics Limited
14 Orchard Road Tel: 0483-502581
Onslow Village Fax: 0483-502581
Guildford, Surrey GU2 5QY

Profile Electronic Componets Ltd.
Studio 2 Tel: 44-252-717771
The Farnham Malting Fax: 44-256-70469
Bridge Square
Farnham, Surrey GU9 7QR

Solid State Supplies
Unit 2, Eastlands Lane Tel: (44) 892-836836
Paddock Wood Fax: (44) 892-837837
Kent TN12 6BU